Application Report
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Supported synchronization modes for TI network synchronizers

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ABSTRACT

This application report outlines the advantages of using ultra-high performance network synchronizer clocks from Texas Instruments to maintain synchronization in packet switched networks that support Synchronous Ethernet, and IEEE1588. Configurations for maintaining synchronization using LMK05318 is described.

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Trademarks

1 Introduction

Synchronization is an important aspect of telecommunication networks for the following reasons:

- Supporting voice and data traffic to/from cellular base stations
  - Synchronization allows smooth call hand-off between base stations, it minimizes dropped calls
- Supporting services that require accurate timestamping like the financial transactions, digital forensics, voice/fax
- Increasing network efficiency through managed bandwidth utilization
- Improving overall quality of service

2 Synchronization in Circuit Switched Networks

Legacy circuit switched networks, like SONET/SDH, are telephony (ATM) based with fixed frame length and are point-to-point that needs support for frequency synchronization only with no explicit need for time synchronization. Such networks work well for voice and low bandwidth data transmission. However, support for high bandwidth spectrums result in unmanageably high line rates and thus extremely expensive to upgrade. Circuit switched networks are also not easily scalable, making them inefficient to handle the exploding user data traffic, and do not work well with switching traffic that operate on packets with varying lengths. Figure 1 shows an example of a legacy telecom network.

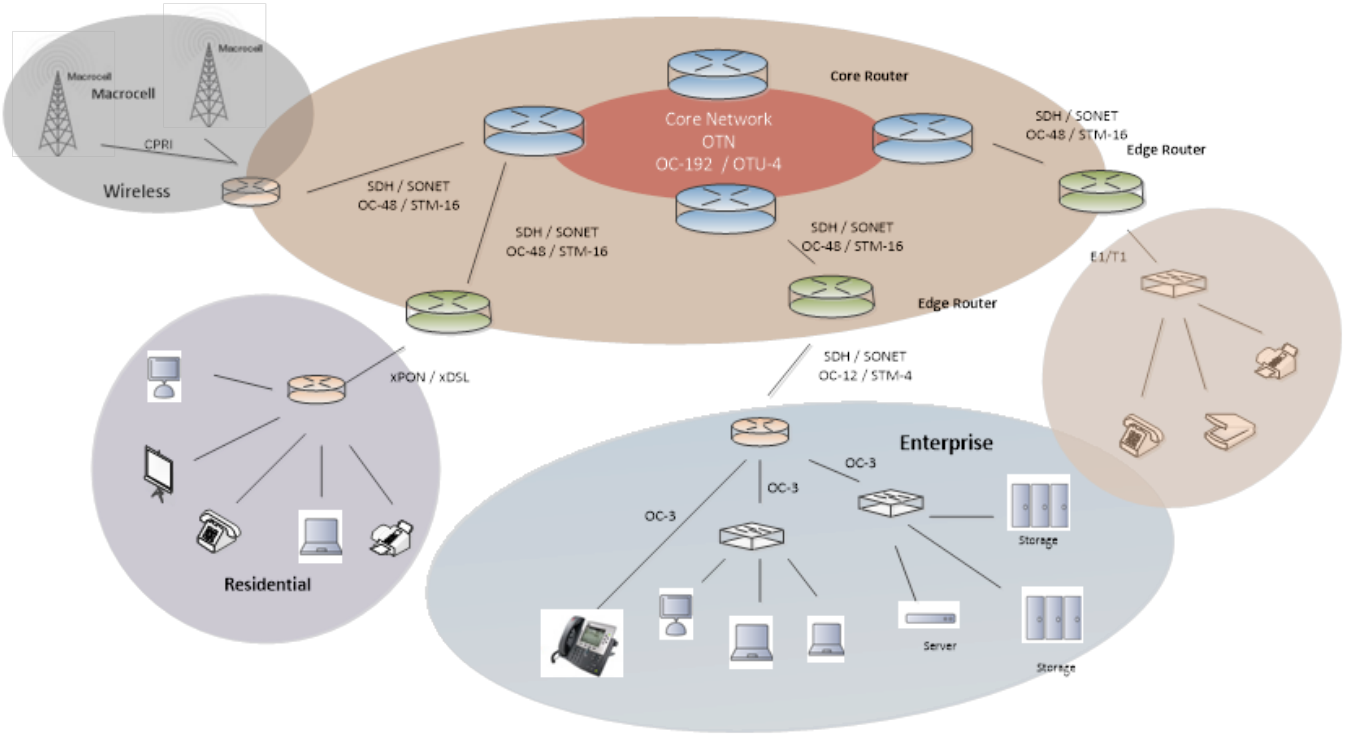

Figure 1. Example of Legacy Telecom Network

2.1 Synchronization in SONET/SDH

Networks based on time division multiplexing (TDM), such as SONET/SDH, require frequency synchronization at every network element (NE) for efficient data transmission. Achieving frequency synchronization at every NE is accomplished with hierarchical categories, based on the desired frequency accuracy, called stratum levels. The hierarchy starts with the highest level of frequency accuracy, defined as a stratum 1 or primary reference clock (PRC) source, with better than ±10 ppt free run accuracy. The stratum 1 source is transmitted to the building integrated timing supply (BITS), defined as a stratum 2 clock, with better than ±16 ppb free run accuracy. The stratum 2 source is transmitted to all the NE, defined as a stratum 3 clock, with better ±4.6 ppm free run accuracy. The example in Figure 2 shows the timing hierarchy where the first NE which is locked to the stratum 2 source is called “External Timed NE”. All of the remaining NE’s can now lock to the first NE and are called “Line Timed NE”.

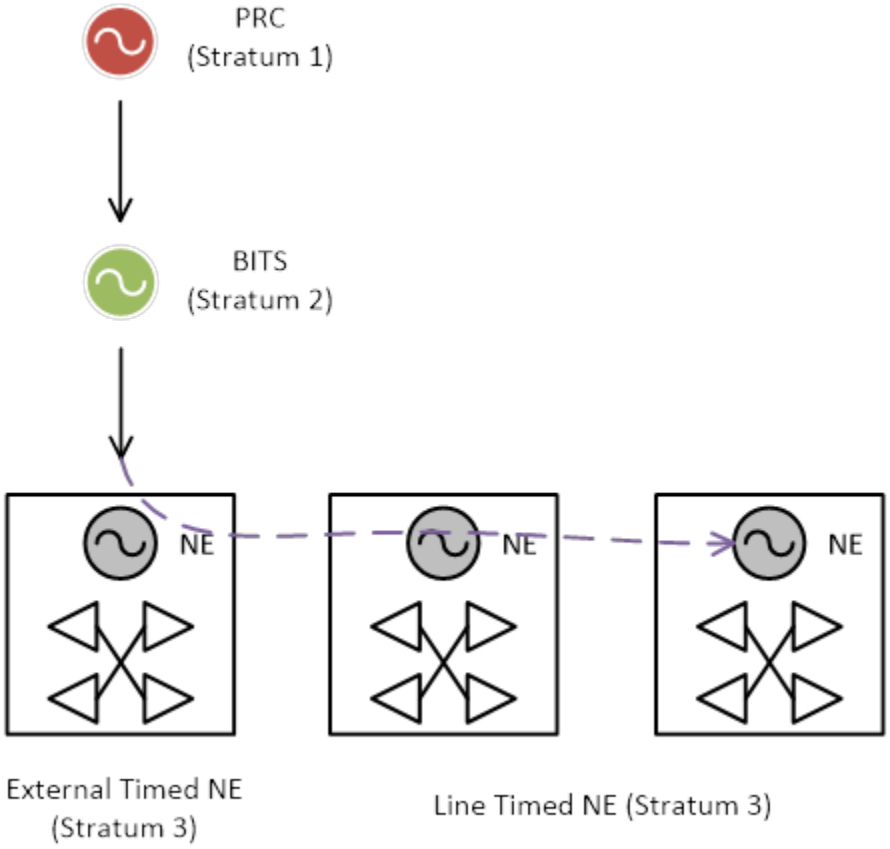

Figure 2. Line Timing Distribution in SONET/SDH

3 Synchronization in Packet Switched Networks

Packet switched networks are multi-point with variable frame lengths and inherently asynchronous. They are cost effective compared to circuit switched networks. But some services require the ability to provide synchronized services as listed in Section 1. Moreover, newly deployed packet switched networks need to be interoperable with existing circuit switched networks. The example network in Figure 3 illustrates a core packet network combined with a TDM network, like xDSL, that is responsible for distributing services closer to the customer premises. To guarantee synchronization across the entire network, packet switched networks need to support means to distribute time and frequency.

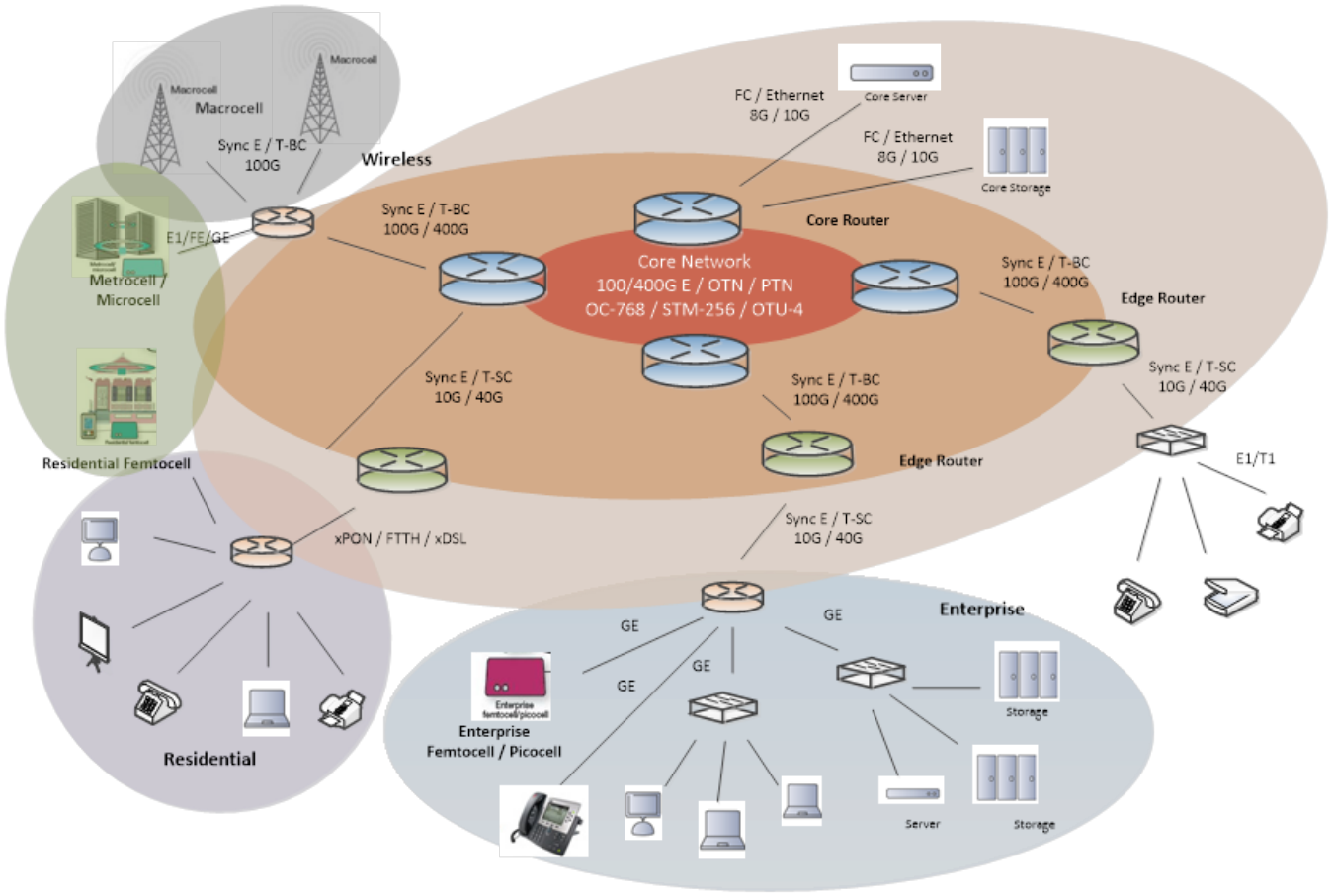

Figure 3. Example of Packet Switched Telecom Network

3.1 Synchronization With Synchronous Ethernet and Precision Time Protocol

Synchronous Ethernet (SyncE) is a way to distribute frequency on physical layer similar to the concept of line timing as described in Section 2.1. However, SyncE cannot provide time synchronization. Precision Time Protocol (PTP), which is standardized by IEEE1588, has been universally adopted to distribute time with hierarchical categories, based on the desired time accuracy. The hierarchy starts with the highest level of time accuracy, defined as a grandmaster or primary reference time clock (PRTC), with “ps” time accuracy. The grandmaster source is transmitted via timestamps in packets to the intermediate nodes where each is defined as a boundary clock, with “ns” time accuracy. The boundary clock source is transmitted via timestamps in packets to the endpoints where each is defined as a slave clock, with “ns” time accuracy. Figure 4 shows an example network with synchronization handled by SyncE and IEEE1588.

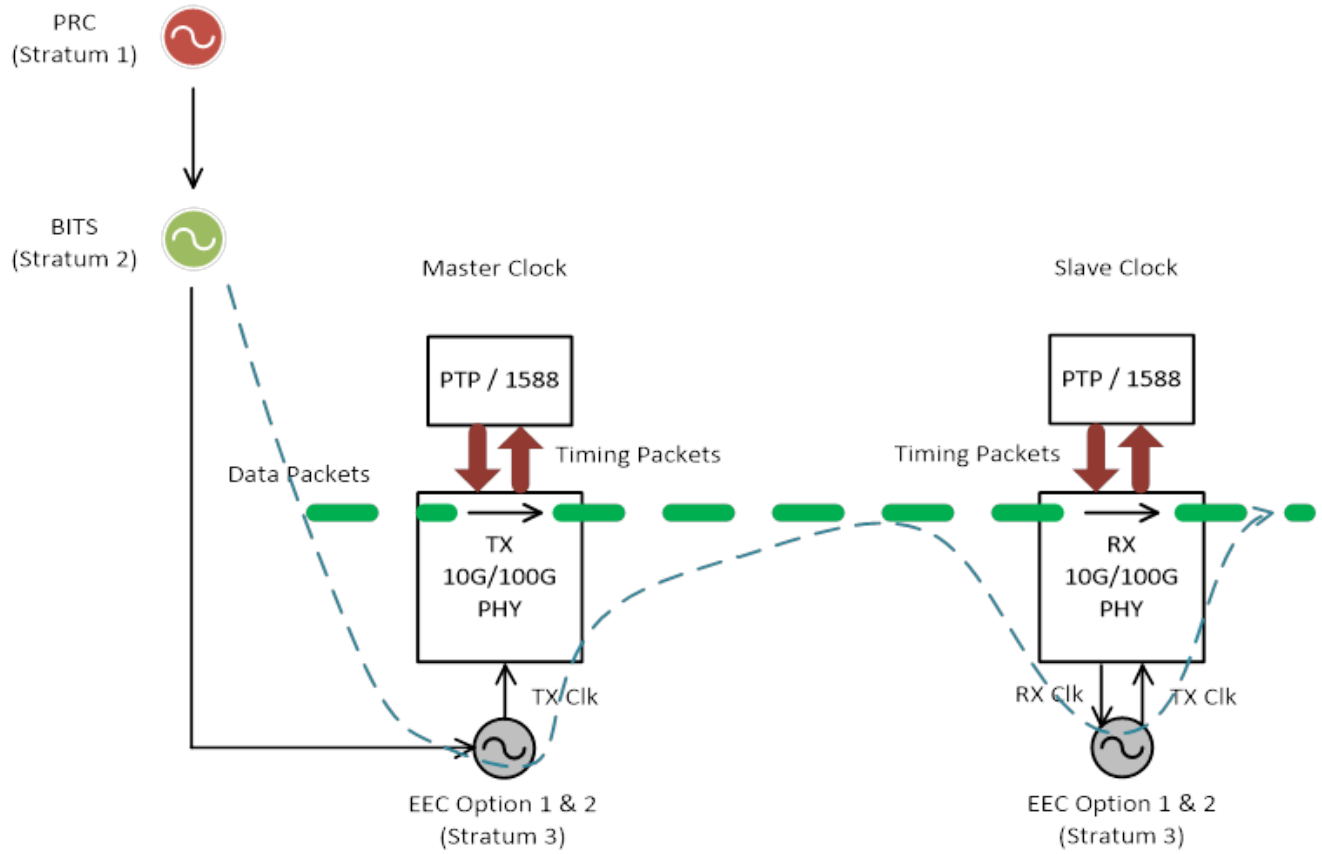

Figure 4. Synchronization With SyncE and IEEE1588

4 Synchronization in Packet Switched Networks With LMK05318

TI's LMK05318 device is an ultra-high performance clock generator, jitter cleaner, and clock synchronizer with advanced reference clock selection and hitless switching feature to meet the stringent requirements of communications infrastructure applications. The ultra-low jitter performance of this device minimizes bit error rates (BER) in applications involving high-speed serial links and is TI's recommended clocking solution for 400G Ethernet where better than 150 fs, rms jitter is required. The device features a single channel synchronizer that can synchronize to one of two differential or single-ended reference clock inputs. The synchronizer is accompanied by one PLL domain that features TI's proprietary Bulk Acoustic Wave (BAW) resonator as a VCO and generates 50 fs, rms jitter and exceeds the 400G Ethernet reference clock needs. There is an additional PLL domain that can be used to generate unrelated frequencies either locked to the reference clock input or the free-run XO input and generates 120 fs, rms jitter. The LMK05318 can generate up to eight high performance output clocks with up to six different frequencies. The advanced synchronization options in each PLL core include superior hitless switching, digital holdover, DCO mode with less than 1 ppt/step for precise clock steering (IEEE 1588 PTP slave operation), supports PLL lock and switchover with 1PPS inputs and zero delay for deterministic input-to-output phase offset.

The LMK05318 is an ideal solution for use in line cards and fabric cards of a modular switch or router as shown in Figure 5. The key features of the LMK05318 include:

- Fully compliant with SyncE requirements (ITU G.8262). Supports EEC Option 1 and EEC Option 2.
- Industry leading jitter of 50 fs, rms using TI's proprietary BAW VCO technology and is independent of the reference clock jitter and system clock frequency and jitter.
- Industry leading phase transient (hitless switching) of ±50 ps using phase cancellation.
- Automatic/manual hitless switching and holdover during loss of input clock.

- IEEE1588 support offered via:
  - DCO mode with ±1 ppt step size
  - Lock to 1PPS input
- Robust operation with PSRR of better than -80 dBc in the presence of supply noise of 50 mV ripple.
- On-chip EEPROM, with re-writes up to 100 times, enables no in-system programming after power up.
- High level of programmability with multiple device monitoring options that can be read via I2C/SPI or by polling STATUS pins.
- Programmable output clock signal format: AC-LVPECL, AC-LVDS, AC-CML, HCSL and LVCMOS
- Operates from a 3.3 V core supply and 1.8 / 2.5 / 3.3 V output supply

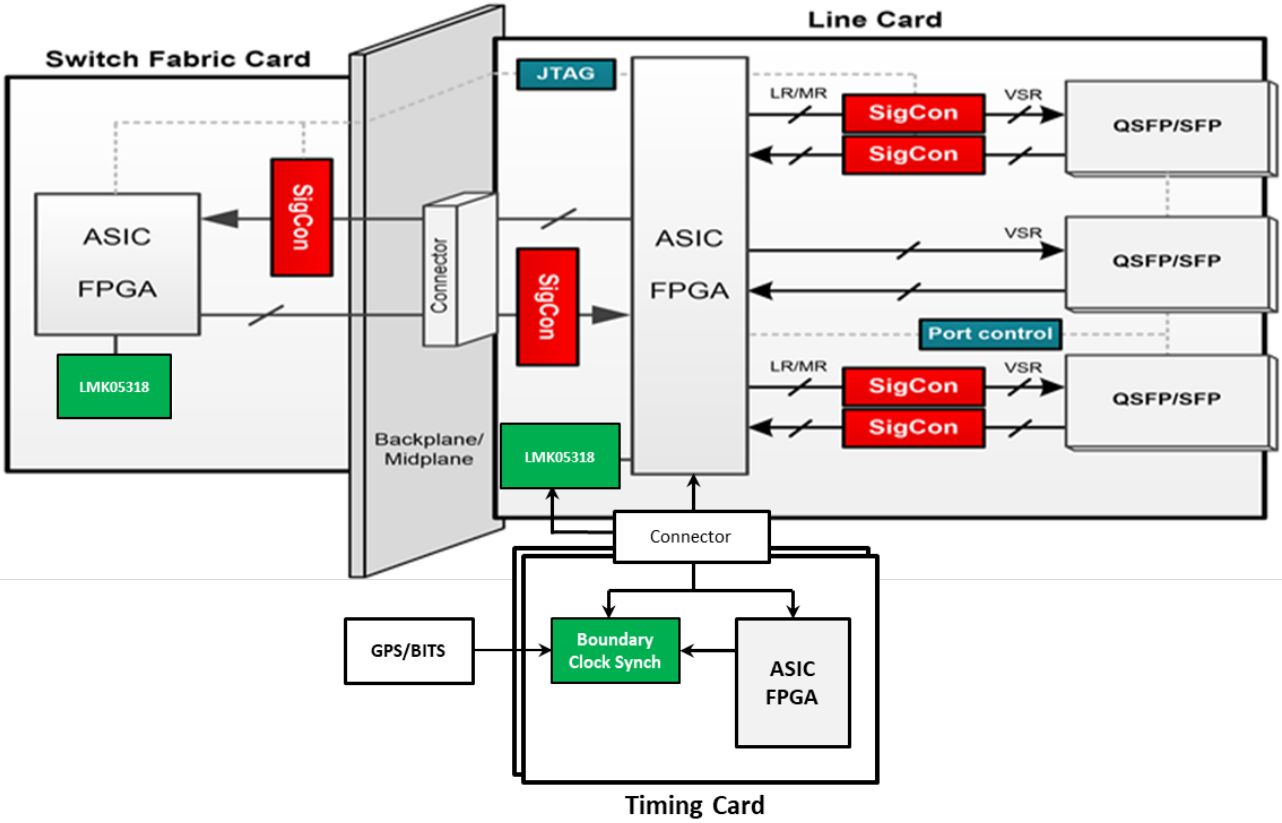

Figure 5. Architecture of Modular Switch Design

When the LMK05318 is used in a line card, it accepts TDM or Ethernet recovered clock frequencies directly from a PHY or a redundant backplane and generates synchronous Ethernet clock frequencies that exceed the jitter specifications of 400G Ethernet PHYs. The support for IEEE1588 can be handled by utilizing the Switch SoC or FPGA as the PTP master and LMK05318 as the PTP slave. Timing packets are recovered from the receive PHY and the Switch SoC or FPGA retrieves the extracted IEEE1588 timestamps, processes the information using a servo loop algorithm, and steers the LMK05318 which is operated as a digitally controlled crystal oscillator (DCO) to produce the clocks that frequency synchronized to the SyncE physical layer clock that is traced back to the PRC and time synchronized to a traceable PRTC.

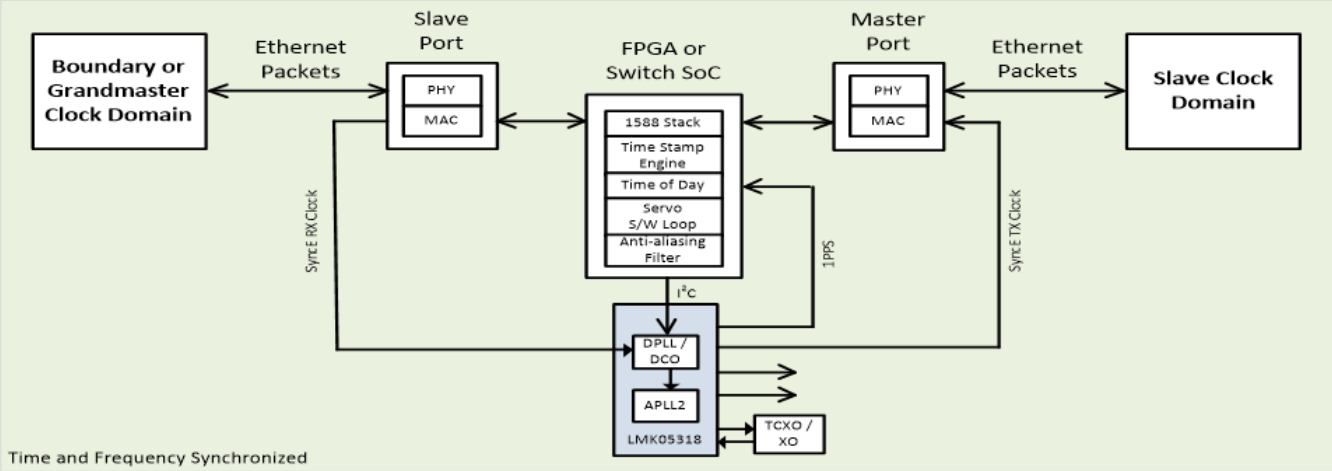

Figure 6. LMK05318 Implementation in a Line Card

Figure 6 consists of the following elements:

- Switch SoC or FPGA
  - Supports 1588 Stack, Time Stamp Engine, and ToD (Time of Day) functions.
  - Processes and switches or routes PTP packets.
  - Hosts servo loop software.
  - Adjusts LMK05318 phase in DCO (Digitally Controlled Oscillator) mode via I2C/SPI.
- LMK05318
  - DCO mode provides precise frequency adjustment with 1 ppt step size.
  - Generates a 1 PPS clock locked to upstream recovered SyncE, phase adjusted per PTP packets, which feeds back to the FPGA.
  - Supplies a downstream SyncE transmit clock also locked to recovered SyncE clock.

5 Summary

Ultra-high performance network synchronizer clocks from TI, like the LMK05318, offer industry leading jitter and phase transient that exceed requirements of serial links up to 400G Ethernet. It also offers support for SyncE and IEEE1588 to guarantee time and frequency synchronization. TI also offers WEBENCH Clock Architect Tool that helps the hardware engineers to select the appropriate settings for the LMK05318 that meet their requirements.

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (November 2018) to A Revision	Page
• Changed document title from: *Supported Synchronization Modes With LMK05318* to: *Supported synchronization modes for TI network synchronizers*	1

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