Application Report
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TI Network Synchronizer Clock Value Adds in Communications and Industrial Applications

Arvind Sridhar, Shawn Han, Alan Ocampo

ABSTRACT

This application note introduces features and performance of TI's first Network Synchronizer Clock device, LMK05028. The application note highlights the device's unique 3-loop architecture, Hitless Switching with Phase Cancellation, 1 PPS Phase Lock, Zero Delay Mode, and Robust Reference Detector, and discusses their value adds in several applications, including wired communications (Switches, Routers and Optical Transport Networks), wireless communication (Base Band Unit), and industrial applications, such as smart grids, medical imaging, and broadcast video. In these applications, the LMK05028 operates as a high-performance clock generator and jitter cleaner with Programmable Loop Bandwidth, while also offering network synchronization with support for Synchronous Ethernet (SyncE) and IEEE 1588.

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1 DPLL Introduction

A basic Analog Phase Locked Loop (APLL) can generate a tunable frequency source from a fixed reference clock. This is accomplished means of a VCO (Voltage Controlled Oscillator), which is a voltage to frequency converter. The output frequency of the VCO is divided by a feedback divider N and compared to the reference clock frequency, F_{REF} (Ref Osc/R). The Phase Frequency Detector (PFD) / Charge Pump compares these two frequencies and puts out current correction pulses proportional to the phase and frequency difference between the two signals. The correction pulses from the PFD are filtered by the loop filter, which converts them into a voltage to steer the VCO frequency and phase. The N and the R Dividers are typically programmable. The output frequency, F_{OUT} is given by the following equation.

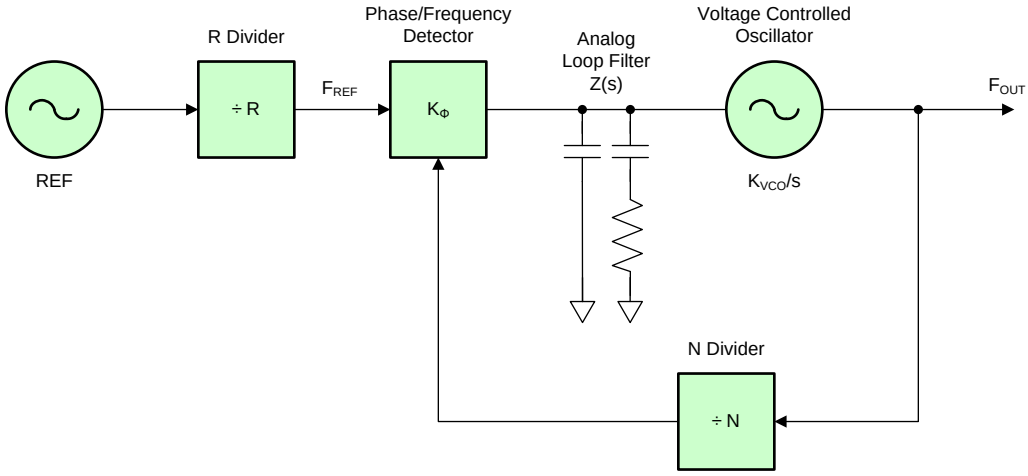


Figure 1. The Basic Analog PLL

$$F_{OUT} = F_{REF} \times N / R \quad (1)$$

DPLLs typically have a control loop structure similar to an APLL, and Equation 1 still applies. Notable differences between the two are that the Time-to-Digital Converter (TDC) replaces PFD, Digital Loop Filter replaces Analog Loop Filter and Digitally-Controlled Oscillator (DCO) replaces VCO. The digital nature of the DPLL helps system engineers to optimize loop parameters without hardware changes, and record tuning word history for maintaining holdover accuracy in certain applications.

DPLLs find use in applications requiring superior hitless switching performance and controlled holdover entry and exit.

Analogous to APLLs, DPLLs suffer from spurs caused by VCO, Reference Inputs, Output channel crosstalk, noise from fractional feedback dividers, power supply noise, and so forth. For optimal clock jitter performance, engineers should still pay attention to reference, System Clock Oscillator, VCO frequency selection, and loop filter design. Optimal configuration of DPLL loop filter parameters is a compute intensive task, and therefore a software tool is helpful to calculate, optimize, and generate register settings for the device. TI's software tool (TICS Pro) helps to simply this process for the user.

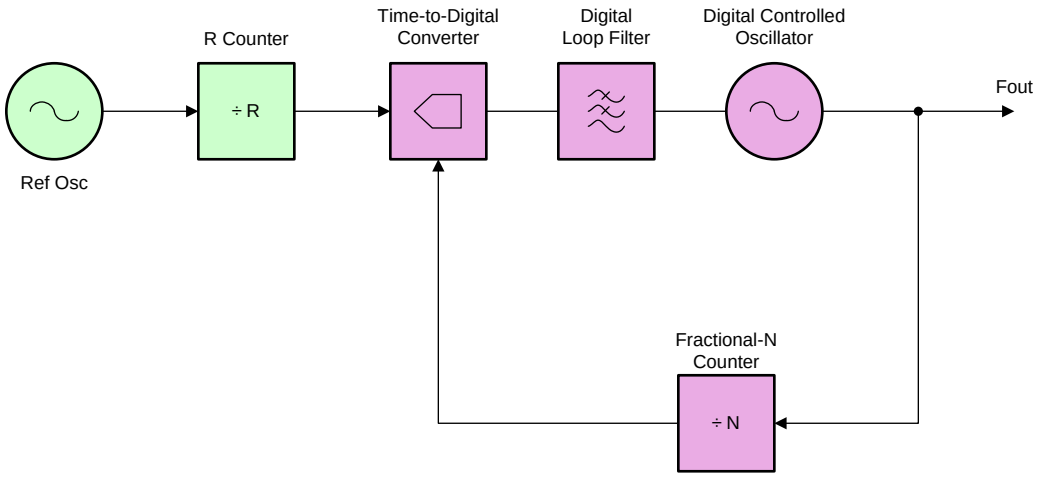


Figure 2. The Basic Digital DPLL

2 TI DPLL Overview

TI's LMK05028 device is a high-performance clock generator, jitter cleaner, and clock synchronizer with advanced reference clock selection and hitless switching feature to meet the stringent requirements of communications infrastructure applications. The ultra-low jitter performance of this device minimizes bit error rates (BER) in applications involving high-speed serial links.

The device has two independent PLL cores that can each synchronize or lock to one of four differential or single-ended reference clock inputs. The LMK05028 can generate up to eight high performance output clocks with up to six different frequencies. The advanced synchronization options in each PLL core include superior hitless switching, digital holdover, DCO mode with less than 1 ppt/step for precise clock steering (IEEE 1588 PTP slave operation), and zero delay for deterministic input-to-output phase offset.

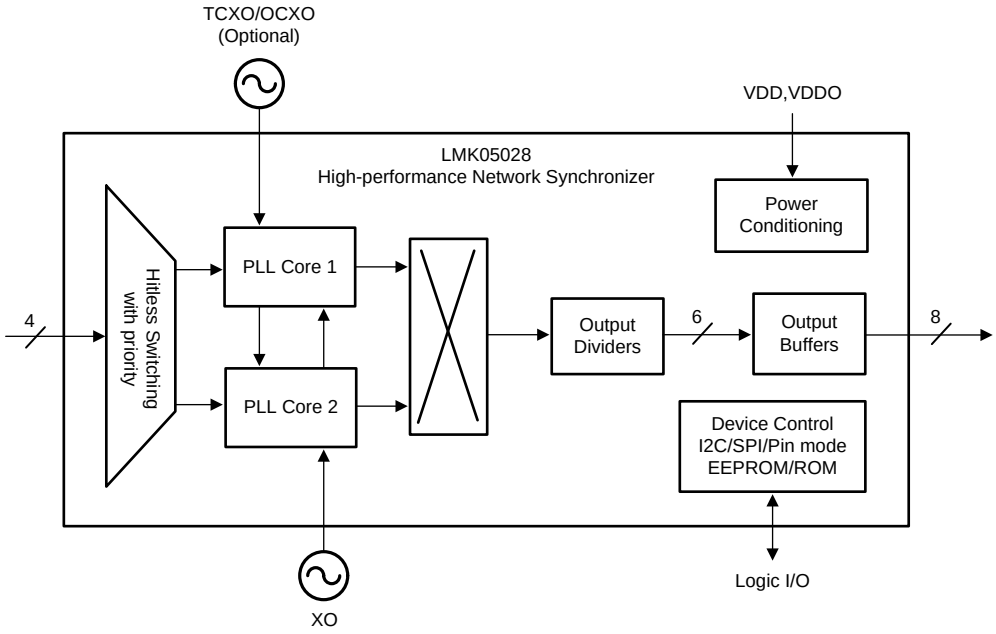


Figure 3. LMK05028 Simplified Block Diagram

Compared to traditional APLL and DPLL solutions in the market, LMK05028 has many differentiated features. Notable ones are:

- Unique 3-loop architecture
- Hitless Switching with Phase Cancellation
- 1 PPS Phase Lock
- Zero Delay Mode
- Robust Window Detector

2.1 Unique 3-Loop Architecture

Each PLL core of LMK05028 cascades up to 2 DPLL loops and 1 APLL loop as shown in Figure 4. The REF-DPLL gets external reference clocks and a feedback clock from APLL. The TCXO-DPLL typically receives a low-frequency local TCXO/OCXO as holdover reference input and a feedback clock from APLL. The TCXO feedback divider also is controlled by the REF-DPLL. The APLL locks to a local XO reference input, and its feedback divider is controlled by the correction word from either the TCXO-DPLL (in 3-loop mode) or REF-DPLL (in 2-loop mode). This unique architecture results in lower BOM cost by enabling customers to use a low frequency TCXO/OCXO holdover reference without sacrificing performance.

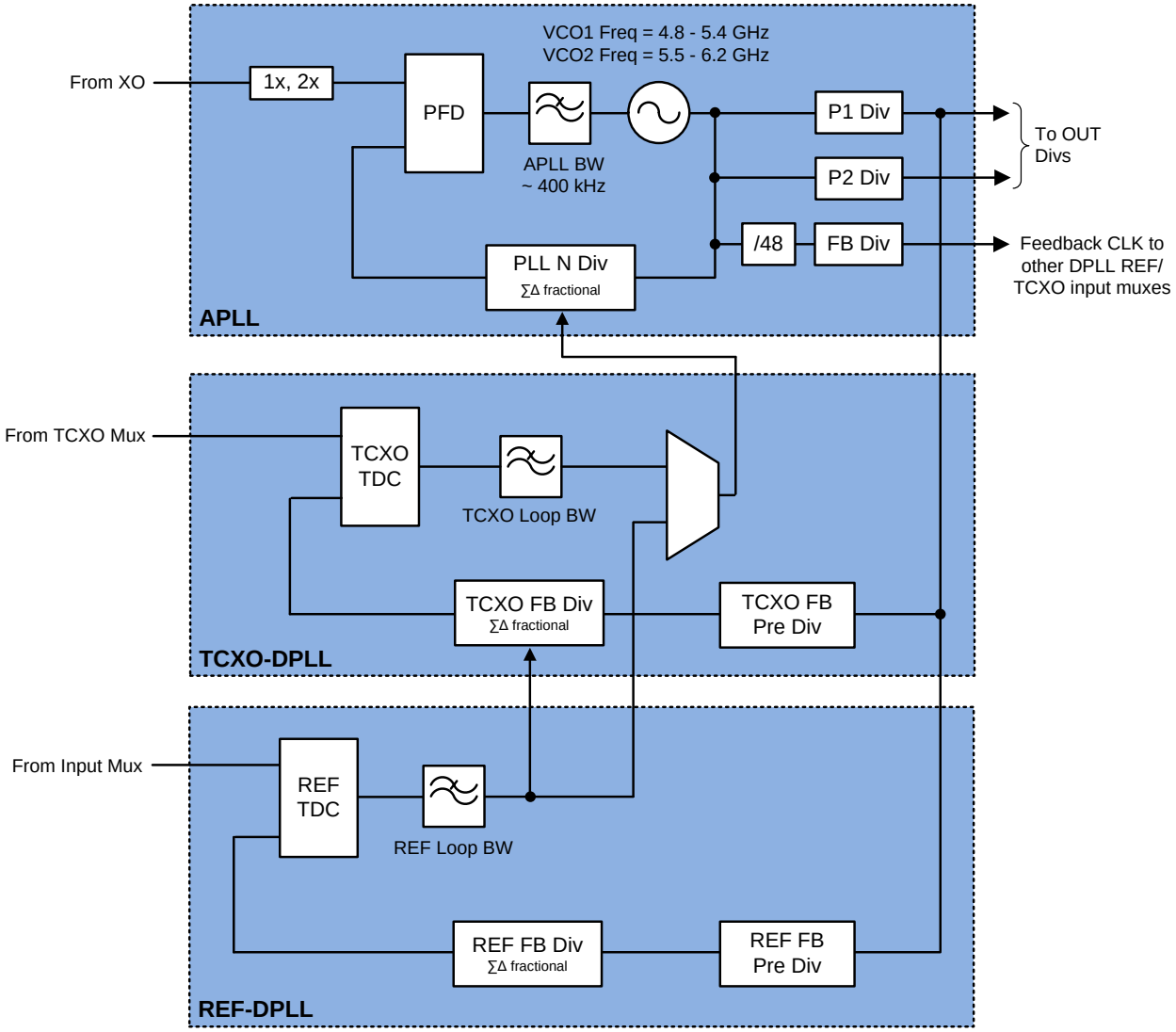
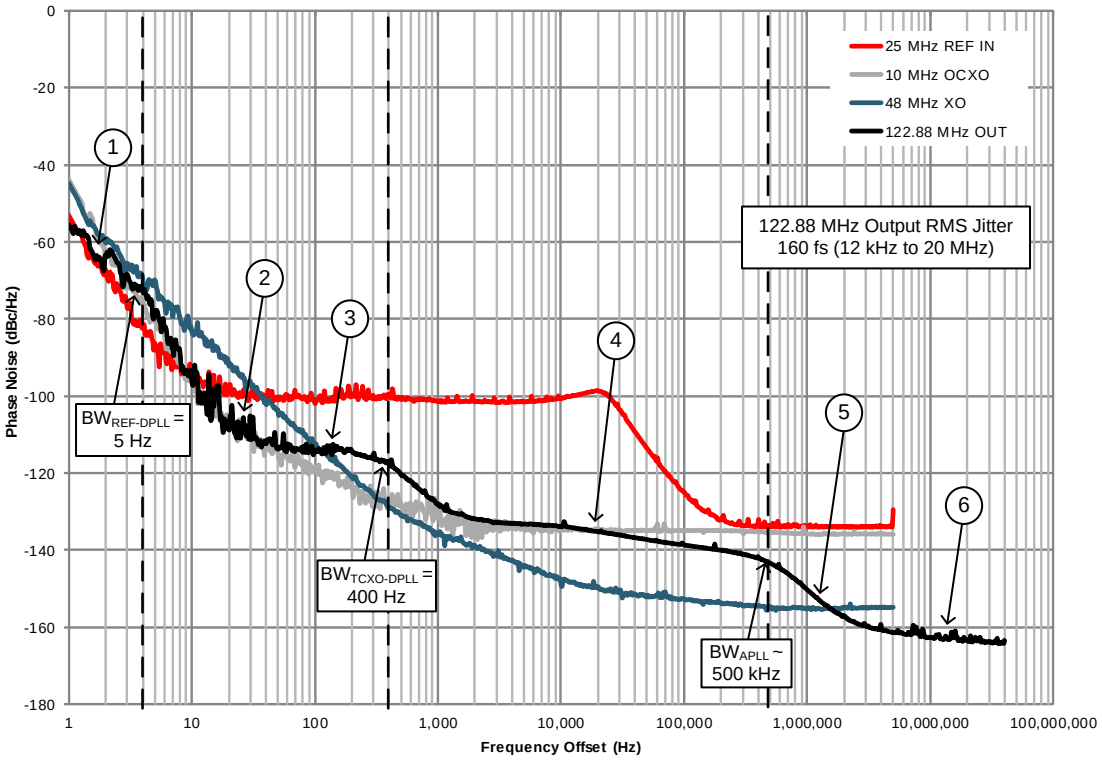


Figure 4. LMK05028 Functional Block Diagram (Single Channel Shown in Figure)

Figure 5 illustrates phase noise contribution of references to the overall phase noise in 3-loop mode. To simply the analysis, the phase noise of the reference to REF-DPLL (REF IN), TCXO-DPLL (OCXO) and APLL (XO) was normalized to the 122.88-MHz output clock. The 122.88-MHz OUT leverages the OCXO's low noise and stability in the range between BW_{REF} (5 Hz) and BW_{TCXO} (400 Hz), and leverage higher frequency XO to reduce APLL noise contribution in the range between BW_{TCXO} (400 Hz) and BW_{APLL} (500 kHz).

If a DPLL runs in 2-loop mode (TCXO-DPLL is bypassed) with a 48-MHz XO, the phase noise of final output will be increased in the range of 5 Hz to approximately 400 Hz. If a DPLL runs in 2-loop mode with a 10-MHz OCXO (as a reference to the APLL), the phase noise of final output will increase in the range of 400 Hz to approximately 500 kHz (close-in phase noise of APLL degrades when using a low-frequency reference). A higher frequency OCXO than 10 MHz is an option, comes at the expense of higher BOM cost. LMK05028's unique 3-loop architecture provides flexible configuration capability to satisfy both performance and cost targets for different applications.



1) Below $BW_{REF-DPLL}$, REF input noise contributes to output.
2) Above $BW_{REF-DPLL}$, REF input noise is attenuated and has no contribution to the output.
3) Below $BW_{TCXO-DPLL}$, OCXO and TDC_{TCXO} noise determine the output noise. TDC_{TCXO} flat noise is -115 dBc/Hz at 100 Hz offset.
4) Above $BW_{TCXO-DPLL}$, OCXO noise is attenuated. Below BW_{APLL}, APLL noise dominates as the XO noise contribution is much lower.
5) Above BW_{APLL}, VCO noise dominates and XO noise is attenuated.
6) AC-LVPECL output noise floor is -163 dBc/Hz.

Figure 5. Phase Noise Contribution From Various Sources (Device in 3-Loop Mode)

2.2 Hitless Switching With Phase Cancellation

Each PLL core of LMK05028 supports hitless switching through phase cancellation which restricts the rate of change of output phase during a reference switchover event in accordance with Stratum 3/4E, Stratum 2/3E, and Synchronous Ethernet EEC Option 1/Option 2. The reference input muxes supports automatic or manual input selection through software or hardware pin control. The reference switchover event will be hitless with superior phase transient performance in the range of 50 ps (typical) compared to 'ns' from competitors. Newer ASICs demand 'ps' level hitless switching and TI DPLLs are poised to exceed their requirements. The hitless switching performance of the device exceeds ITU-T G.8262 spec with practically no phase hits for synchronous input switching and smooth frequency transition while switching between asynchronous inputs.

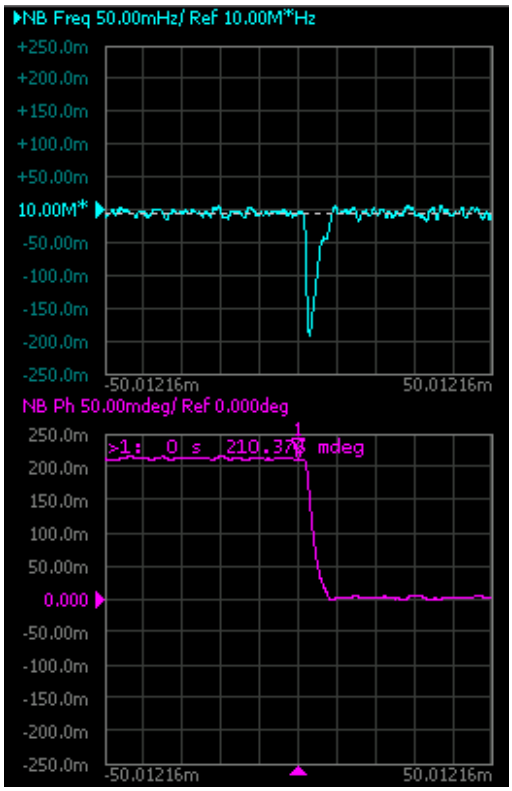


Figure 6. Hitless Switching in LMK05028 (10-MHz Output With Switching 25-MHz Inputs in 3-Loop Mode)

2.3 1 PPS Phase Lock

The LMK05028 3-loop mode supports 1 PPS input synchronization.

In classic synchronous clock generator application with GPS reference input, an FPGA plays the key role to detect 1 PPS signal from GPS, compare the phase error with a divided down clock from a Voltage Controlled Oven Controlled Crystal Oscillator(VC-OCXO) feedback clock. The FPGA then sends control data for DAC to calibrate VC-OCXO. FPGA can typically output synchronous clocks with their internal PLLs. However, if the jitter performance of the generated clocks from the FPGA's internal PLLs are not sufficient to meet the stringent needs of the end application, or there are multiple high performance frequency domains required that the FPGA cannot generate, a discrete high performance clock jitter cleaner or clock generator IC is needed.

In case of the example system solution shown in Figure 7, engineers have to spend a lot of time on the FPGA internal "DPLL" design. This "DPLL" in FPGA also consumes many resources in the form of configurable logic blocks and RAMs. The synchronous output clock accuracy depends on FPGA internal operating clock frequency and RAM depth.

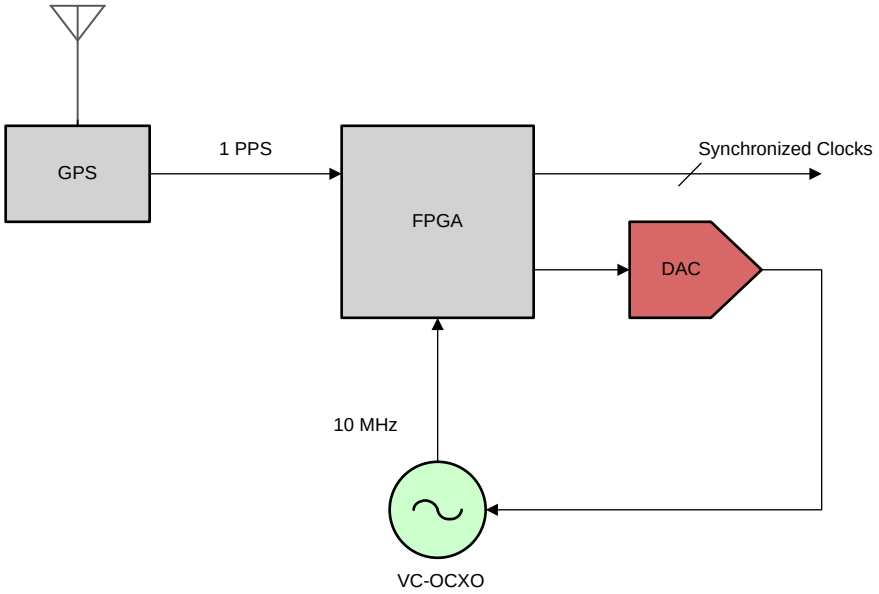


Figure 7. GPS Steered FPGA Control Loop Based Clock Generation

Within the alternate architecture using LMK05028 as shown in Figure 7, FPGA resources can be freed up for other tasks. In Figure 7, the TDC block in LMK05028 compares 1 PPS reference and feedback clock, a local 10-MHz OCXO is supplied as reference to the TCXO-DPLL to achieve superior stability in holdover, and a local 48.0048-MHz XO is provided as reference to the APLL to achieve good jitter performance for final output clocks. 8 high performance outputs from LMK05028 can help to minimize system BOM cost by consolidating clock generators and/or clock buffers. A filtered 1 PPS can be output on two clock output ports of LMK05028.

FPGA can monitor LMK05028 1 PPS synchronization status or take over synchronization by Digitally Controlled Oscillator (DCO) mode. In some systems, either local GPS or IEEE1588 through Ethernet can be a synchronization source. FPGA or CPU selects the best source from them.

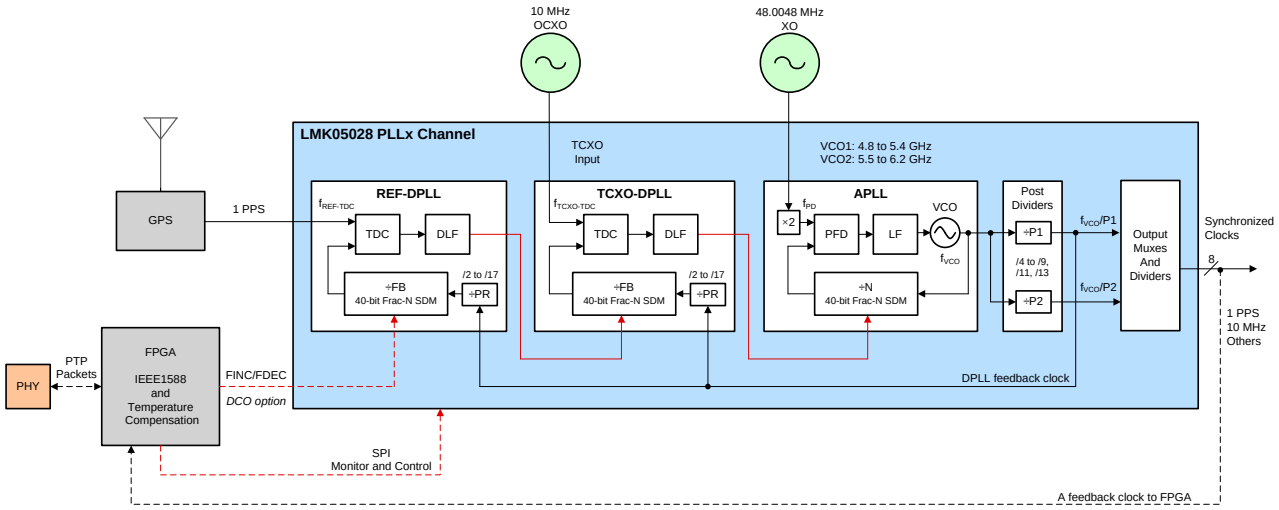


Figure 8. LMK05028 Works With GPS (Option for IEEE 1588 PTP)

2.4 Zero Delay Mode

Zero delay can be enabled to achieve a deterministic phase offset between selected output clocks and the DPLL reference input clock. This function enables the output clock to preserve the phase information from input clock. A typical use-case for this feature can be found in a Telecom Network with Timing Cards & Line Cards. The DPLLs in the Line Cards can be configured in Zero Delay Mode thereby maintaining deterministic phase relationship with the reference clock from the Timing Cards.

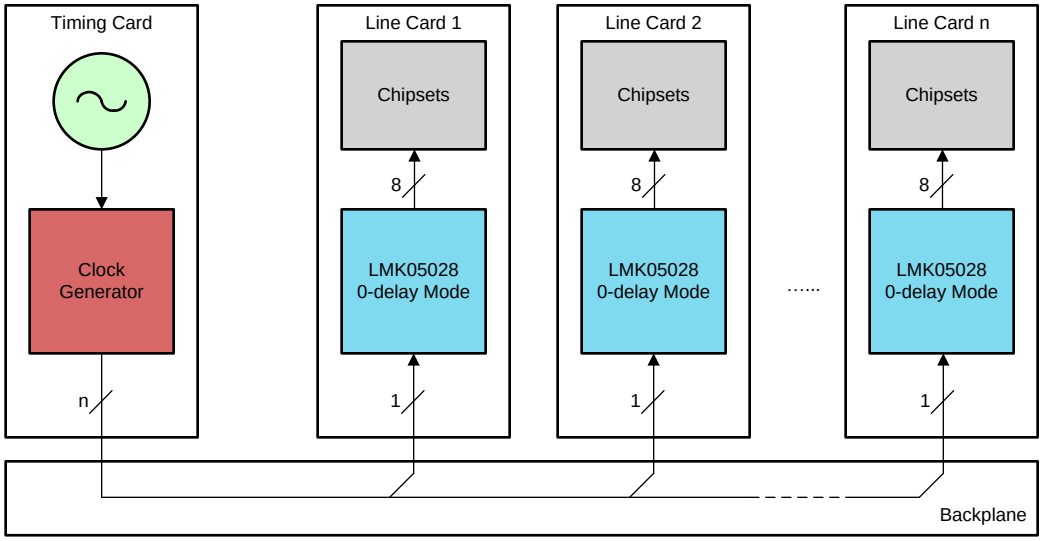


Figure 9. Zero-Delay Clock Distribution for Line Cards in Backplane Architecture

For applications that require IEEE1588 steered clocks, the LMK05028 supports Digitally Controlled Oscillator (DCO) mode. In this mode, the output clock frequency (phase) is steered with fine granularity of 1 ppt through control word from FPGA or ASIC. The control word is communicated to the device through serial I2C/SPI interface. When the LMK05028 enables DCO mode, it disables zero delay mode.

2.5 Robust Window Detector

A redundant design comprising of Master & Slave Timing Cards is typically adopted in the Timing Card & Line Card scenario described in the previous section. Redundancy ensures that a line down situation is avoided due to unanticipated failure of the Timing Card that is being used to provide reference timing to the downstream line cards. The backup Slave Timing Card ensures the role of a Master Timing Card in such scenarios to guarantee system timing. When the operational Timing Card is removed for maintenance, Line Cards should detect the missing timing pulses and make a decision to enter holdover mode or switch to a valid reference from the redundant Slave Timing Card. Additionally, Line Cards need to support live insertion, hot plugging and hot swap. These events can cause runt pulses on the reference should also be detected by the Line Cards. LMK05028 has a special design to reliably detect missing timing pulses and runt pulses events.

LMK05028 has programmable window detectors for active reference monitoring. Early or Late Edges can be detected reliably outside of a programmable window (green) thereby facilitating faster entry into Holdover or Reference Switchover. The minimum width of the valid window is ±3 × (8/VCO frequency) and the window is programmable with a resolution of 8/VCO frequency.

This window detector can support gapped clocks on reference inputs. We will talk more about gapped clock in section Section 3.3.

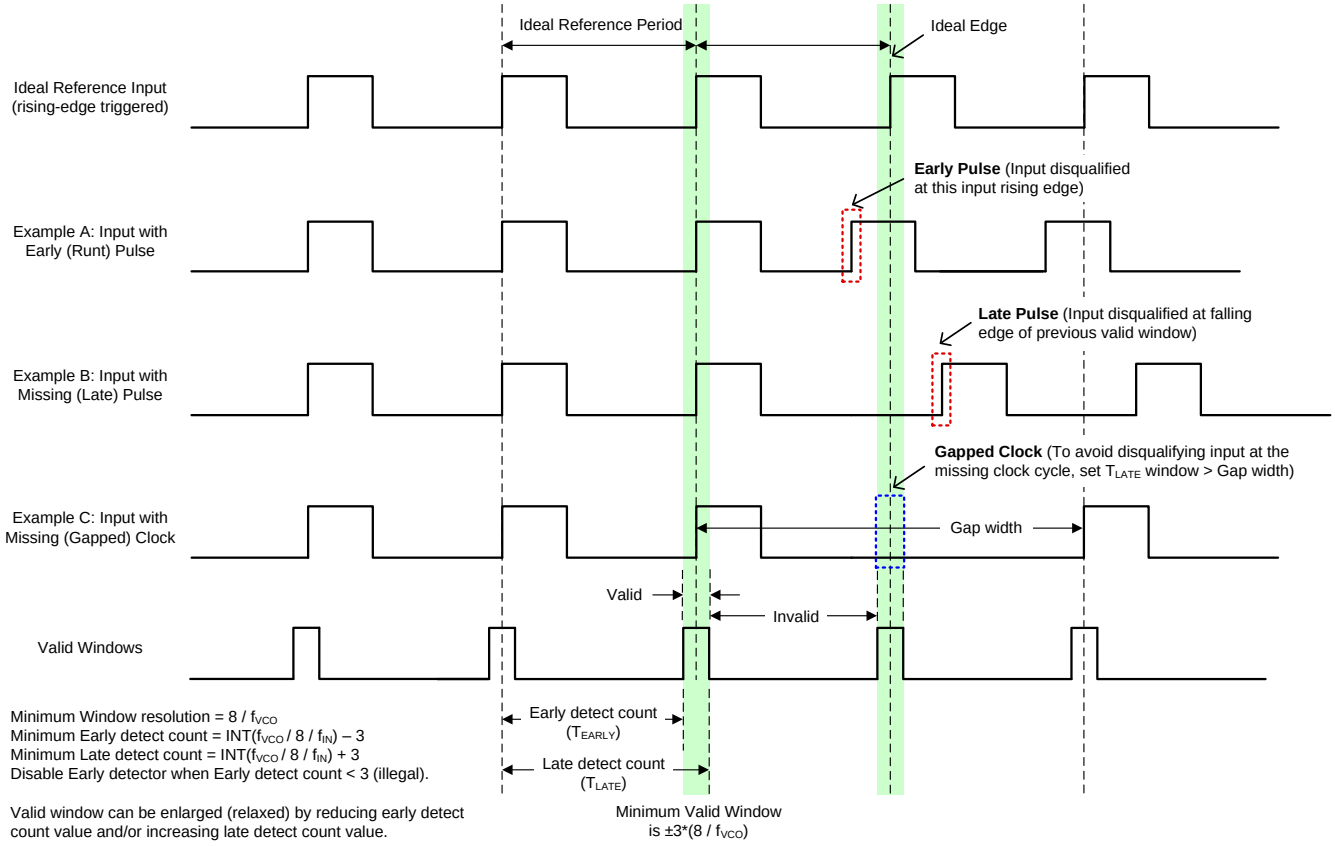


Figure 10. Window Detector Implementation in LMK05028

3 DPLL Applications

3.1 DPLLs in Wired Communications Network

In Next-Generation Networks (NGN), there are key architectural changes in telecommunication core and access networks. For telecommunication core, operators are migrating from legacy TDM (Time-Division Multiplexing) synchronous networks to a packet-based network. Ethernet-based packet networks are low-cost, reliable, scalable but inherently asynchronous. With a growing number of applications requiring both accurate time and frequency synchronization, the time error of 100 ms or more from IETF's Network Time Protocol (NTP) is not sufficient. ITU-T cooperated with IEEE to standardize Synchronous Ethernet (SyncE) for frequency synchronization. IEEE also defined IEEE1588 Precision Time Protocol (PTP) to achieve time synchronization in packet networks. New Ethernet switches or routers in wired communications or data communications support both SyncE and IEEE1588 to achieve nanosecond or sub-nanosecond accuracy.

The LMK05028 integrates two DPLL channels. One DPLL channel can work as a boundary clock or a slave clock in IEEE1588 synchronization hierarchy, another DPLL channel can be dedicated for SyncE, as shown in Figure 11.

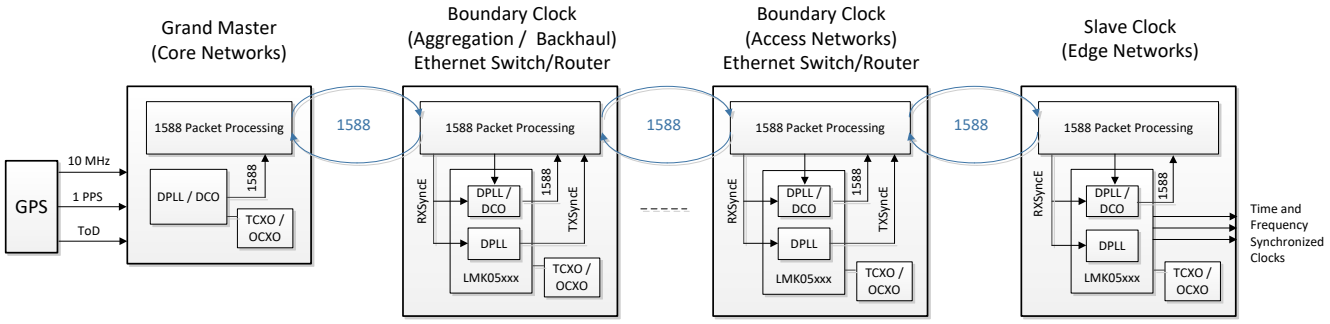


Figure 11. DPLLs in PTP Networks

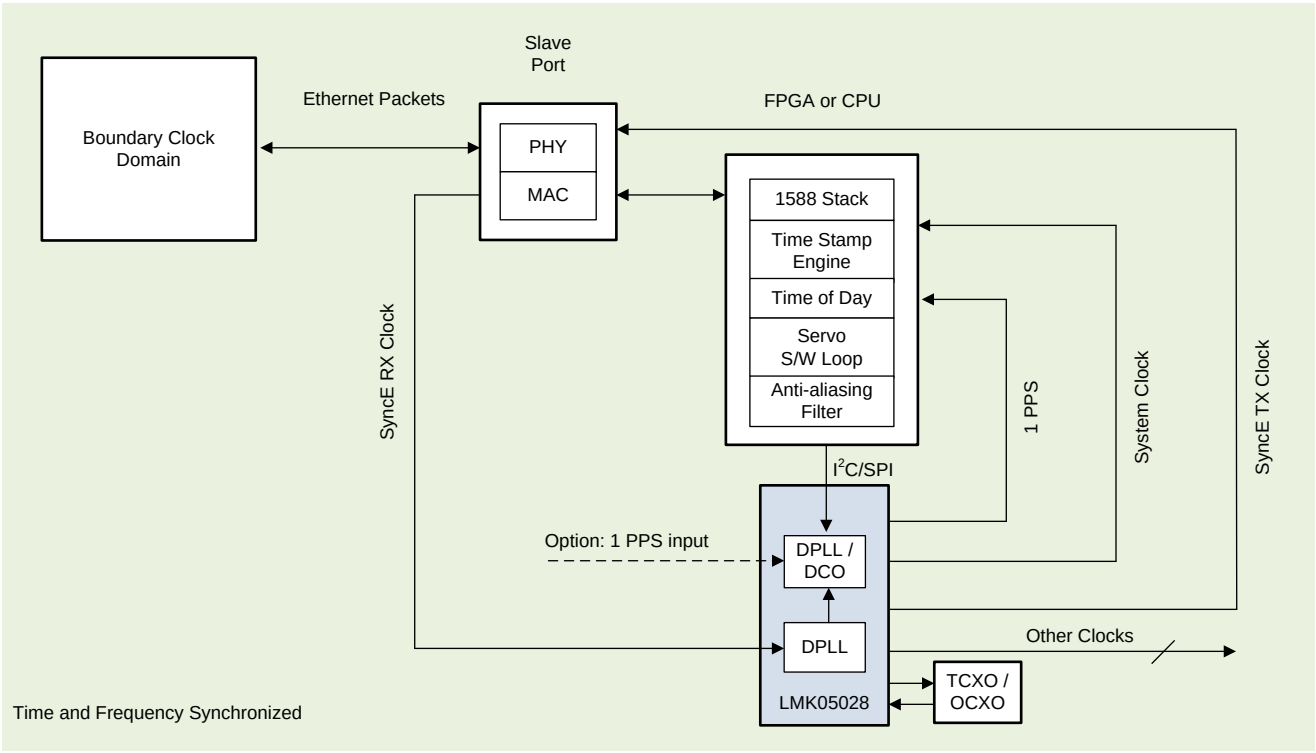


Figure 12. LMK05028 Works as a Slave Clock

In Ethernet switches and routers, at lower hierarchy of the communication networks, more and more optical access networks (PON), wired access networks (DSLAM) and cable access networks (CMTS) use DPLLs. DPLLs are also adopted in OTN at higher hierarchy of the telecommunication core networks. Section 3.3 discusses DPLLs in OTN.

3.2 DPLLs in Wireless Communications Network

DPLL opportunities emerge more and more in wireless communication applications. With wireless communication core network evolution, as an access unit, BBUs (Baseband Unit) adopt DPLLs to implement SyncE and IEEE1588.

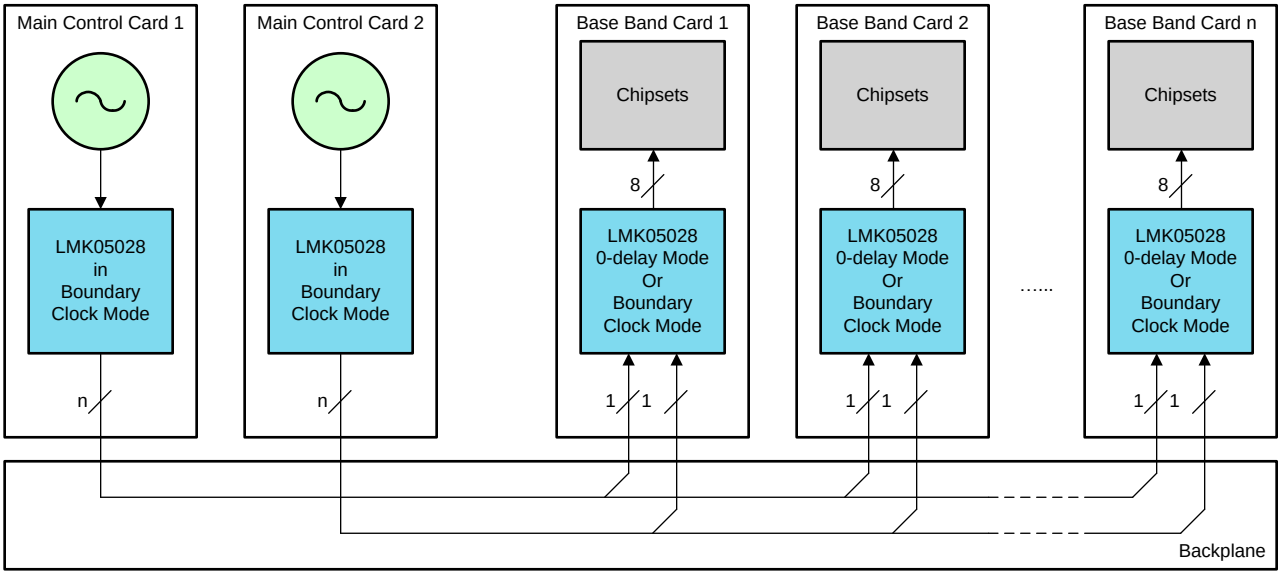


Figure 13. DPLLs in a BBU

For the interface between RRU (Remote Radio Unit, or Remote Radio Head) and BBU, the new eCPRI specification is under consideration. The eCPRI specification will support the 5G Front-haul and will provide enhancements to meet the increased requirements of 5G. RRUs will recover the synchronization and timing from the link with BBUs, and the air interface of the RRU shall meet the 3GPP synchronization and timing requirements. PTP and SyncE are suggested in the synchronization plane of eCPRI. TI is closely tracking technologies and standards for 5G wireless communication, and new DPLLs optimized for 5G are under development.

3.3 DPLLs in OTN

An Optical Transport Network (OTN) is composed of a set of Optical Network Elements connected by optical fiber links, able to provide functionality of transport, multiplexing, routing, management, supervision, and survivability of optical channels carrying client signals, according to the requirements given in Recommendation ITU-T G.872. OTN can carry different client signals for a wide array of services, such as synchronous SDH, asynchronous Ethernet, Fiber Channel, CPRI, Video, and so forth. Transponders and Muxponders convert different client signals to line side rate signals. Figure 14 below highlights a case of an OTN transponder mapping between 100GbE (Client) and OTU4 (Line) rates.

Because OTN adopts digital wrapper technology, the data rates on Line side (OTU-n) are typically higher than Client side. As an example, OTU4 data rate including FEC is 155.52 × 16 × 40 × 255／227 Mbps (approximately 112 Gbps after rounding). The 100GbE data rate is 103.125 Gbps. Figure 14 below lists recommended reference clock frequencies for 100GbE and OTU4. LMK05028 has dual DPLL channels to support multiple rate conversions simultaneously between the Line and Client side.

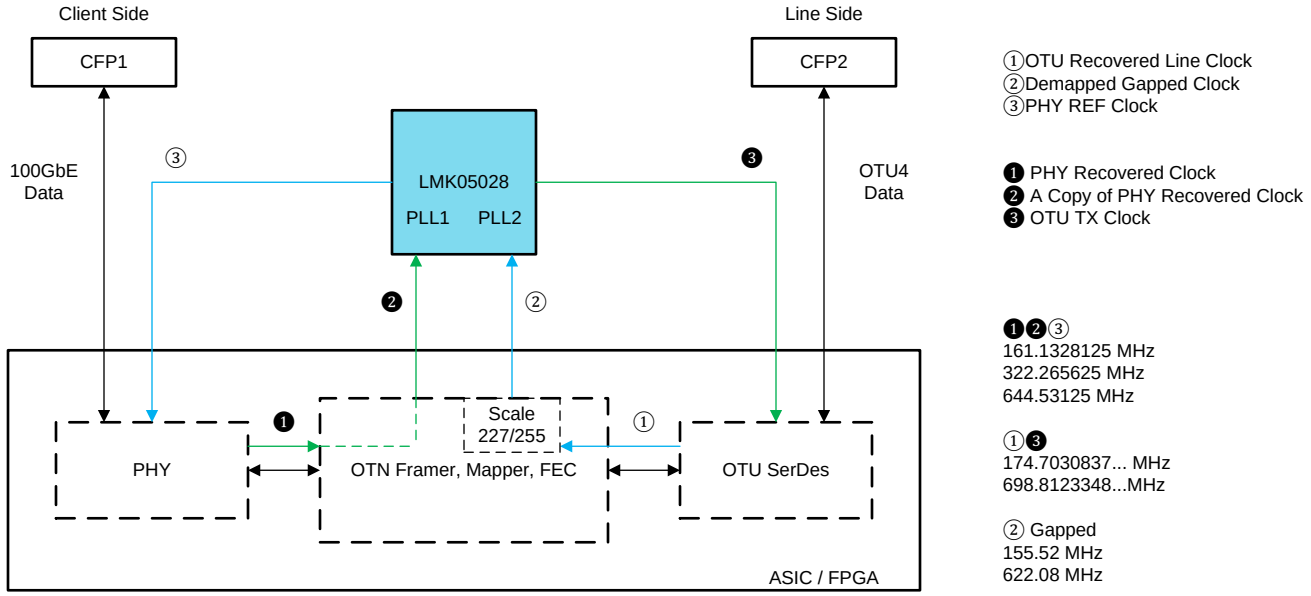


Figure 14. LMK05028 in 100G OTN Transponder

OTN can convert line rate with client rate with adding or deleting clock gaps. Figure 15 shows an example converts OTU4 line rate clock to client clocks.

LMK05028 can lock to the gapped clock and output will be a periodic non-gapped clock with an average frequency of the input with its missing cycles.

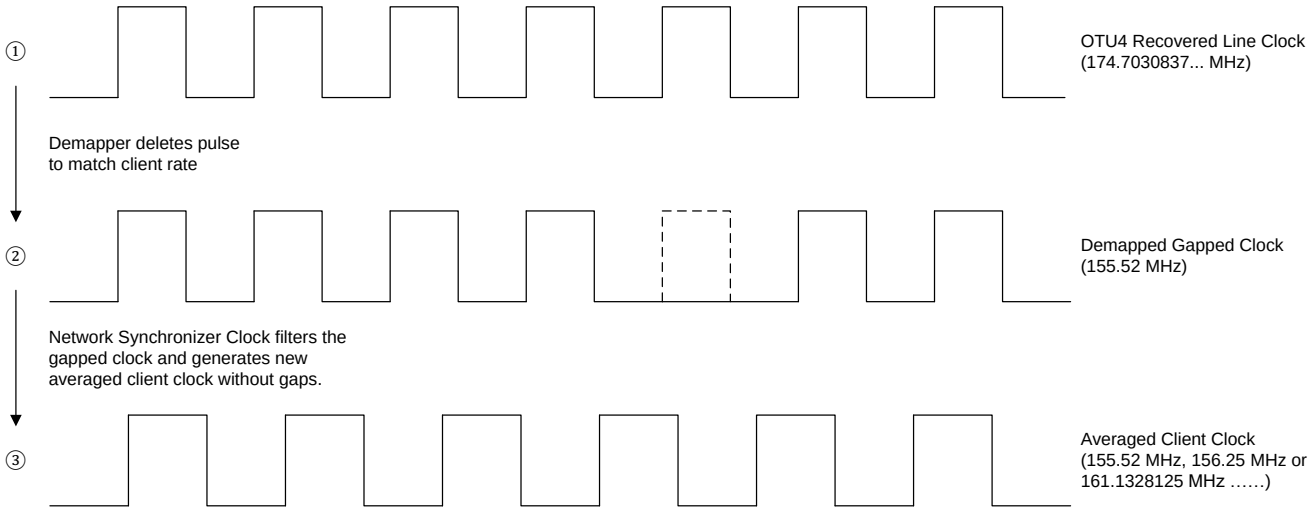


Figure 15. DPLL Averages Gapped Clocks

For the application highlighted above, the LMK05028 can generate a high-performance PHY or Serdes reference clock supporting integrated RMS Jitter less than 300 fs (12 kHz - 20 MHz).

In Muxponder applications, where there are several Clients, the LMK05028 supports reference priority selection and switchover between Line and Client side.

3.4 DPLLs in Smart Grid Infrastructure

The Smart Grid must adapt and shift from a centralized source to a distributed topology that can absorb different energy sources in a dynamic way. There is a need to track realtime energy consumption and demand to the energy supply; this goes with the deployment of more remote sensing equipment capable of measuring, monitoring and communicating energy data that can be used to implement a self-healing grid, increase the overall efficiency, and increase the level of self-monitoring and decision making. The connected smart grid provides a communication network that will connect all the different energy-related equipment of the future.

To achieve accuracy electric power data in the grid, the key element is the PMU (Phasor Measurement Unit), which measures voltage and current phasors across wide area grid with high precision using a very precise time synchronization scheme. IEEE standards association establishes IEEE Std C37.238 to use IEEE 1588™ Precision Time Protocol in power system applications.

A typical usage of LMK05028 in a Smart Grid PMU is shown in Figure 16 below.

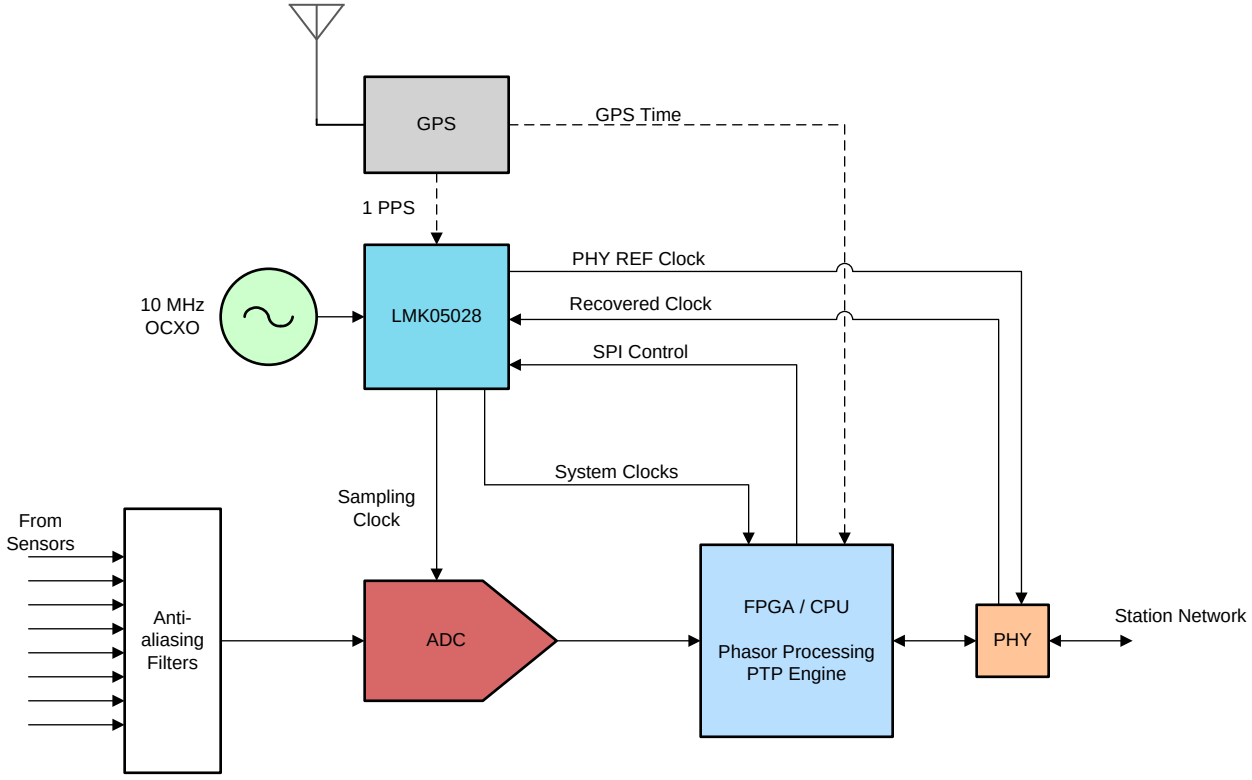


Figure 16. LMK05028 in Smart Grid PMU

3.5 DPLLs in Medical Ultrasound Imaging

DPLL also adopted in medical applications. A popular application is Medical ultrasound imaging that requires a wide range of frequencies from kHz to MHz. In most of these use-cases, a single clock domain is insufficient to meet the frequency needs of the application. LMK05028 can support two high performance clock domains and output dividers with deep divide capability making them suitable for this application segment.

In Continuous wave (CW) Doppler ultrasound application, the LMK05028 can works as a CW clock generator with tunable function. To generate the 16 phases required for CW beam forming, one method is to input a CW clock in kHz or MHz and a 16x (or 8x, 4x) CW clock for phase generator. The LMK05028 has fractional PLLs and deep dividers, can flexibly generate and tune the CW clock and the 16x (or 8x, 4x) CW clock. Texas Instruments™ AFE58xxxx devices integrate the CW signal path. The application notes *Understanding CW Mode for Ultrasound AFE Devices* (SLAS253) describes details about CW mode in Ultrasound AFE devices.

Figure 17 is an example for LMK05028 in medical ultrasound imaging.

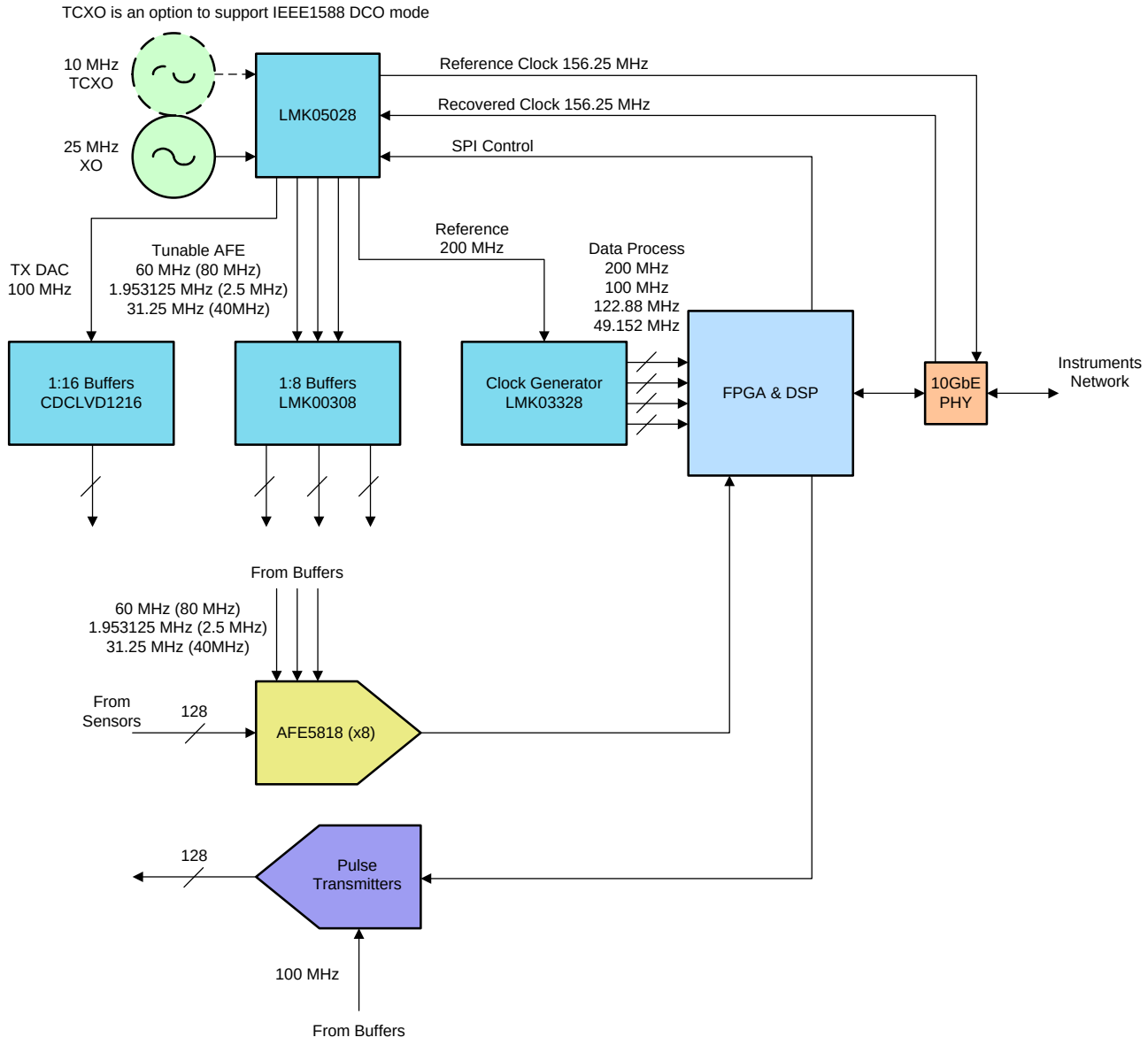


Figure 17. LMK05028 in Medical Ultrasound Imaging

The LMK05028 can run in DCO mode to support IEEE 1588 for medical equipment interconnection. ISO/IEEE 11073 sets the standards for how medical equipment communicate. One goal is to process the data from multiple equipment in real time, especially for the vital signs information. IEEE 1588 can achieve microsecond to sub-microsecond accuracy. This topic is beyond the scope of this report, but we can monitor the trend.

3.6 DPLLs in Broadcast Video

LMK05028 can support two categories of broadcast video clocking applications, namely Genlock and video processing.

Genlock stands for generator locking, and is used to synchronize equipment in a professional broadcast studio. Master sync generator or Master Clock Reference Generator distributes video reference signals to all equipment that need Genlock, including cameras, video switchers, video servers, frame synchronizers, and so on.

When there is an asynchronous video source entering a studio, the Frame Synchronizer can synchronize the timing of the video source signal to coincide with a central timing reference from Genlock. See Figure 18 below for a typical block diagram of a Frame Synchronizer.

With LMK05028, this Frame Synchronizer supports up to three interfaces to accept suitable reference signals. The first one is the common port for traditional analog video reference signal or sync signal input, connected to a Sync Separator LMH1981. The second one is a port for GPS 1-PPS input. The third one is I2C or SPI interface to accept control instructions from IEEE1588 PTP master. The Frame Synchronizer can synchronize SDI signals to any one reference from above mentioned interfaces. If the application do not need support 1-PPS or PTP, LMK05028 can also function as a clock generator similar to LMH1983 or LMK03328.

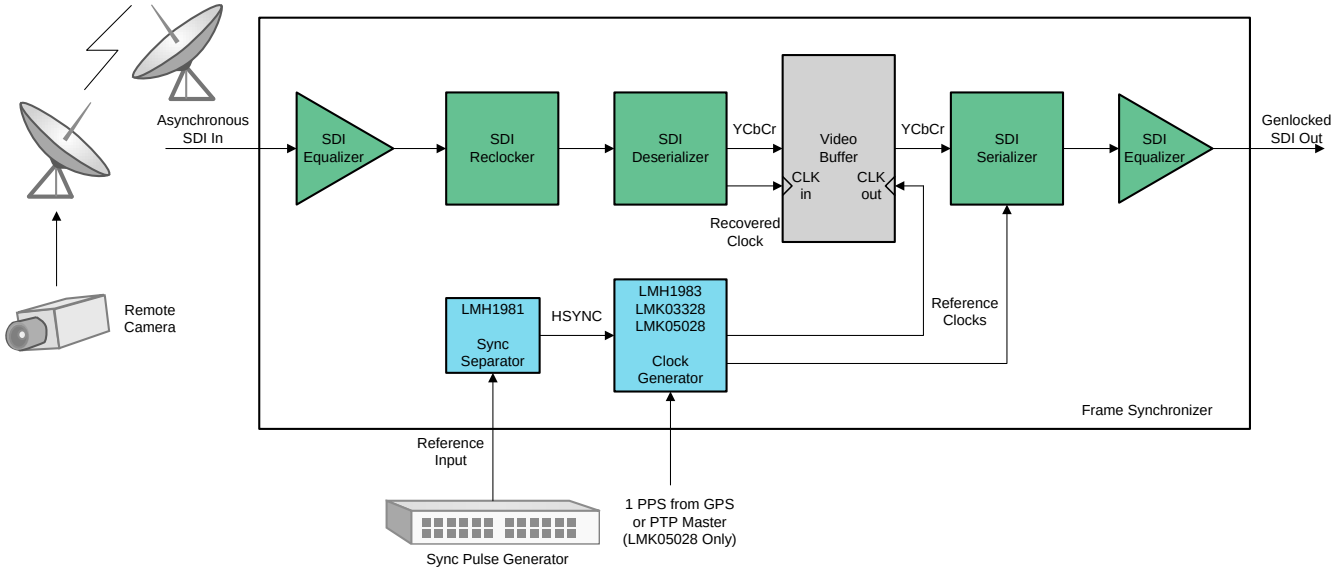


Figure 18. LMK05028 in Frame Synchronizer

LMK05028 can operate as a jitter attenuator or clock gen to simultaneously generate two high performance output clock domains. For example, PLL1 can generate 27-MHz and 148.5-MHz (or 297-MHz) video clocks, PLL2 can generate another domain, which can be 148.5/1.001-MHz (or 297/1.001-MHz) video clocks or a 24.576-MHz audio clock.

Both domains could be locked to HSYNC video pulses recovered from TI's LMH1981 sync separator chip or recovered video clock from SDI receiver or De-Serializer. Gapped clock support is necessary for locking. The DPLL Loop BW will be less than 3 Hz to provide jitter attenuation above 10-Hz timing jitter bandwidth for 12G-SDI video standard. The DPLL in 2 loop mode is sufficient for this case with a low-cost XO/TCXO reference to the APLL.

The solution highlighted in Figure 19 below can be used for 12G-SDI video applications, and is backwards compatible with traditional SD-SDI, HD-SDI, 3G-SDI, and 6G-SDI.

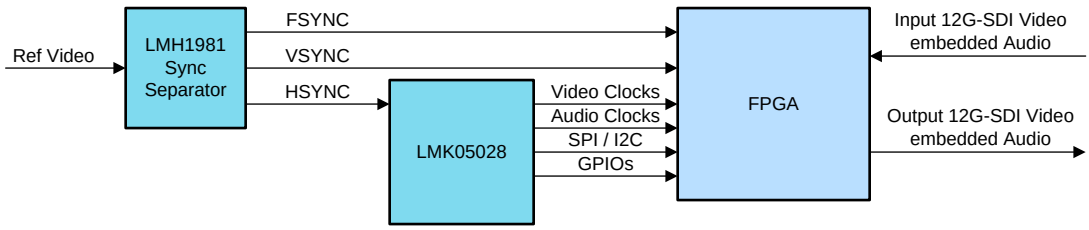


Figure 19. A Clock Solution for 12G-SDI Video Processing

4 Summary

As a high-performance clock generator, jitter cleaner, and clock synchronizer, LMK05028 has some differentiated features that bring value to new designs.

- This device shows superior hitless switching performance with patented phase cancellation technique.
- The unique 3-loop architecture leverages the advantages from each loop to achieve the optimal balance of jitter, stability, and cost.
- The 1 PPS phase locking feature offloads the FPGA resource, simplifying system design.
- The zero delay mode achieves deterministic delay from reference clock input to clock output, which is essential for those phase-sensitive systems.
- The special window detector circuit can detect missing reference input timing pulses and runt pulses, which could be caused by live insertion or hot-swap of the PC board, allowing robust system operation during intermittent input conditions.

Remember that the LMK05028 device is not limited to communications, but can also be used in many industrial applications like smart grids, medical imaging, broadcast video, and so on. The number of applications that demand the performance and flexibility offered by TI's high performance LMK05028 DPLL is growing.

5 References

1. *LMK05028 Low-Jitter Dual-Channel Network Synchronizer Clock With EEPROM* (SNAS724)
2. *Clock Conditioner Owner's Manual* (SNAA103)
3. eCPRI Specification V1.1 (2018-01-10)
4. ITU-T G.872 (01/2017

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265