Application Report
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Using the LMK0480x/LMK04906 for Hitless Switching and Holdover

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ABSTRACT

This application report discusses some of the key performance results when using LMK0480x/LMK04906 to implement hitless switching between reference clocks. Hitless Switching is required in certain applications such as SONET/SDH/line port cards and routers/switchers in order to minimize the propagation of phase transients to the clock outputs during reference clock switching. On loss of all valid reference clocks, LMK0480x/LMK04906 will switch into a programmable holdover state to preserve the frequency of the output clocks. Holdover specifications highly depend on the reference Crystal, VCXO, VC-OCXO, VC-TCXO chosen as holdover reference input to the LMK device. Depending on the requirements of the end application, selection of this reference clock may vary. Some control from the host processor may be required to exit holdover in a deterministic way.

One of the growing application areas where the LMK0480x/LMK04906 device could potentially be used is in Synchronous Ethernet (SyncE) line cards. With the Telecommunication networks evolving from circuit-switched based networks to packet-switching based networks, Synchronous Ethernet networks are now more than ever being introduced in the wireless base station backhaul. Given the synchronization requirement of base station for cell networks, SyncE networks must enable the transport of frequency synchronization, support hitless reference clock switchover and meet tight holdover stability specifications. The phase noise requirement on the output clocks is also quite stringent.

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1 Synchronous Ethernet Clock Network

A typical application block diagram of a Synchronous Ethernet clock network is shown in Figure 1.

There are two redundant timing cards that act as the reference frequency source for multiple line cards. The timing card takes external input reference timing from the network clock (SSU or BITS).The clocking devices in these timing cards are typically Digital PLLs. These SyncE network timing cards must comply with the frequency accuracy, holdover performance, noise generation, tolerance and transfer requirements per ITU-T G.8262 standard. The line cards are required to monitor the system clock and lock to either its primary or secondary reference clock inputs, and to be able to switch intelligently between the two. The main functions of the clocking devices used in line cards include frequency conversion, noise filtering and jitter attenuation. These requirements can be easily met with a high performance analog PLL, such as Texas Instruments' LMK0480x/4906 series as shown in Figure 1 below.

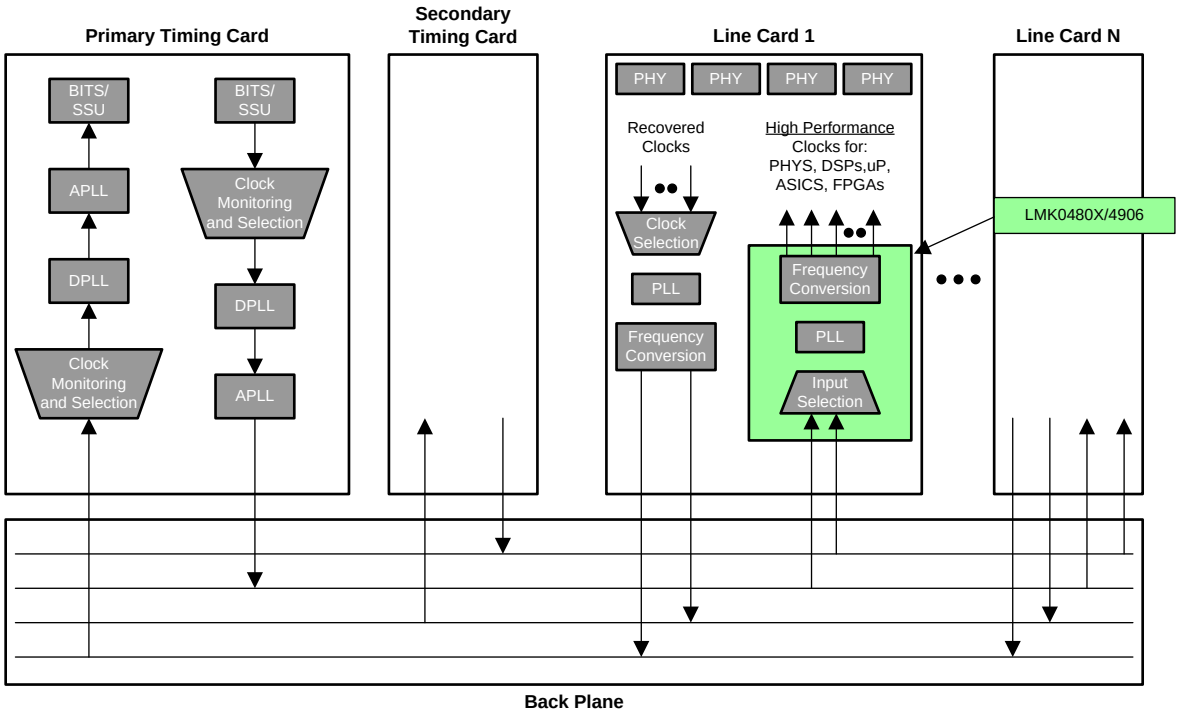

Figure 1. Synchronous Ethernet Clock Network

2 Feasibility Analysis on Applying LMK0480X/04906 in SyncE Line Card Clock Design

2.1 FREQUENCY ACCURACY

Figure 2 shows a typical block diagram of a PLL implemented with a TCXO reference.

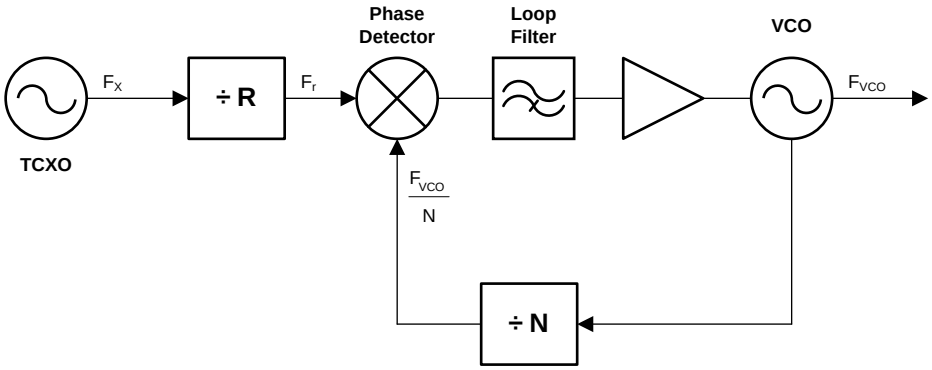

Figure 2. Typical PLL Block Diagram

When the PLL is in unlocked state (such as during initial power up or immediately after reprogramming a new value for N) the phase detector will create an error voltage based on the phase difference of the two input signals. This error voltage will change the output frequency of the VCO so that it satisfies Equation 1.

$$Fvco / N = Fx / R = Fr \quad (1)$$

As long as the system is in a locked condition the VCO will have the same frequency accuracy as the TCXO reference. If the accuracy of the reference clock is 1 part-per-million (ppm), the output frequency of the synthesizer will also be accurate to 1 ppm.

For the system topology we are discussing, the line card clock's reference input is coming from the output of digital PLL on timing cards. The BITS/SSU is typically a Stratum 2 compliant source with accuracy up to 16ppb, so the same frequency accuracy propagates through to the line card clock's output.

2.1.1 Measured Result

Figure 3 shows the measured result for the LMK04906. The frequency accuracy of the 156.25 MHz clock output was within +/- 250 mHz during phase lock, which is +/- 1.6 ppb, as shown in Figure 3.

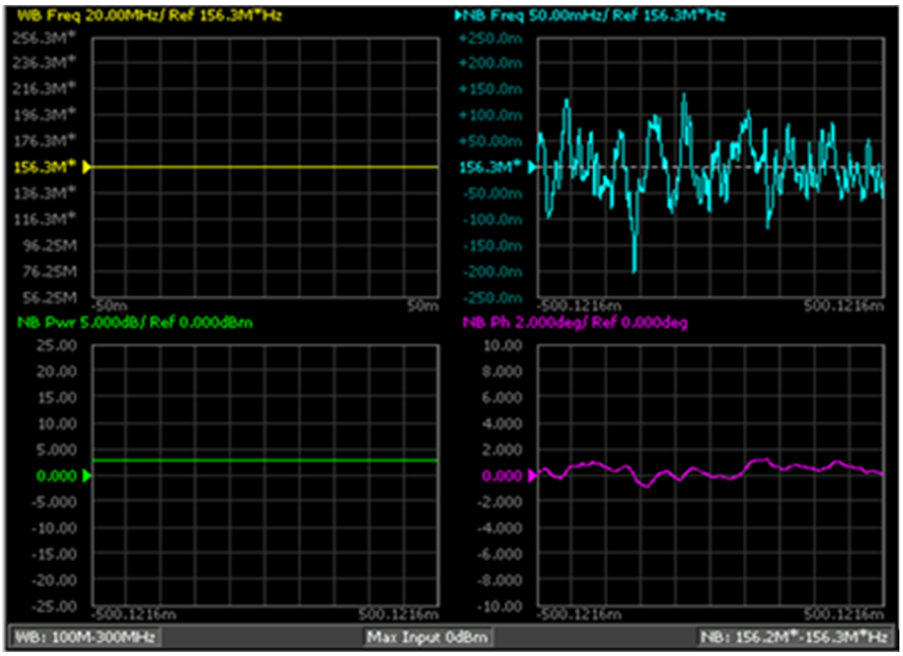

Figure 3. LMK04906 Frequency Accuracy During Lock

2.2 JITTER

LMK0480x/4906 employs a dual loop architecture which consists of two high-performance phase-locked loops (PLL), a low-noise crystal oscillator circuit, and a high-performance voltage controlled oscillator (VCO), as shown in Figure 4.

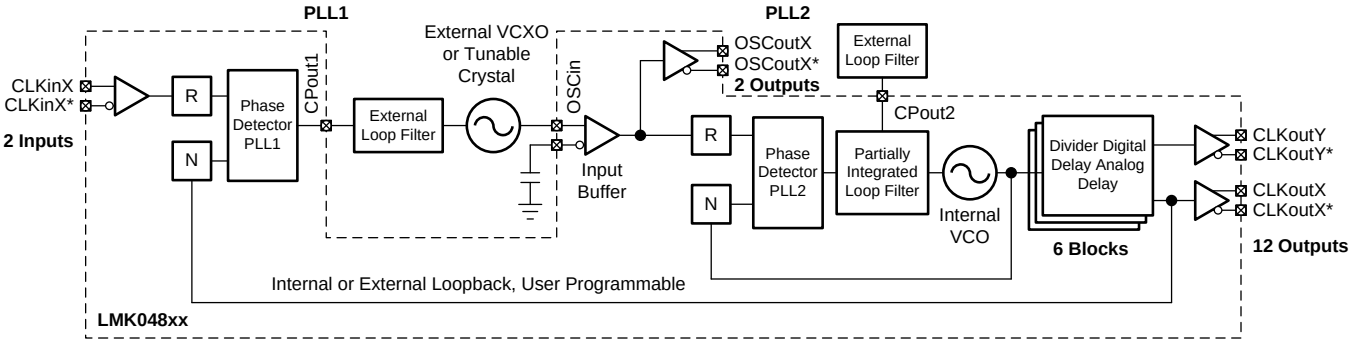

Figure 4. LMK0480x/4906 Cascaded PLL Architecture

The first PLL (PLL1) provides a low-noise jitter cleaner function while the second PLL (PLL2) performs the clock generation. PLL1 can be configured to either work with an external VCXO module or the integrated crystal oscillator with an external tunable crystal and varactor diodes. When used with a very narrow loop bandwidth, PLL1 uses the superior close-in phase noise (offsets below 50 kHz) of the VCXO module or the tunable crystal to clean the input clock. The output of PLL1 is used as the clean input reference to PLL2 where it locks the integrated VCO. The loop bandwidth of PLL2 can be optimized to clean the far-out phase noise (offsets above 50 kHz) where the integrated VCO outperforms the VCXO module or tunable crystal used in PLL1.

In the following paragraphs, we further illustrate and describe the phase noise transformation that takes place in the dual PLL jitter-cleaning architecture, as well as how the ultra-low jitter performance can be achieved in this architecture.

Figure 5 shows the phase noise of a reference clock that is excessively high at large offsets from the carrier frequency, and even at lower offsets. This would be unacceptable clock phase noise for the high performance SyncE application.

Using PLL1 configured with a narrow loop band width, the phase noise of the incoming reference clock is replaced by the phase noise of an external oscillator, which can be either a VCXO or inexpensive crystal. This “clean” external oscillator then becomes the reference input to PLL2. When combined with the internal low noise VCO, a high frequency, low jitter clock is generated and injected to the distribution block.

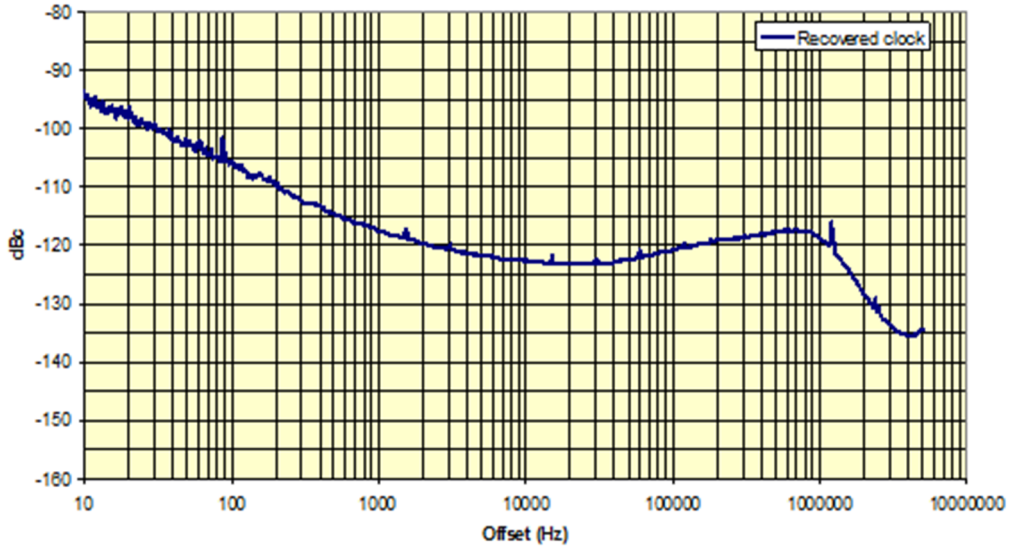

Figure 5. Phase Noise Plot of Reference Input

Figure 6 shows that when the VCO frequency is divided down to the original reference input frequency, a lower noise replica of the input clock is achieved. Note that the wideband noise of the output clock is much lower than that of the input clock.

The LMK0480x/4906 can achieve sub-150fs RMS jitter (12 kHz to 20 MHz) with a low noise VCXO, when using a DPLL output as the 1st PLL’s reference input. This meets the demanding jitter specification of SyncE.

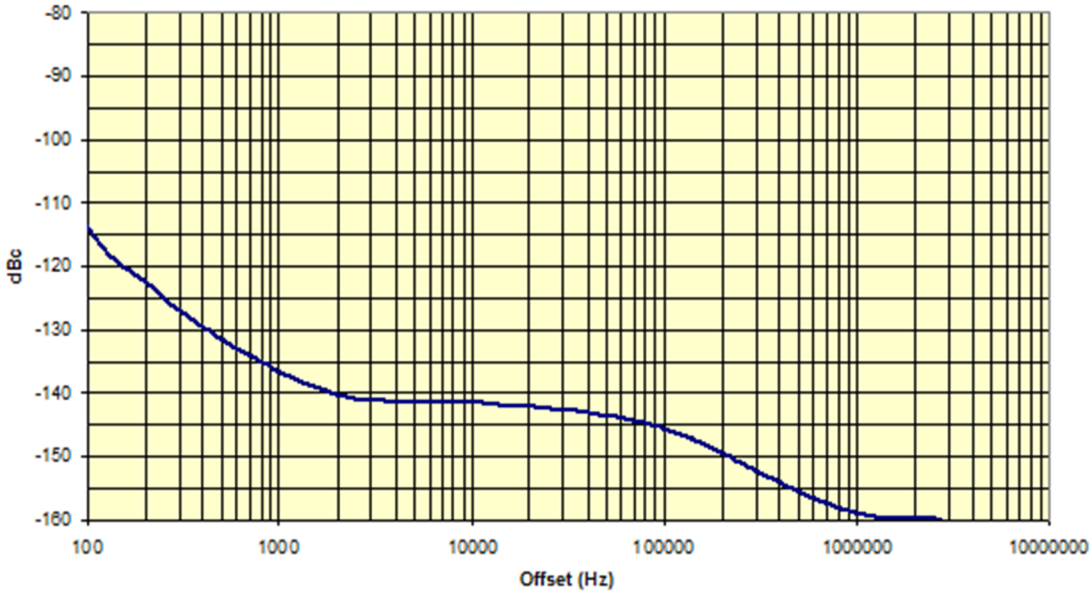

Figure 6. Phase Noise Plot of LMK0480x/4906 Output

2.2.1 Measured Result

Figure 7 shows the LMK04806 jitter is 103 fs RMS (integrated from 12 kHz to 20 MHz) with the following settings for the dual stage PLLs:

- PLL1 = 300 Hz LBW, 55 deg PM.
- PLL2 = 321 kHz LBW, 75 deg PM.

More phase noise plots can be found in the LMK04806 evaluation board instructions (SNAU076).

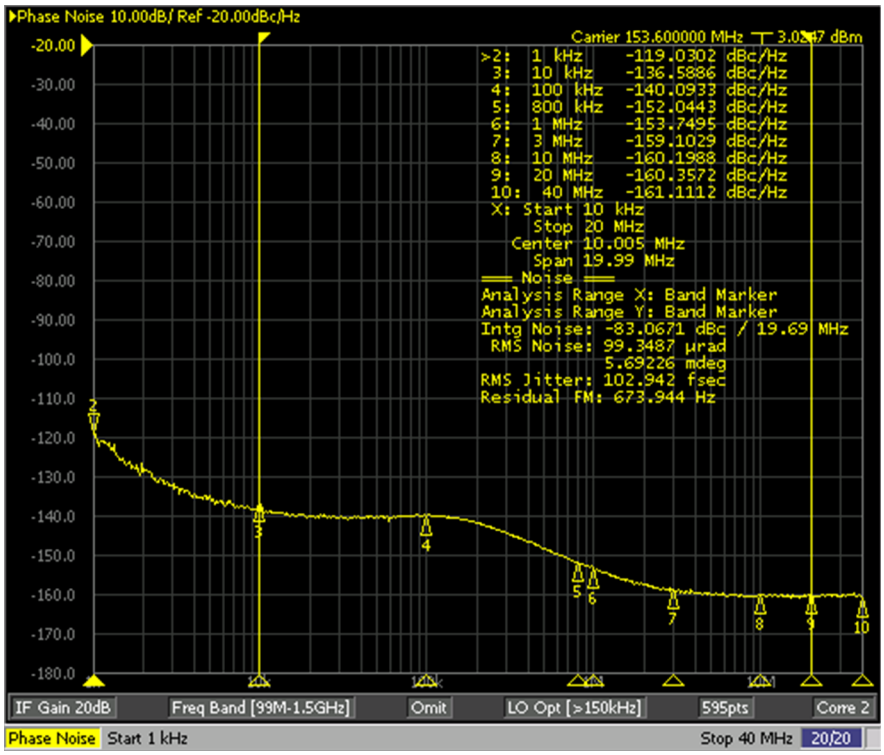

Figure 7. LMK04806 Jitter Performance

2.3 HOLDOVER

When an input clock switch event is triggered and holdover mode is enabled, the clock device will enter holdover mode and remain in holdover until a holdover exit condition is met.

For traditional analog PLLs, the typical way to implement holdover on loss of reference clocks is to toggle the VCO's tuning voltage to a fixed value, such as Vcc/2. The limitation of this approach is that the power supply noise could potentially find its way into the device and vary the VCO tuning voltage, thereby affecting the stability of the output clock during holdover. One of the advantages of LMK0480x/LMK04906 series is that they offer multiple holdover modes. The user may configure these devices to either use a fixed tuning voltage during holdover, or to use the last measured tuning voltage value prior to loss of reference (Tracking mode). This capability is enabled by a high precision built-in DAC. When the reference is lost or switching between the references, the DAC is used to set and hold the tuning voltage on the external oscillator.

When in holdover mode PLL1 will run in open loop and the DAC will set the CPout1 voltage. If **Tracked** CPout1 mode is used, the tuning voltage is monitored on a periodic basis. When holdover is entered, the output of the DAC will be the voltage at the CPout1 pin before holdover mode was entered. When using **non-Tracked** mode (EN_MAN_DAC = 1), during holdover the DAC value is loaded with the programmed value into one of the internal registers (MAN_DAC); the tracked value is not used.

When in Tracked CPout1 mode the DAC has a worst case tracking error of ±2 LSBs once the PLL1 tuning voltage is acquired. The step size is approximately 3.2 mV/bit, therefore the VCXO frequency error during holdover mode caused by the DAC tracking accuracy is ±6.4 mV * Kv, where Kv is the tuning sensitivity of the VCXO in use. Therefore the accuracy of the system when in holdover mode in ppm is [5]:

$$\text{Holdover Accuracy (ppm)} = \frac{\pm 6.4\ \text{mV} * \text{Kv} * 1e6}{\text{VCXO Frequency}} \quad (2)$$

For example, a system with a 25 MHz clock input, and a 25 MHz VCXO with a Kv of 4.5 kHz/V, will have a holdover accuracy of:

$$\pm 1.15\ \text{ppm} = \pm 6.4\ \text{mV} * 4.5\ \text{kHz/V} * 1e6 / 25\ \text{MHz} \quad (3)$$

The LMK0480x/4906 can also be configured to gracefully exit the holdover state after a valid external reference clock is restored, resulting in glitch-free operation of the output clocks.

In summary, LMK0480x/4906's holdover feature provides the possibility to achieve frequency stability and maintain integrity of the system even during disruptions in the reference input.

2.3.1 Measured Result

Figure 8 shows that upon entering holdover, a small ppm error occurs.

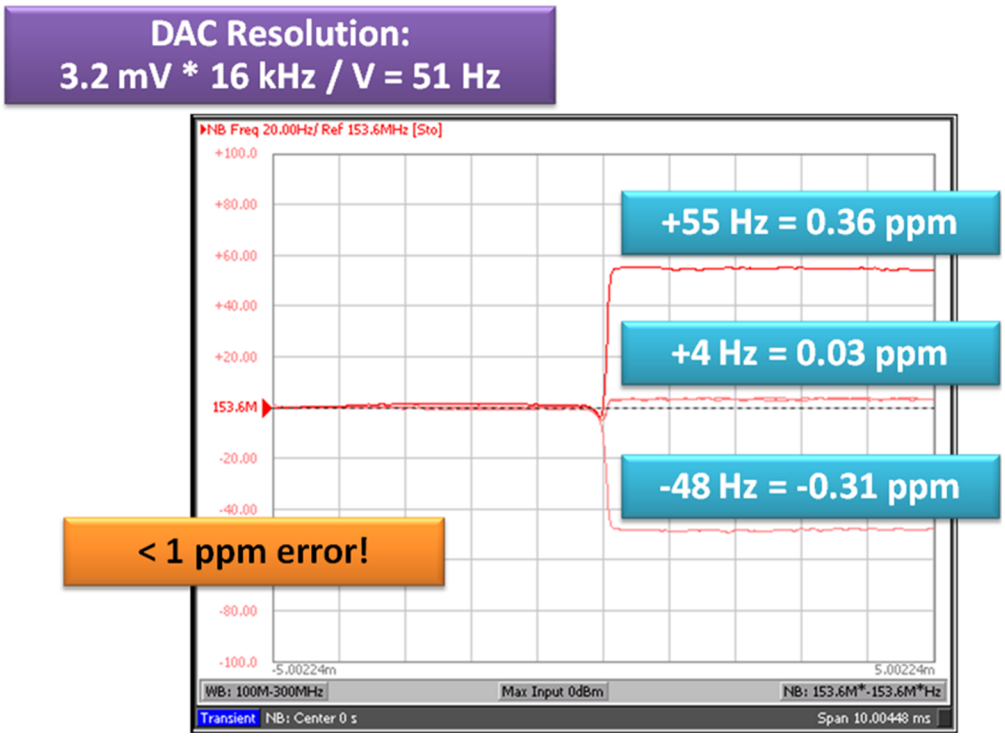

Figure 8. Entering Holdover Using TCO-2111-153.6 MHz VCXO Kvco = ~16 kHz/V

Figure 9 shows that upon exiting holdover, only a small frequency glitch occurs. This glitch can be minimized by reducing the size of the PLL1 phase detector error window (PLL1_WND_SIZE).

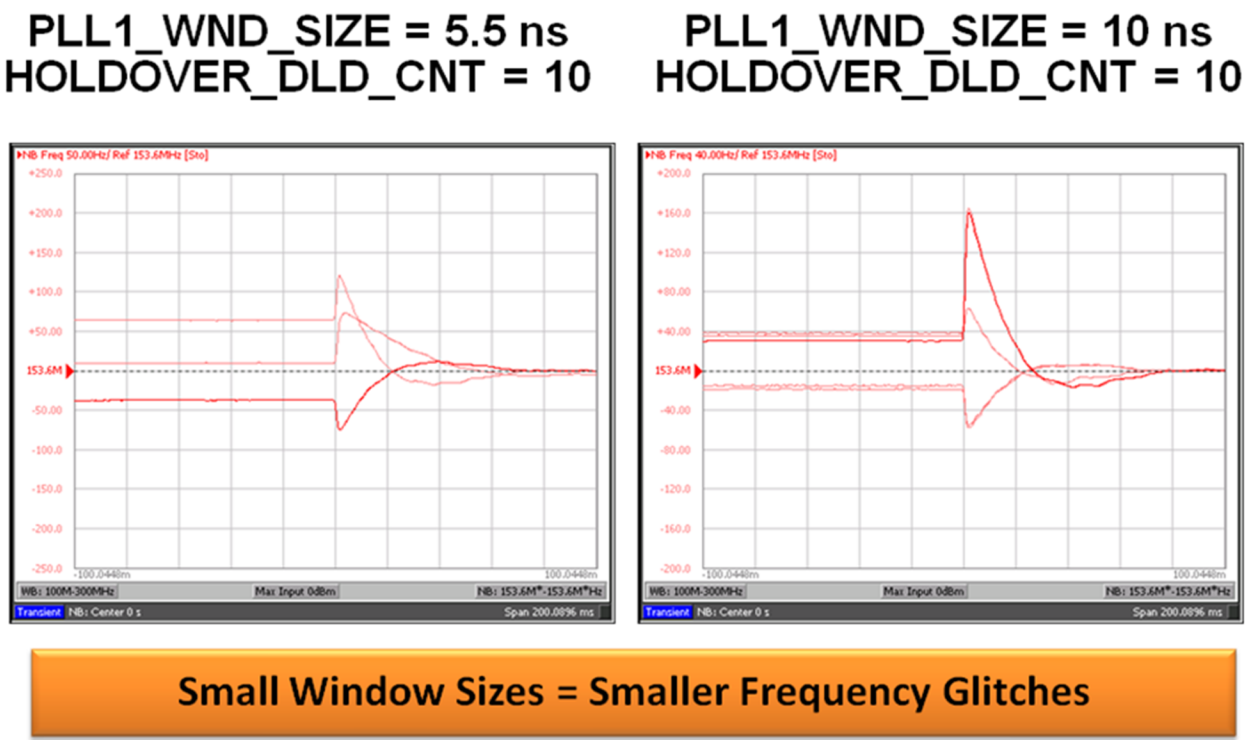

Figure 9. Exiting Holdover Using Automatic Exit

2.3.1.1 AUTOMATIC EXIT OF HOLDOVER

The LMK048xx device can be programmed to automatically exit holdover mode when the accuracy of the frequency on the active clock input achieves a specified accuracy. The programmable variables include PLL1_WND_SIZE and DLD_HOLD_CNT.

The **DIGITAL LOCK DETECT FREQUENCY ACCURACY** section of the LMK04800 datasheet (SNAS489) indicates how to calculate the register values to cause holdover to automatically exit upon reference signal recovery to within a user specified ppm error of the holdover frequency. It is possible for the time to exit holdover to vary because the condition for automatic holdover exit is for the reference and feedback signals to have a time/phase error less than a programmable value. Because it is possible for two clock signals to be very close in frequency but not close in phase, it may take a long time for the phases of the clocks to align themselves within the allowable time/phase error before holdover exits.

Use of automatic holdover exit relies upon the natural phase drift between the VCXO and incoming reference clock. A deterministic exit from holdover condition cannot be ensured without intervention from the host controller to select the desired backup clock and disable holdover mode. Holdover mode can be re-enabled later.

Because using the host controller would interrupt the natural hitless recovery, using the host controller to shorten holdover time results in a phase hit to the output clock.

2.3.1.2 LONG TERM HOLDOVER STABILITY

For long term holdover stability, the temperature drift of the holdover oscillator must be taken into account.

2.4 HITLESS SWITCHING

2.4.1 Switching Mode

Both Manual and Automatic reference clock hitless switching is possible using the LMK0480x/4906 devices. This greatly minimizes the phase transient propagation to the output on loss of primary reference clock. The PLL loop bandwidth, lock time and frequency accuracy achieved upon switching over to the new source are all reconfigurable in these devices. This allows the customer to have some control over the initial phase slew rate upon loss of current active reference clock and also the maximum time interval error (MTIE) associated with the switchover.

For the automatic switching mode, LMK0480x/4906 device will detect the presence of the reference clocks through its PLL1 DLD signal and automatically switch to the active clock input port. This is illustrated in Figure 10. The figure shows the active clock is selected in priority order of enabled clock inputs starting upon an input clock switch event. The priority order of the clocks is CLKin0 → CLKin1 → CLKin0, etc.

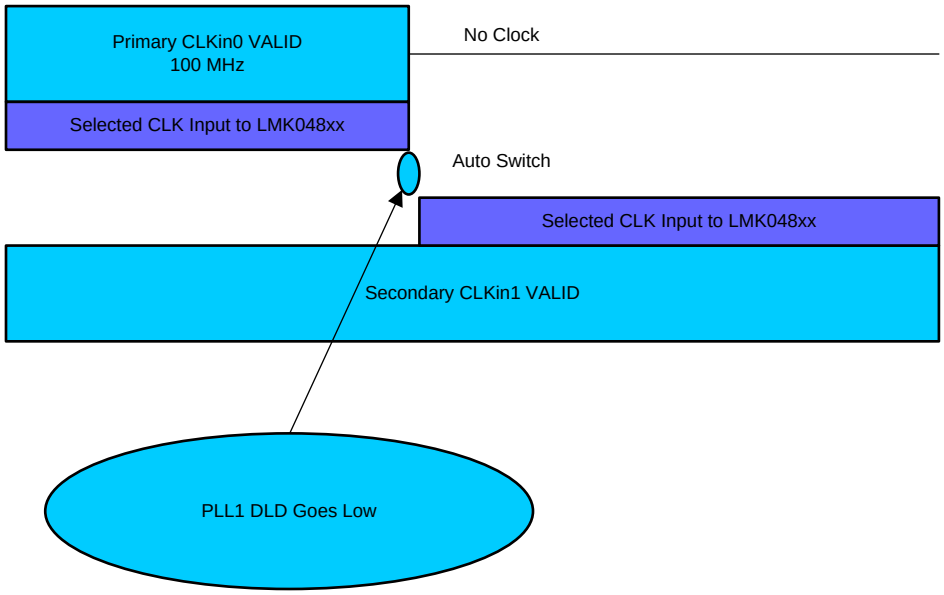

Figure 10. Automatic Switching Scenario

While in most application scenarios, manual switching mode is employed, in this case, the line card reference clock's switching is controlled by the clock IC through the hardware pin, as shown in Figure 11. This can be implemented using the DLD pin or other signal from the timing card. This implementation approach provides best synchronization between line card and timing card, as well as the fastest switching speed of the reference inputs.

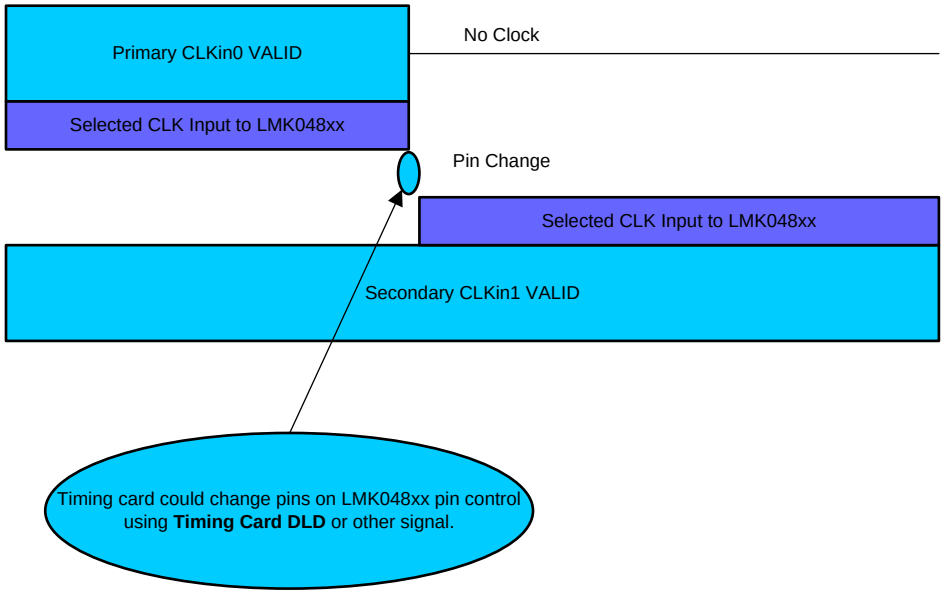

Figure 11. Manual Switching Scenario

In some applications, like OTN/SDH, it is possible that both of the reference inputs from the timing card are lost simultaneously, therefore, holdover of the line card clock needs to be involved. As indicated in Equation 2, the holdover accuracy mainly depends on the VCXO's tuning sensitivity. For an OTN/SDH application, this spec is 20ppm and therefore can be easily met by using a VCXO.

2.4.2 Phase Transients

For LMK0480x/LMK04906 family, the lock time is dependent upon PLL1 loop filter design; both the bandwidth and phase margin can impact lock-time. The time at which PLL1 DLD (digital lock detect) asserts depends upon programming of PLL1_WND_SIZE and PLL1_DLD_CNT. Depending on this programming, PLL1 DLD may assert before desired PPM accuracy of output is achieved. It is also possible that frequency could be within desired PPM tolerance and the PLL1_DLD_CNT will not have been met, thus PLL1 DLD will occur long after the signal is within desired tolerance.

Because the phase between the new reference and VCXO clock is unknown, different lock-times will be observed because the effective starting frequency is not known. The distribution of the initial time error between the VCXO and the new reference is expected to be a uniform distribution.

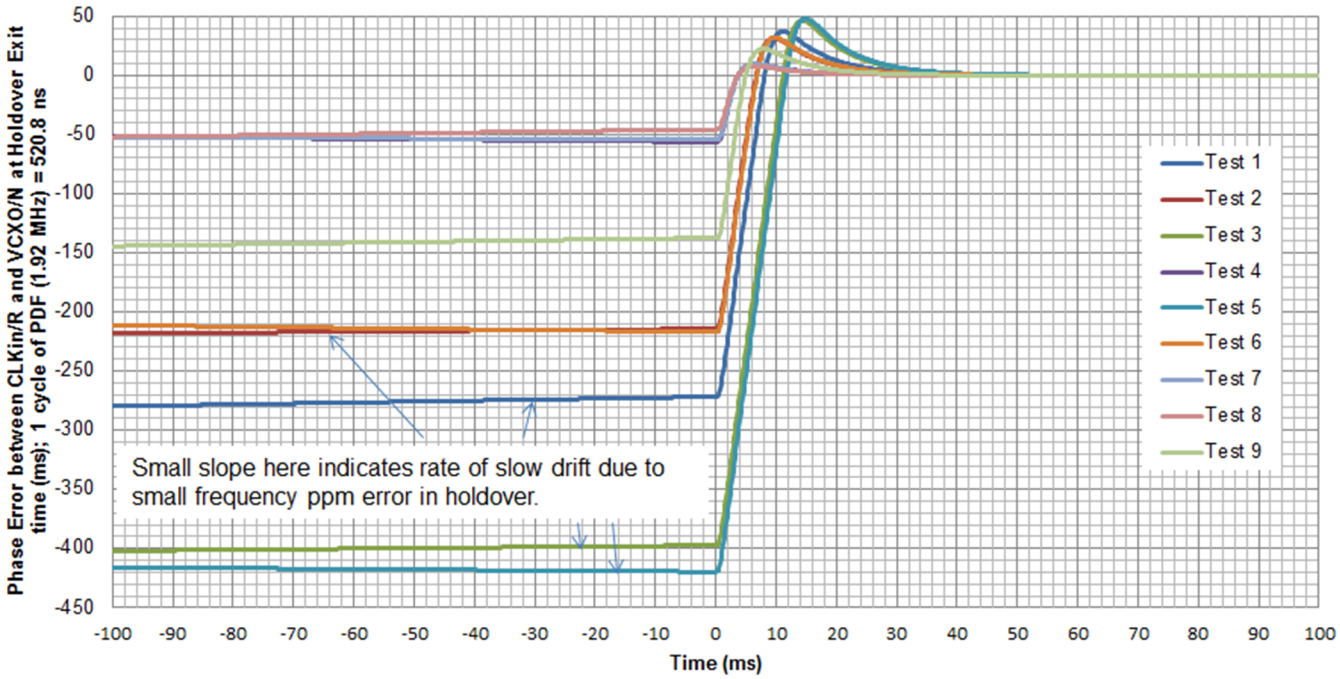

Figure 12. Phase Error Between CLKin/R and VCXO/N at Holdover Exit

Figure 12 shows the lock time using a 3rd order filter, 50 Hz closed loop bandwidth, 60 degree phase margin, and 1.92 MHz PDF (phase detector frequency). The various tests from 1~9 represent the various random phases as the starting point for re-locking PLL1. They will be within one PDF period, ~520.8 ns in this example. Doubling the PDF to 3.84 MHz reduces start max phase error to ~260.4 ns.

In summary, the theoretical maximum phase error is one period of phase detector frequency, that is, 1920 kHz corresponds to ~520.8 ns phase error. Lock time increases as phase error increases at holdover exit. Generally, when forcing holdover exit, the following factors will decrease the lock time, as well as the resulting phase error:

- Higher phase detector frequency
- Wider loop filter bandwidth
- Optimum loop filter phase margin
- Wider frequency tolerance for re-lock.

3 Conclusion

This application note has discussed the feasibility to apply LMK0480x/LMK04906 in the applications requiring hitless switching between reference clocks with programmable holdover; both theoretical analysis and actual measurement results have been presented in terms of frequency accuracy, jitter, holdover and hitless switching respectively.

Providing superior jitter performance while meeting the hitless switching requirement, the LMK0480x/04906 devices can potentially be employed as a high performance, low cost clock solution in SONET/SDH/Optical and SyncE line card applications.

4 References

1. International Telecommunication Union; ITU-T Recommendation G.803: Architecture of transport networks based on the synchronous digital hierarchy (SDH); Geneva, Switzerland; March 2000.
2. International Telecommunication Union; ITU-T Recommendation G.8261: Timing and synchronization aspects in packet networks; Geneva, Switzerland; May 2006.
3. International Telecommunication Union; ITU-T Recommendation G.8262: Timing characteristics of synchronous Ethernet equipment slave clocks; Geneva, Switzerland; August 2007.
4. International Telecommunication Union; ITU-T Recommendation G.8264: Distribution of timing through packet networks; Geneva, Switzerland; October 2008.
5. Texas Instruments; LMK04800 Family/LMK04816/LMK04906 Datasheet.

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