ADC081000,ADC081500,ADC08D1000, ADC08D1500,ADC08D500,LMH6550,LMH6574, LMH6703,LMH6704,LMH7220,LMK02000, LMK03000,LMK03001,LMX2531

Generating Precision Clocks for Time- Interleaved ADCs

Literature Number: SNAA124

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No. 109

Generating Precision Clocks for Time-Interleaved ADCs

— By James Catt, Applications Engineer

Many digitized test and measurement applications requiring both high resolution *and* high sampling speeds in excess of what can be delivered by a single Analog-to-Digital Converter (ADC) commonly use multiple ADCs whose sample clocks have staggered phases. Broadband communication systems can also benefit from this architecture. ***Figure 1*** illustrates a *time-interleaved* ADC sampling architecture.

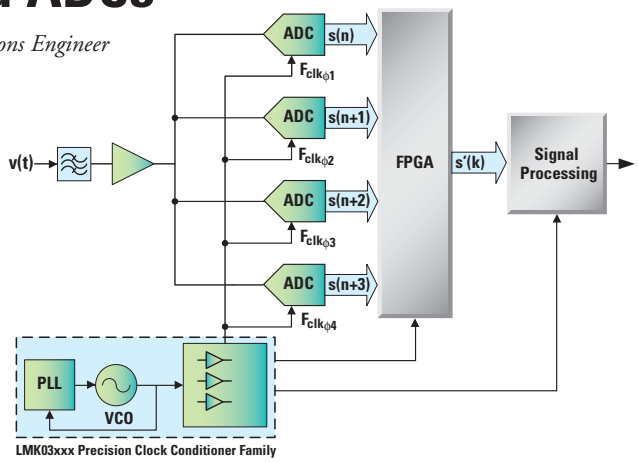

Figure 1. Time-Interleaved ADC System

Mathematically, the concept is simple. Even though each ADC is clocked at the same speed, the evenly staggered clock phases result in an effective increase in sample rate. The effective sampling rate is the number of ADCs multiplied by the sample clock. ***Figure 2*** illustrates the time domain relationship between the sample clocks, in this case a four ADC system.

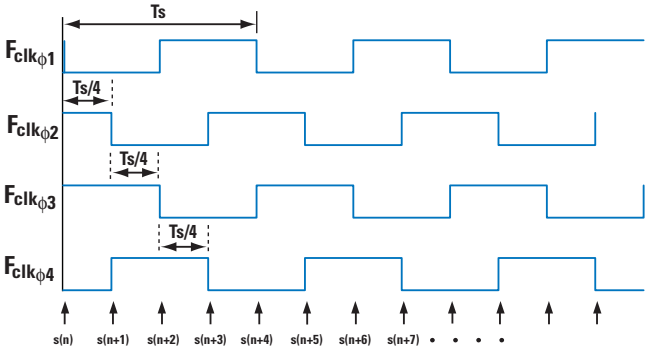

Figure 2. Staggered Sample Clocks For a Time-Interleaved 4-Channel ADC System

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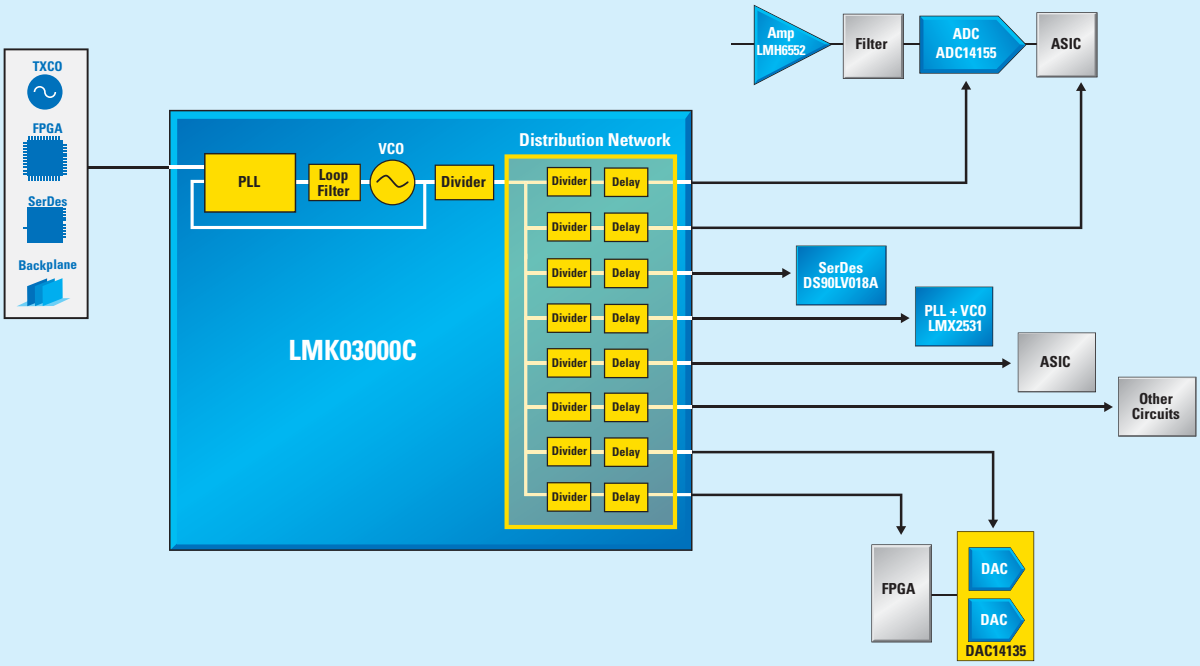

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Generating Precision Clocks for Time-Interleaved ADCs

In *Figure 1* the input to each ADC channel is sampled at the rate of Fs (= 1/Ts) samples per second (SPS). Each ADC sample clock is offset relative to the other sample clocks by a fraction of the clock period Ts. If M is the total number of ADCs, then the fractional phase offset is (in units of one clock period): $\phi_m = \frac{m \cdot T_s}{M}, m = 0,1\ldots,M-1$

The effective sample rate illustrated in *Figure 2* is $4 \cdot F_S$. However, the mathematical simplicity belies the complexity of implementing such a system. Hardware imperfections can destroy the performance of the system. In addition to noise and non-linearities that plague all hardware designs, the performance of time-interleaved ADC designs can be degraded by differences in DC offset, gain, and clock skew between the ADCs. *Figure 3* illustrates how these differences are modeled.

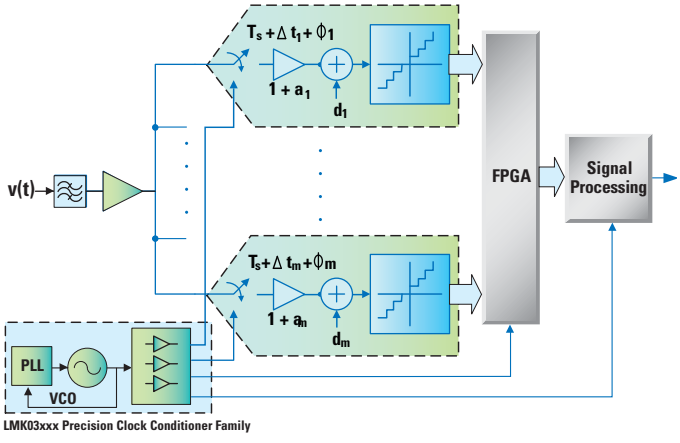

Figure 3. ADC Model with DC, Gain, and Time Skew Offsets

The model in *Figure 3* shows a gain offset parameter a_m for the m-th channel and a DC offset, d_m. The Δt_m parameter applied to the sampling switch instant represents a fixed but arbitrary time skew relative to the ideal sample instant. While the gain and DC offsets are intrinsic to the ADC circuitry, the time skews, Δt_m, originate in the external clocks. The cause of the time-skew may be in the circuit used to create the phase offsets in the clocks, or it may be the result of path length differences in the clock lines. In future articles, these causes will be more fully examined.

All of these imperfections in the ADC channels must be addressed during the system design phase. There is a significant amount of literature that discusses different approaches to compensation and correction schemes for time-interleaved ADC architectures. This article will address the impacts of sample clock time skew and its relation to the topic of precision timing devices.

To gain a better understanding of the impact of the clock skew between ADC channels, a 4-channel time-interleaved system will be analyzed. The time-domain representation of the sampling process is shown in *Figure 4*. The ideal sampling times are indicated by the arrows. The actual sampling times (with skew) are shown as the vertical dotted lines slightly offset from the ideal sampling points. The resulting amplitude errors are replotted on the time axis at the bottom (magnified). In a periodic signal the sampling error due to the clock skew is periodic as well.

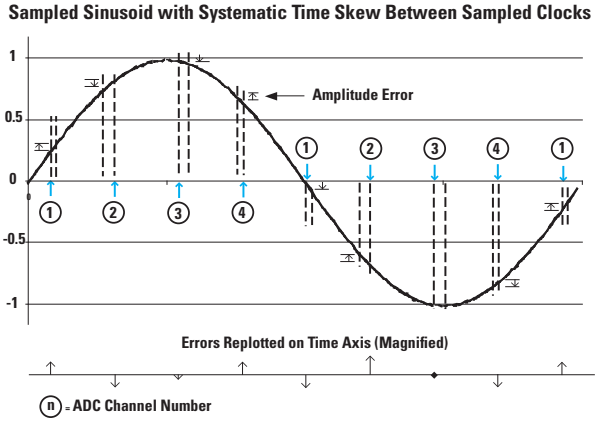

Figure 4. Sample Clock Time Skew Errors in an Time-Interleaved ADC System, M=4

Figure 5 shows another plot of an error signal in a sampled sinusoid due to time skew between clocks. The periodicity of the error signal is clearly seen. Note that the error reaches a maximum at points in the signal where the slope is the steepest.

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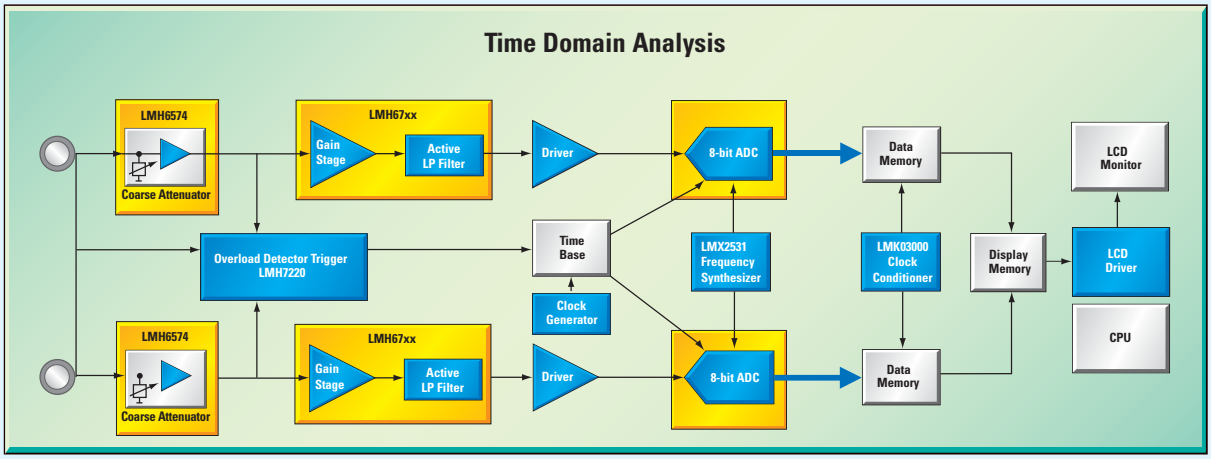

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ADC08D1500	8-Bit, dual, 1.5 GSPS (3 GSPS in DES mode)

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LMH6574	4-to-1 multiplexer	500 MHz	13	2200	SOIC-14
LMH6550	Differential amplifier	400 MHz	20	3000	SOIC-8
LMH7220	2.9 nsec high-speed comparator with LVDS output	2.9 nsec	6.8	600 psec	TSOT23-6

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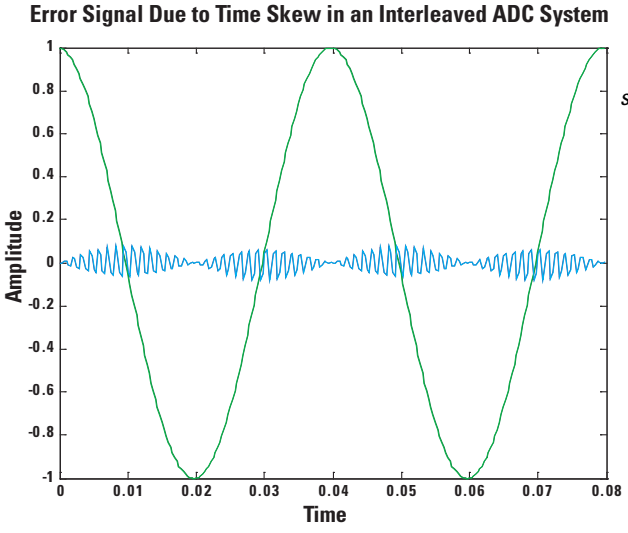

Figure 5. Error Signal Due to Time Skew between Interleaved ADC Clocks, M=4

The frequency domain plot is shown in ***Figure 6.***

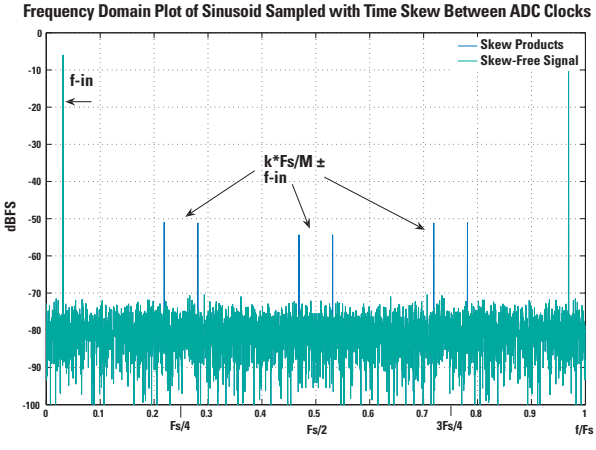

Figure 6. Frequency Domain Plot of Sampled Sinusoid with Spurs Due to Time Skew

If we consider the sample stream $\{s_m(n)\}$ from the ADC in the m-th channel of the system with time skew error, the sample sinusoid can be represented by:

$$s_m(n) = \cos(2\pi f_{IN}(n + r_m)T_s),$$

where r_m = the fixed skew error for the *m-th* ADC channel as a fraction of the sample clock period (T_s), $r_m \in [0,1)$.

Some trigonometric manipulation yields:

$$s_m(n) = \cos\left(\frac{2\pi f_{IN} \cdot n}{f_s}\right) + 2 \cdot \sin\left(\frac{2\pi f_{IN} \cdot r_m}{f_s}\right) \sin\left(\frac{2\pi f_{IN} \cdot (n + \frac{r_m}{2})}{f_s}\right),$$

where fs = sample clock frequency.

The first term in the summation is the desired term, so the 2nd term represents the error due to skew. The amplitude component of this error term depends on f_{IN} and r_m, which should not be a surprise. As f_{IN} increases, the slew rate increases and hence the voltage change over the skew interval increases, leading to increased error. Likewise, as r_m increases, the greater the chance that the signal magnitude will change significantly over the skew interval, also leading to a larger error term. We can see that as r_m goes to zero, the error term goes to zero. There is also an additional frequency component that is in quadrature to the desired component. As indicated in ***Figure 6***, it can be shown that the spurs due to time skew in the multiplexed signal will correspond to $\pm f_{IN} + \frac{k \cdot f_s}{M}$, meaning that they appear as sidebands centered at frequencies $\frac{k \cdot f_s}{M}$, k = 0,1,…,M-1.

In a more noise-like random signal, such as a signal with wideband digital modulation (for example: HDTV, digital cable, WCDMA), the sampling errors due to skew are randomized and so appear as additive random noise and raise the noise floor, decreasing SNR. It should also be clear that increasing skew leads to larger spurs in the periodic signal, and higher noise floor in the modulated signal.

SNR is often the figure of merit that is most indicative of system performance. Hence, the designer needs to be able to predict the degradation in system SNR for some given set of clock skew values. In most cases, however, clock skew can only be controlled to within some interval with some confidence level. In other words, the realized clock skew values and their allocation to different ADC clock inputs are random. Because SNR depends on the random time skew values, it is also a random variable. Therefore, the best we can do is to understand its distribution so that a confidence interval for SNR can be established for a particular distri-

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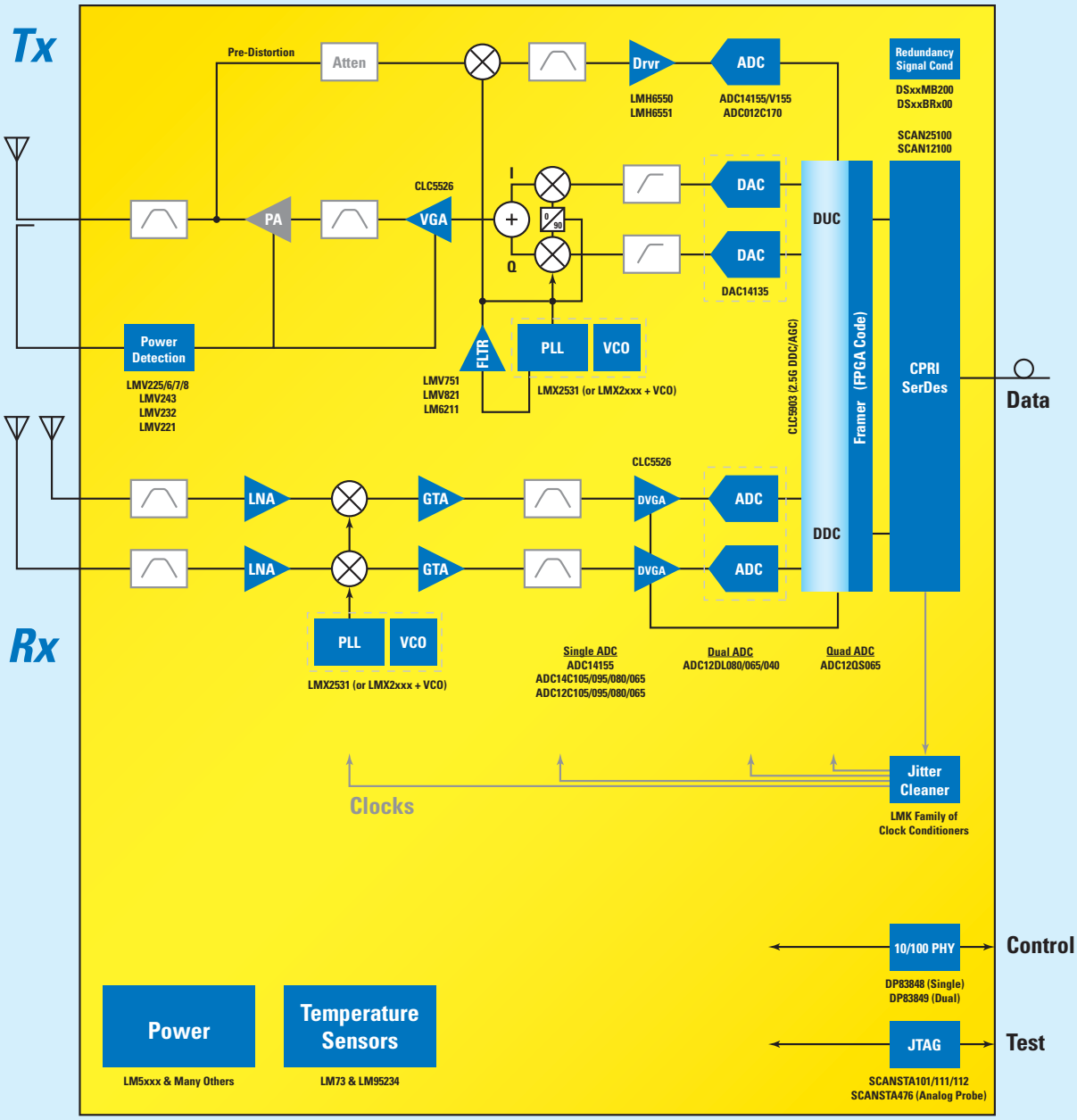

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Generating Precision Clocks for Time-Interleaved ADCs

bution of clock skew values. The key then is relating the statistics of clock skew to the confidence interval for SNR. ***Reference [1]*** addresses this question and derives a closed form of the Probability Density Function (PDF) for SNR that is generalized to any of the ADC channel mismatch parameters. This derivation assumes that the mismatches are Gaussian random variables.

While the closed form expression for the PDF provides good insight, it does not take into account the impact of clock skew in combination with quantization noise. One way to gain insight into these combined effects is to model them using a tool such as Matlab. For example, a 4-channel time-interleaved ADC system model was implemented and simulated in Matlab. The ADCs used in the model employed perfect quantizers so that the distortion contained in the output of the ADC was attributable only to the quantization operation and sample clock skew. Hence, the sensitivity of SNR to clock skew can be isolated from other distortion effects that may also be observed in a sampled signal in the real world. Once a model has been constructed and tested for validity, it can then be used to examine sensitivity relative to the standard deviation of the clock skew and number of time-interleaved ADCs. For example, ***Figure 7*** shows the results of simulations for resolutions of 14 and 12 bits when the input signal is band-limited Additive White Gaussian Noise (AWGN). A Gaussian signal was used in this example because its statistics are similar to many wide-band digital signals. Because skew is a random variable with respect to each ADC clock input, the model allows us to run several thousand simulations in which each simulation run assigns random but fixed values of skew to each ADC clock, drawn from a zero mean Gaussian distribution with a chosen standard deviation (in UI). The SNR is calculated for each simulation run, and a histogram of SNR values is generated after completion of all the runs. Examples are plotted in ***Figure 7***.

The key observation to be drawn from ***Figure 7*** is that for a given Standard Deviation (SD) of the clock skew, in fractions of a unit interval (UI = one clock period), the SNR distribution will be dispersed. A secondary observation is that as expected,

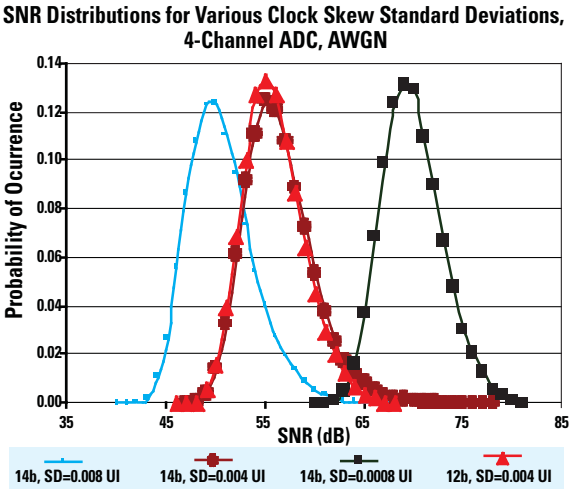

Figure 7. SNR Distributions for a 4-Channel Interleaved ADC System with Various Skew Distributions

SNR degrades as the standard deviation of the clock skew increases. In the 14-bit case, we see that when clock skew reaches 0.8% UI, the SNR of the sample stream has seriously degraded. Because most designs must meet a minimum target SNR, the histogram data represented in the plots in ***Figure 7*** enable the designer to begin evaluating design specifications for the clocking system driving the time-interleaved ADCs. The 90%, 95%, and 99% confidence intervals for SNR associated with a particular clock skew distribution can be estimated from the histogram data, allowing the designer to determine the suitability of a clocking design exhibiting such performance.

Summary

In this article, we have examined the impact of sample clock skew on time-interleaved ADC systems. National's LMK03xxx family of Precision Clock Conditioners with integrated VCO features multiple clock outputs that are locked to a single reference. These outputs may be edge synchronized, or, alternatively, programmable delay may be assigned to each clock output. Because path length differences can impact skew between clocks, having an adjustable delay capability is an important tool when designing a clocking scheme for a time-interleaved ADC system.

[1] G. Leger, E. J. Peralias, A. Rueda, J. L. Huertas, "Impact of Random Channel Mismatch on the SNR and SFDR of Time-Interleaved ADCs," *IEEE Transactions on Circuits and Systems – I: Regular Papers,* Vol. 51, No. 1, January 2004.

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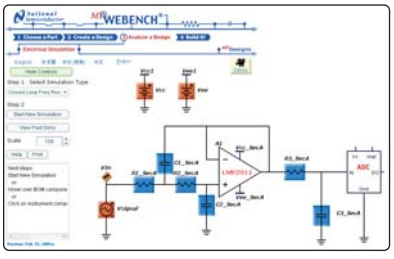

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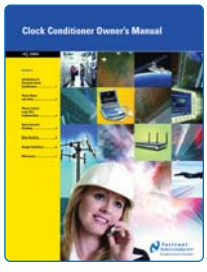

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