LMX2470

Delta Sigma PLLs Raise The Standard For Performance

Literature Number: SNAA094

Delta Sigma PLLs Raise The Standard For Performance

Application Brief 125

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Introduction

The high performance, low power, and low cost requirements of today's mobile telephone handsets sometimes put designers between a rock and a hard place. System issues such as integration level, type of architecture, and critical system performance all affect key parameters such as linearity, error rates, power consumption, cost, and time-to-market. Meeting CDMA specifications adds additional requirements over other technology segments such as GSM by requiring much finer frequency resolution. This forces designers to use narrow loop bandwidths, which can compromise the system's ability to switch in fast timeframes. Faster switching times imply longer standby times, which means that the battery life is increased. Set frequency plans limit the options, which can be used to trade-off phase noise, spurs, and locktime in CDMA frequency synthesis design. PLL manufacturers often focus their design efforts on improving phase noise and reducing spurs. National Semiconductor and others have developed the delta sigma PLL as the next revolutionary product in the quest for the optimum frequency synthesizer.

Advantages Of Using A Delta Sigma PLL Over A Traditional Fractional N PLL

Traditional Fractional N PLLs tend to have high fractional spurs. There are several ways to compensate for these spurs, but these techniques are analog and can vary over the wafer process. Analog compensation can also add significantly to the phase noise. Delta sigma modulation can be used to compensate for the fractional spurs, and is based on digital algorithms. The basic concept is that the energy of the fractional spurs at lower frequencies is pushed out to higher frequencies by modulating the N counter. Higher order modulators push this energy out to higher frequencies. However in practice, they also cause fractional spurs at a sub-multiple (1/2 or 1/4) of where traditional fractional spurs would be if there were not sufficient filtering.

The result of delta sigma modulation is a highly accurate frequency synthesizer with excellent phase noise, low in-band spurs, and very fast switching speeds. Delta sigma PLLs allow one to raise the comparison frequency to very high values for excellent phase noise. Unfortunately, a consequence of high comparison frequencies is a phenomenon referred to as cycle slipping.

Impact Of Cycle Slipping On Lock Times

Cycle slipping occurs when a large frequency error is presented to the phase detector and the loop bandwidth is not sufficient to correct for it in a fast timeframe. The phase detector then causes a temporary correction in the opposite direction than it should. The result of this cycle slip is extra time required for the phase detector to lock to the correct frequency. The net impact of cycle slipping is that it increases lock time. Cycle slipping occurs generally in situations where the comparison frequency is very high relative to the loop bandwidth. In general, if the comparison frequency exceeds about 100 times the loop bandwidth, cycle slipping begins to emerge as a problem.

Figure 1 shows this cycle slip phenomenon simulated for a PLL using the same loop filter. The product of comparison frequency times charge pump gain was held constant in order to keep all the loop dynamics exactly the same. Note that the rise-time and lock-time are severely degraded at higher comparison frequencies due to cycle slipping. This simulation was based on a 2 kHz loop bandwidth.

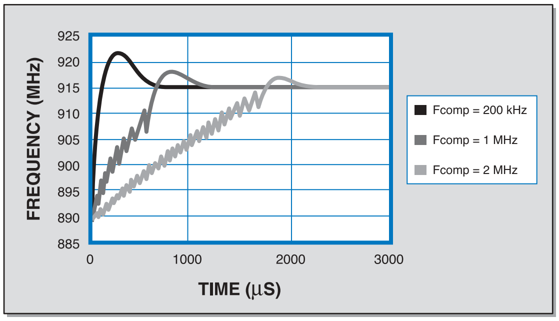

Figure 1: PLL Simulation Results

Fastlock Schemes vs. Cycle Slip Reduction

The concept of fastlock involves increasing the loop bandwidth initially, and then returning to a narrow loop bandwidth when the PLL is sufficiently close in frequency. Because this increases the loop bandwidth during frequency acquisition, it does help fight cycle slipping. However, fastlock schemes tend to be optimized for a second order loop filter and often require additional components to be switched in. Delta sigma PLLs tend to run at high frequencies and require higher than 2nd order filters in order to filter out all the high frequency noise generated by the delta sigma modulator. Furthermore, all fastlock schemes produce a disengagement glitch. The magnitude of this glitch tends to be worse at higher comparison frequencies.

Although fastlock techniques do help with reducing cycle slipping, cycle slip reduction circuitry can be optimized for any order of loop filter, and fights cycle slipping more aggressively. National Semiconductor has implemented a patented routine that involves switching the comparison frequency and charge pump gain in such a way that cycle slipping is reduced dramatically.

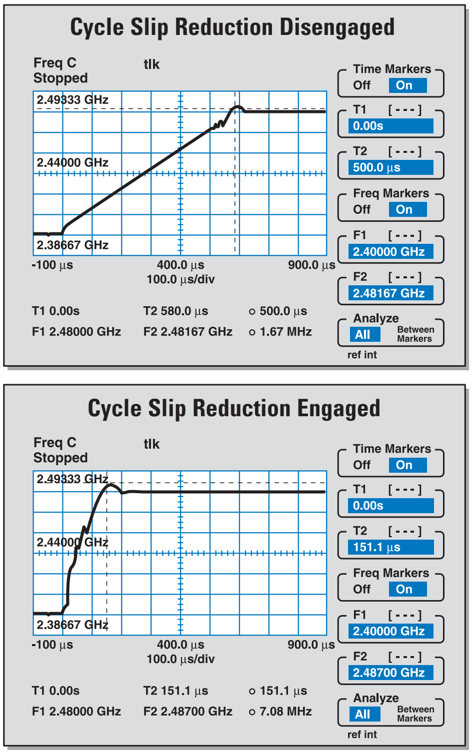

Figure 2

Delta Sigma Technology vs. Higher Power Consumption

Some delta sigma PLLs seem to draw a high amount of current to achieve low phase noise. This forces system designers to decide between low phase noise and long battery life. Is a delta sigma PLL worth the power drain? Delta sigma technology doesn't imply any more power drain than a conventional Fractional N PLL. Take the case of National Semiconductor's LMX2470. For some of the best phase noise in the industry, the LMX2470 only draws 5 mA at 2.5 V_{CC}, clearly setting the standard for current and performance.

Delta Sigma PLLs With Enhanced Features

Fastlock can be a useful method for achieving a faster locktime. However, additional programming is required which disengages the fastlock scheme as the PLL reaches frequency lock. This additional programming adds unnecessary overhead to the already complex DSP programming and can involve significant development time. Time out counters present in National Semiconductor's PLLs, including the LMX2470 delta sigma PLL, alleviate this double burden. Only one programming word is required to engage and disengage the fastlock and/or cycle slip reduction scheme. Programming is fast and simple.

A programmable delta sigma modulator is an enhanced feature only available in advanced delta sigma PLLs. This allows the designer the utmost in flexibility to optimize for the fastest locktime, lowest spurs, and lowest phase noise. Only National Semiconductor's LMX2470 has the ability to program the modulator order.

Summary

It is clear that delta sigma PLLs can advance frequency synthesis to higher levels of performance. However, not all delta sigma PLLs are created alike. Designers must look for delta sigma solutions like National Semiconductor's LMX2470 which have low phase noise, low spurs, fast locktimes, and address issues like low power consumption, fastlock timeout counters, and cycle slip reduction.

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