AN-2128 ADC1xD1x00 Pin Compatibility

ABSTRACT

In order to facilitate upgrading applications from a 10-bit Gig ADC to a 12-bit Gig ADC, the ADC10D1x00 (ADC10D1500/ADC10D1000) is designed to be pin-compatible with the ADC12D1x00 (ADC12D1800/1600/1000). This means that a single board layout may be designed with both resolution ADCs in mind for more cost efficient and time-to-market product development.

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1 ADC10D1x00 vs. ADC12D1x00

The only difference on the pin-out between the ADC10D1x00 and the ADC12D1x00 is that the ADC12D1x00 has two additional data bits for each output data bank. Bits<11:2> for the ADC12D1x00 correspond to Bits<9:0> for the ADC10D1x00. The placeholders for the two additional bits for the ADC12D1x00 are labeled as RSV bits on the ADC10D1x00. The RSV bits on the ADC10D1x00 correspond to the two LSB, Bits<1:0>, on the ADC12D1x00, see Table 1.

Table 1. ADC1xD1x00 LSB Pins

Ball No.	ADC10D1x00 Name	ADC12D1x00 Name
V10/U10	RSV7±	DQd1±
Y10/W10	RSV6±	DQd0±
W19/W20	RSV5±	DQ1±
W18/V17	RSV4±	DQ0±
B19/B20	RSV3±	DI1±
B18/C17	RSV2±	DI0±
C10/D10	RSV1±	DId1±
A10/B10	RSV0±	DId0±

2 Terminating RSV Pins on the ADC10D1x00

The RSV pins may be terminated in a way which makes one board usable for both ADC10D1x00 and ADC12D1x00, see Figure 1. On the ADC10D1x00, the RSV pins are high impedance, so only the 100Ω differential termination resistor for the LVDS driver from the ADC is necessary to be compatible with the ADC12D1x00. However, if these pins are terminated into an FPGA and it is necessary for them to be forced to a known voltage, then the additional 1kΩ resistors can be added to the design; the specific value of the 1kΩ resistors may be changed based upon the requirements of the specific FPGA. For a board that is populated with an ADC12D1x00, the 1kΩ resistors should be left unpopulated.

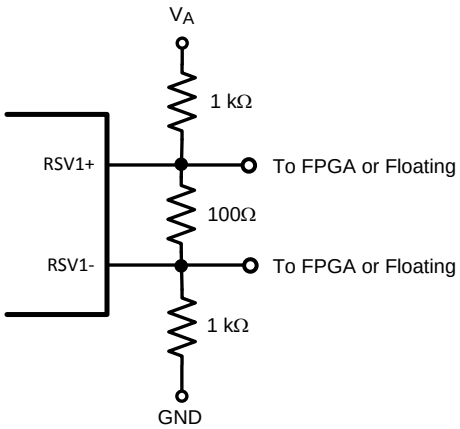

Figure 1. RSV Pin Termination

3 Data Sheet vs. Reference Board

For a few exceptions, Texas Instruments Reference Board does not follow the datasheet recommendations for certain pin connections. These exceptions are listed in Table 2. Historically, the exceptions exist because the Reference Board was developed before silicon development was finalized. In every case, it is correct to follow the datasheet recommendation. 'DNC' stands for 'Do Not Connect' and 'NC' stands for 'Not Connected.'

Table 2. Data Sheet vs. RB Comparison

Ball No.	ADC1xD1x00 Data Sheet Name	Reference Board Connection
C6	V_A	POREN (from FPGA)
C7	NC	WSS (from FPGA)
E3 / F4	DNC / DNC	VTEST± (to header)
D1	DNC	GND
D7	DNC	VNEGI (shorted to J4/K2)
U7	DNC	VNEGQ (shorted to L2/M4)
W3	DNC	CALFAIL (to FPGA)
R3, R4	V_{TC}	VA-C(1:2)
G1, G3, G4, H2, J3, K3, L3, M3, N2, P1, P3, P4	V_{TC}	VA-T(1:12)

The following is an explanation of the differences:

- **C6** – This pin was used for an internal test function for pre-production silicon, but it is not bonded in production parts.
- **C7** – This pin was used for an internal test function; it is not bonded in production parts and may be connected to any potential or left floating.
- **E3/F4** – These pins are used for internal test functions; do not connect them.
- **D1** – This pin was used for an internal test function for pre-production silicon, but it is internally bonded in production parts.
- **D7** – On an earlier version of the silicon, J4/K2/D7 were shorted externally. On final silicon, D7 is connected to the other pins internally, so it is no longer necessary to do so externally.
- **U7** – On an earlier version of the silicon, L2/M4/U7 were shorted externally. On final silicon, U7 is connected to the other pins internally, so it is no longer necessary to do so externally.
- **W**3 – This pin is used for an internal test function; do not connect it. Despite its name, note that the CALFAIL pin does not indicate that the execution of the calibration process has actually failed.
- **R3, R4** – On the original design, the analog clock supply (VA-C) and the analog track-and-hold supply (VA-T) were electrically separate. These pins were for the analog clock supply.
- **G1, G3, G4, H2, J3, K3, L3, M3, N2, P1, P3, P4** – These pins were originally for the analog track-and-hold supply (VA-T). Although the clock and track-and-hold supplies were kept separate for the purpose of initial evaluation, it was determined that there is no significant performance advantage to keeping them separate. So, for greater simplicity, they are combined in the datasheet.

4 Planning for Power Consumption

In general, higher speed ADCs consume more power and the ADC12D1x00 family consumes more power than the ADC10D1x00. If a system will be upgraded from a 10-bit to 12-bit ADC, take care to design the power supply accordingly with margin, so that it can supply the maximum required power. The limits for the power consumption, P_C, may be found in each datasheet.

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