# Accelerating Analog Performance With Packaging Breakthroughs

**Les Stark**
Director of Package Development

**Sreenivasan Koduri**
TI Fellow

# At a glance



## Introduction

Semiconductors permeate nearly every aspect of life, with devices optimized for use in every application that you can imagine. Complementary metal-oxide semiconductor (CMOS) technology, guided by Moore's law, has fueled advances in digital computing, while variations of bipolar semiconductors have enabled analog products that connect digital processors to the physical world, detecting temperature, pressure, movement, light, sound and touch.

Every wafer contains thousands of integrated circuits (ICs), which are separated into individual units known as semiconductor chips, or dies. These chips are fragile, and require protective packaging for everyday use inside products from smartwatches to industrial robots. As shown in **Figure 1**, among other effects, a package protects the semiconductor chip, provides electrical connections to the printed circuit board (PCB), and provides a path for heat dissipation. As applications for semiconductor devices grew, package functionality and form factors evolved to meet different needs.

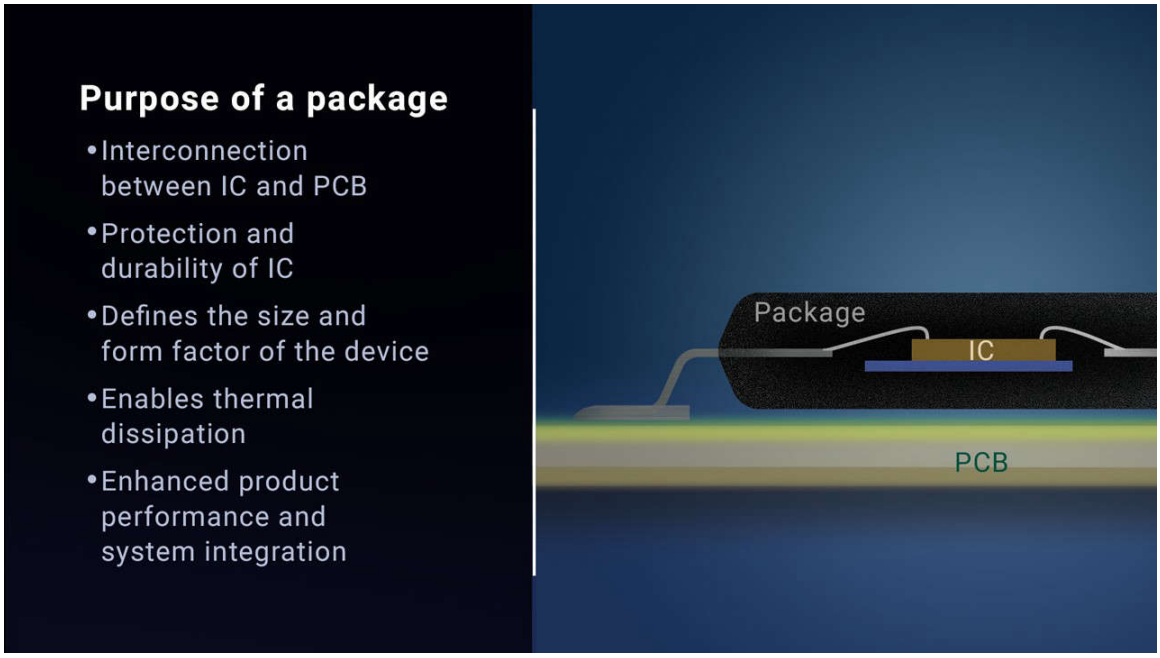


***Figure 1.*** *Internal diagram of a typical analog package, and what packaging accomplishes.*

A semiconductor device consists of a package that optimizes performance and protects the chip. Each package comprises several elements as outlined in **Figure 2**, including pins (or leads), resin, bond-wire and the chip itself. Pins or leads are the interface between the device and external circuitry, facilitating the transfer of signals and power. The resin covers the chip and bond-wires, protecting or shielding against factors such as moisture, dust, vibration and impact. The bond-wire connects the chip to the package leads, enabling electrical connections between the chip and external circuitry on a PCB.

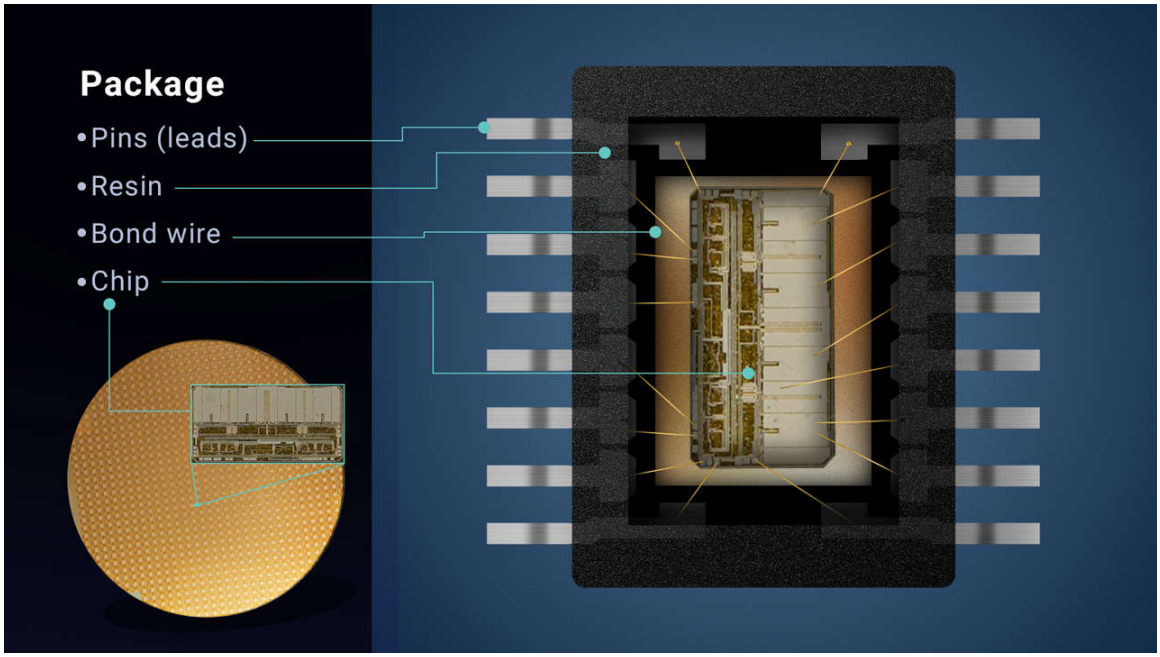


***Figure 2.*** *A package includes pins (or leads), resin, bond-wire, the chip-attach epoxy and the semiconductor chip itself.*

In today's rapidly changing electronics landscape, design engineers are under tremendous pressure to get the analog semiconductors they need to meet stringent performance, cost and time-to-market requirements. A product portfolio with diverse packaging options gives designers the flexibility to leverage different package types and technologies to optimize performance, form factor, thermal management and cost-effectiveness, helping them innovate and accelerate time to market. Engineers have depended on industry-standard packages for decades. **Figure 3** shows several common and plastic packages for analog and power-management ICs.


***Figure 3.*** *Common package types and miniature plastic packages for analog and power-management ICs.*

## How package variations meet market demands

Because no single package type meets every electronic device's design requirements, over the years diverse packaging types evolved to address specific needs such as reliability, electrical performance, thermal performance, cost, supply-chain considerations and size.

For example, reliability requirements differ widely based on application, from simple electronics in a small toy to vital components in automotive braking systems. Industrial implementations require long-lasting ICs, while communication towers in climates like Dubai, Singapore or Alaska need devices that can withstand temperature extremes, humidity and corrosive environments. ICs installed in a spacecraft must survive the shocks of launch and endure radiation in space.

In high-speed communications or high-power applications, the electrical impedance of the package can significantly affect system performance, necessitating optimized connections between the chip and package, as well as between the package and the PCB. While traditional semiconductor devices relied on fine gold wire-bonds (typically 15µm to 50µm in diameter) for these initial connections, modern devices may also employ methods such as copper-wire bonding, ribbon bonding, high-density bonding, copper posts, copper clips, solder bumps and through-silicon vias to address specific electrical impedance requirements.

Let's take a look at the market requirements that drove the creation of diverse packaging options.

## Cost efficiency

When optimizing the PCB, package and silicon for cost, minimizing the size of the silicon will lower costs; however, many applications may require larger packages with a large input/output (I/O) pitch. In **Figure 4**, spacing of the I/O pads are <100µm on the silicon to enable a small chip size, while these same I/Os are fanned out to >650µm to meet the design constraints for a low-cost PCB.

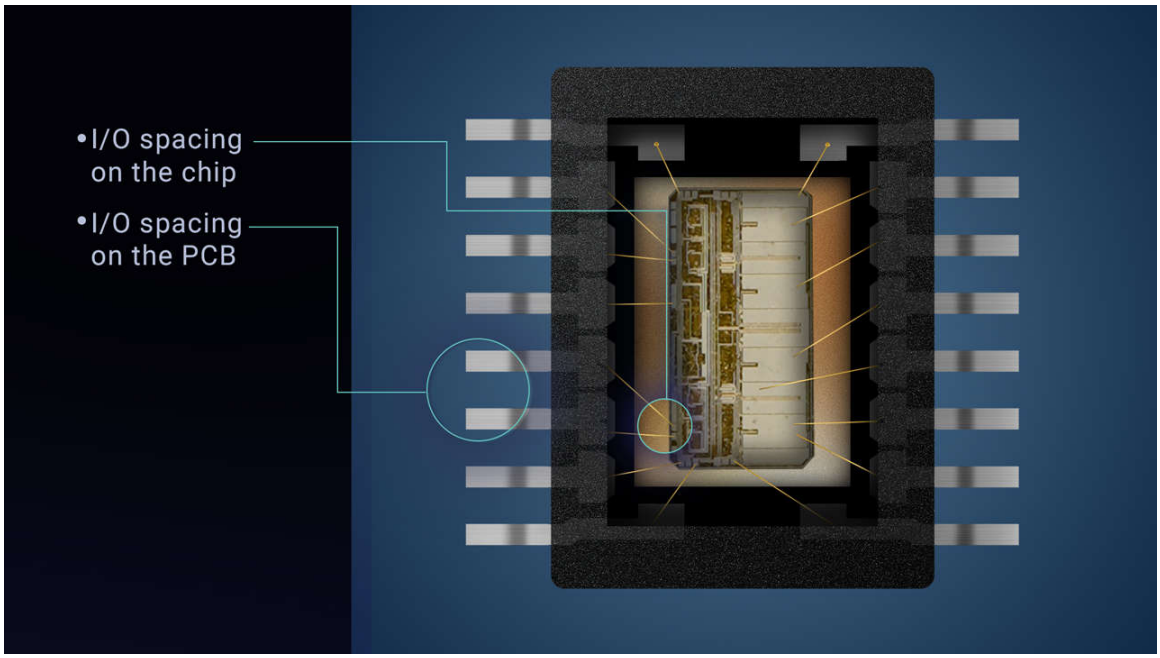


***Figure 4.*** *I/O spacing <100µm is typical for a compact chip design, while I/O spacing >650µm fits with low-cost PCB designs.*

Standardizing PCB dimensions and package sizes for commodity, general-purpose products makes it possible to purchase identical parts from multiple suppliers. Additionally, such packages offer the flexibility for the silicon to continue shrinking (which again, lowers costs) without impacting the fit in an end application. In some cases, packages can be shrunk while still allowing for **industry-standard footprints**. This enables a migration toward miniature packages with backward compatibility for existing PCB layouts.

## Power efficiency

Efficiency is the most important metric for designing high-power solutions. While TI offers discrete field-effect transistors (FETs) and regulators, integrating the FET with a controller is important in many power designs. Earlier designs relied on numerous gold wire-bonds (such as those shown in **Figure 5**) to minimize electrical resistance in FETs, with the cost of the wire sometimes exceeding that of the chip in the package. To reduce costs and improve power and performance, TI developed silicon technologies compatible with copper wire-bonds.

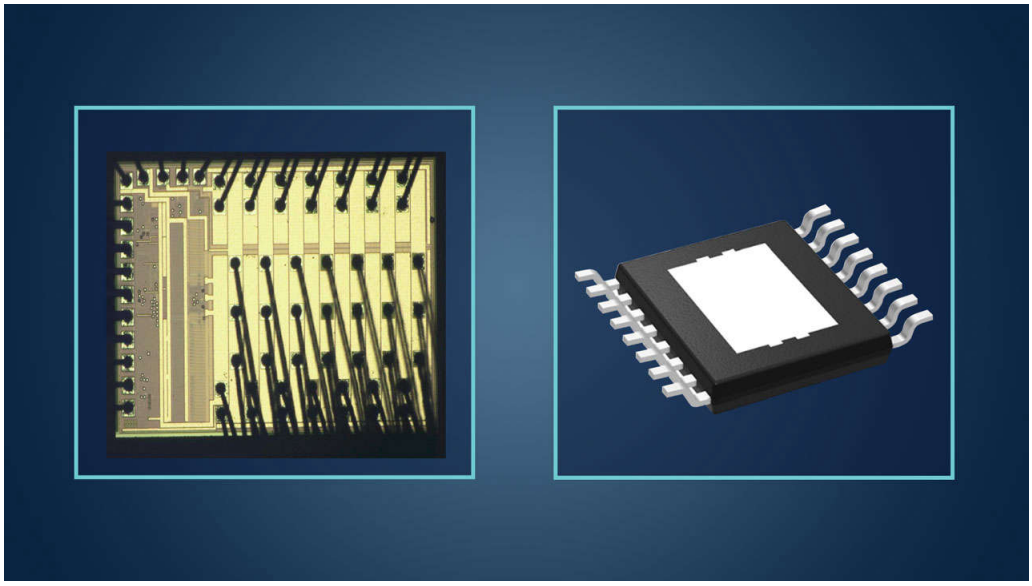

***Figure 5.*** *Even though a HTSSOP package may only have a few external pins, dozens of heavy-gauge wire bonds are needed to meet electrical current and resistance requirements for an integrated FET.*

As power densities increase, TI has adopted vertical FET technology and copper clips such as those shown in **Figure 6** to maintain low resistance in FETs in high-current packages.

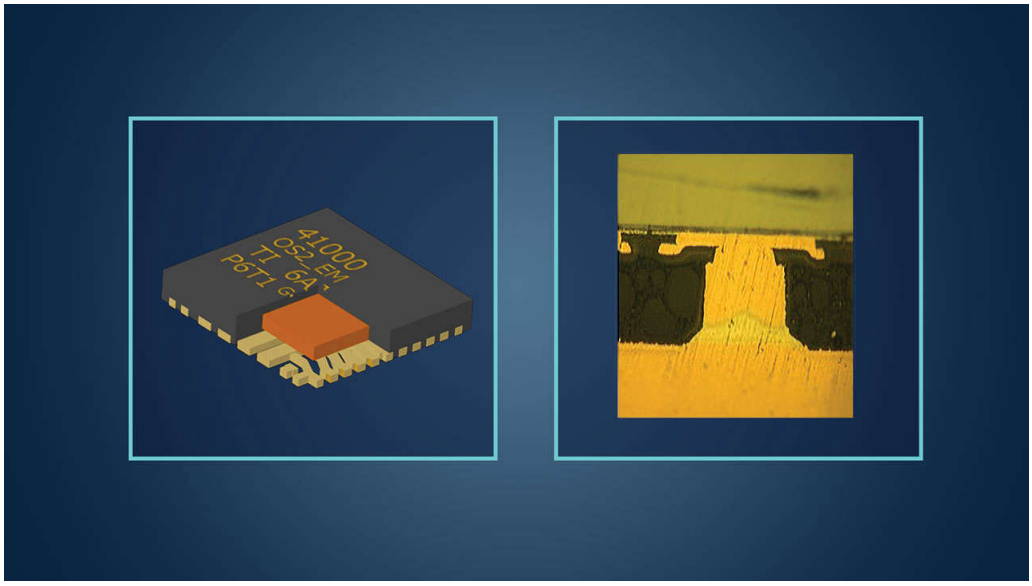


***Figure 6.*** *Copper clips are used in high-current packages to reduce resistance compared to multiple wire-bonds as shown in Figure 5.*

Innovations in semiconductor manufacturing have integrated CMOS and bipolar transistor technology on the same chip, and led to the development of high-performance FETs with integrated controllers. To meet demands for low electrical resistance and advanced controllers, TI created HotRod™ technology, which uses low-resistance copper bumps to closely connect the power circuitry on the PCB to the chip, as shown in **Figure 7**.

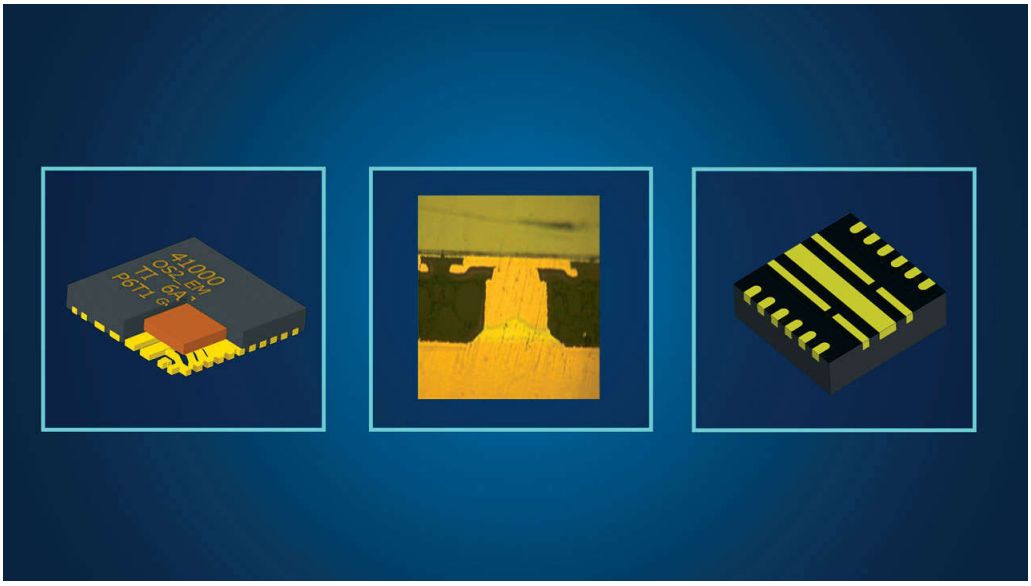

***Figure 7.*** *Copper bumps directly connect the silicon die to the copper in the package, providing a nearly direct path from the FET to the PCB.*

For designers requiring industry-standard package footprints, TI's **enhanced HotRod QFN package technology** offers the flexibility to route signals throughout the package – as shown in **Figure 8** – while maintaining very low-resistance connections to efficiently deliver power to end equipment.

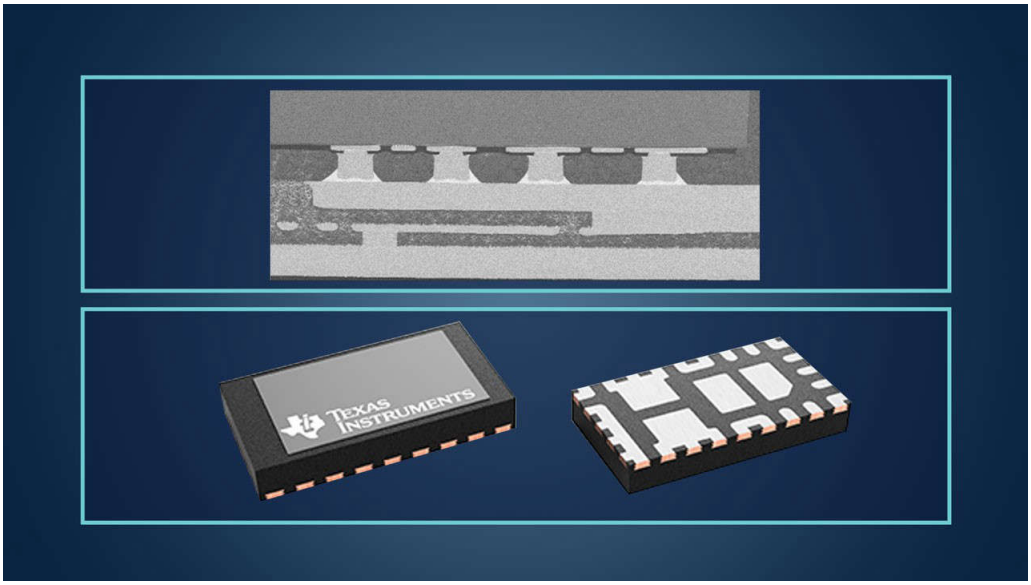


***Figure 8.*** *Enhanced HotRod technology connects the silicon to thick copper routing layers. This approach enables very low resistance to the PCB, while allowing flexibility for thermal pads or matching standardized package footprints.*

There are many applications, such an electronic stylus, that require extreme miniaturization. As shown in Figure 9 and Figure 10, integrating an inductor into the package helps address small-size constraints so that designers can implement a high-efficiency switching regulator where historically it hasn't fit. In addition to miniaturization, TI's **MicroSiP™ packages** (shown in **Figure 9** and **Figure 10**) are designed to transfer all of the module's heat to the PCB by closely coupling the chip to the thicker copper layers within the PCB.

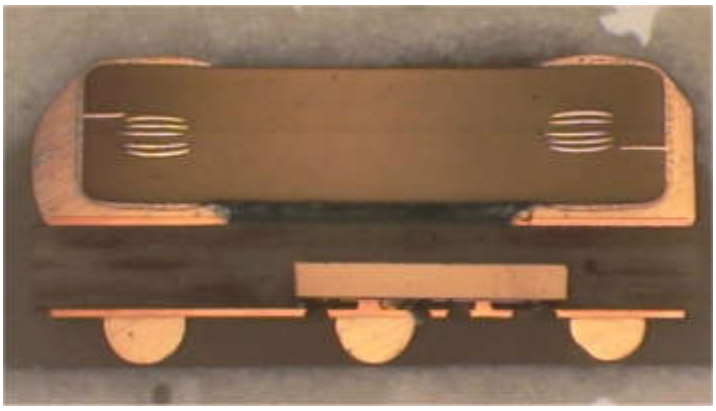

***Figure 9.*** *A cross-section of TI's TPS82670 step-down converter in the MicroSiP™ package. The embedded silicon circuit is located beneath its inductor*

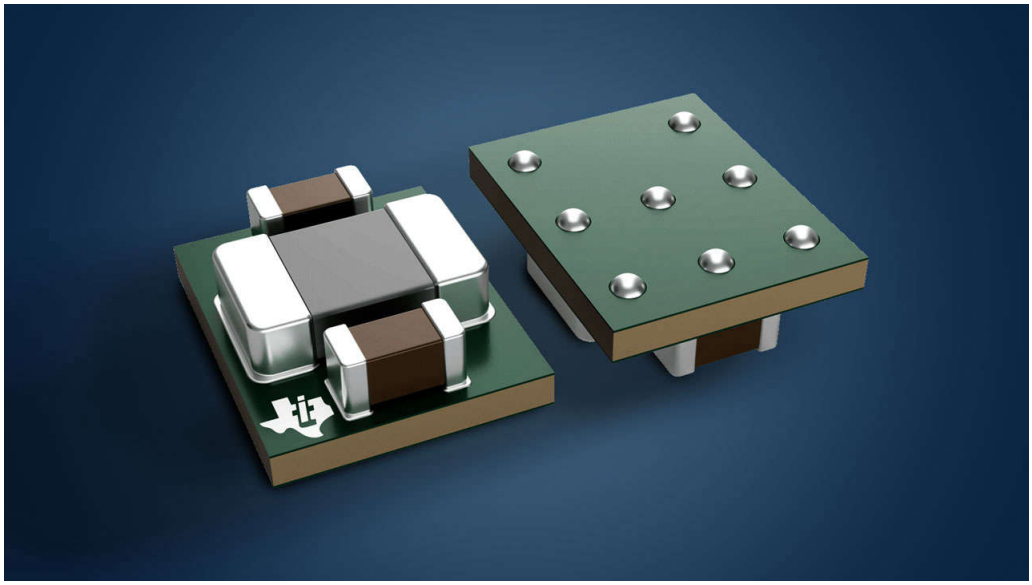

***Figure 10.*** *A top- and bottom-side view of the TPS82670 step-down converter in the MicroSiP package.*

Design engineers also need higher-power modules that integrate high-efficiency inductors directly into the package, while increasing the limits of power density. TI's new power modules leverage MagPack™ technology, our new proprietary integrated magnetic packaging, increasing power density and efficiency and reducing temperatures and radiated emissions while minimizing board space and system power losses. Modules with MagPack technology such as the **TPSM82866A** 6A step-down converter (shown in **Figure 11** and **Figure 12**) have a power density of nearly 1A per 1mm$^2$.

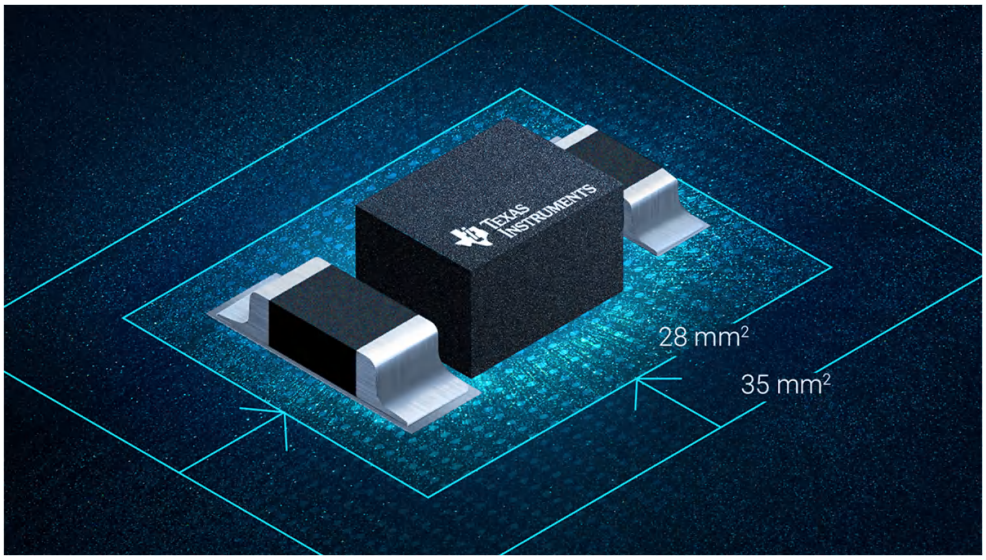


***Figure 11.*** *The TPSM82866A 6A step-down converter in the 2.3mm-by-3-mm MagPack package achieves a total solution size of 28mm2.*

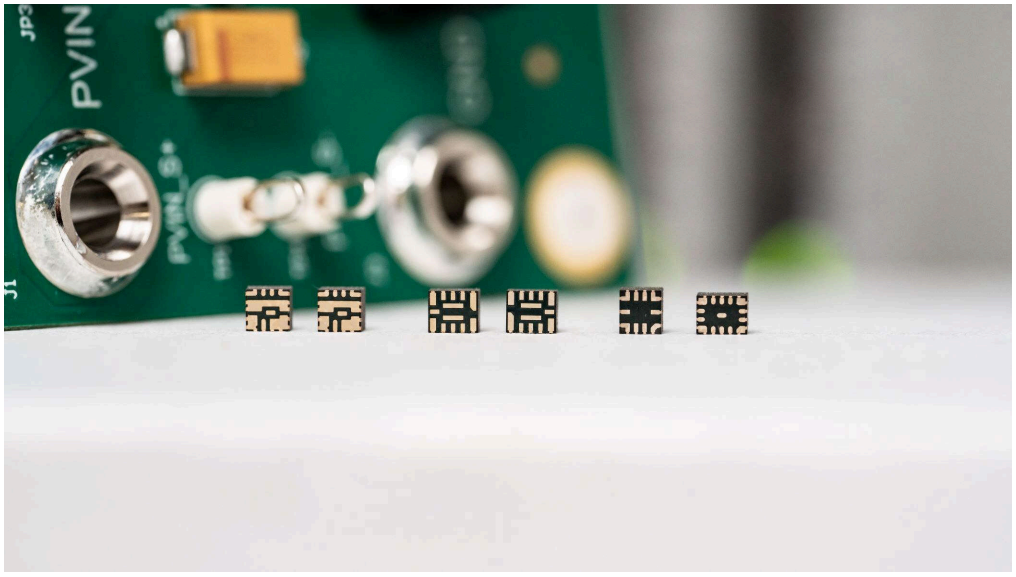


***Figure 12.*** *Power modules with MagPack technology are 20% smaller than competing 3A and 6A modules.*

Gallium nitride (GaN) power stages, with their high power density and ability to operate at higher voltages, are becoming popular in markets such as battery charging and solar energy. As **Figure 13** illustrates, TI's **100V LMG3100 GaN FET** with enhanced HotRod package technology enables the placement of thermal vias close to the input voltage, while power pads optimize power dissipation from the package.

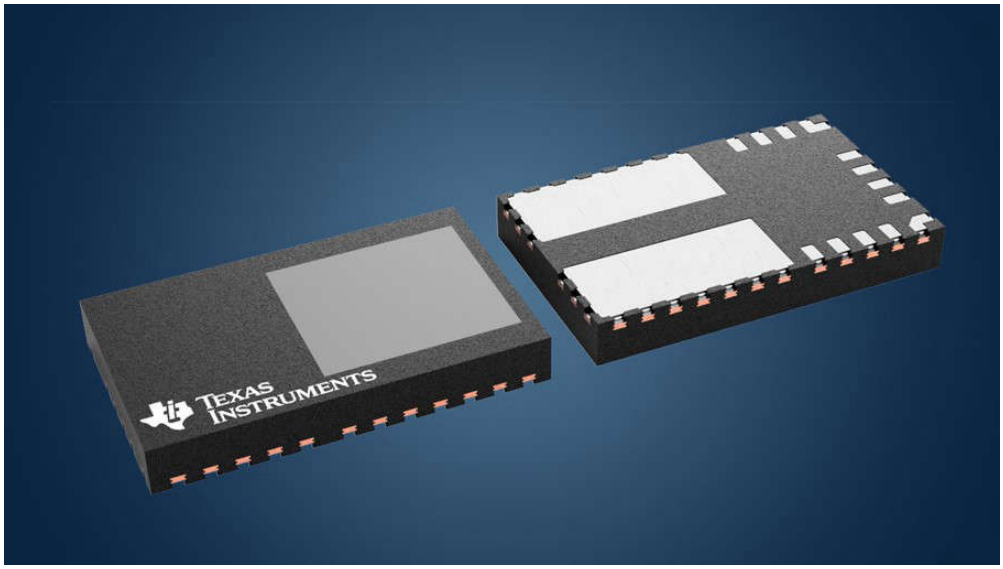


***Figure 13.*** *The LMG3100 GaN FET power stage in a 15-pin very thin quad flat no-lead (VQFN) package. The GaN device uses large source and drain pads and an exposed chip for improved thermal management.*

Another GaN-based device, TI's three-phase **DRV7308 GaN intelligent power module (IPM)**, comes in an industry-standard quad flat no-lead (QFN) 12mm-by-12mm package, which is 55% smaller than competing 250W IPMs and reduces PCB size more than 65%, as shown in **Figure 14**.

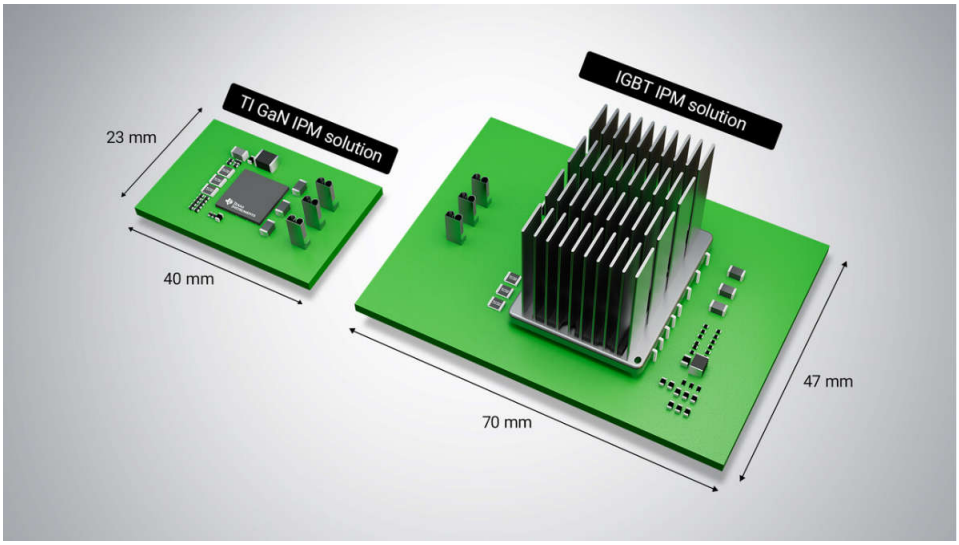


***Figure 14.*** *The DRV7308 GaN IPM PCB compared to a 250W insulated-gate bipolar transistor solution.*

## Enabling miniature products

When devices must be exceptionally small or thin for products such as smartphones, hearing aids or camera lenses, wafer chip-scale packages (WCSPs) are the best option. These packages are built directly on the wafer, with the I/O created on the silicon surface. Despite their compact nature, WCSPs such as the tiny current-sense amplifier shown in **Figure 15** require enhancements to help ensure reliability. Specialized overcoats protect the chip from mechanical stresses on the PCB, while optimized metallurgy withstands thermal stresses and potential mechanical challenges such as bending and dropping. Read the company blog, **The power of packaging** to learn how TI helps engineers create smaller designs.

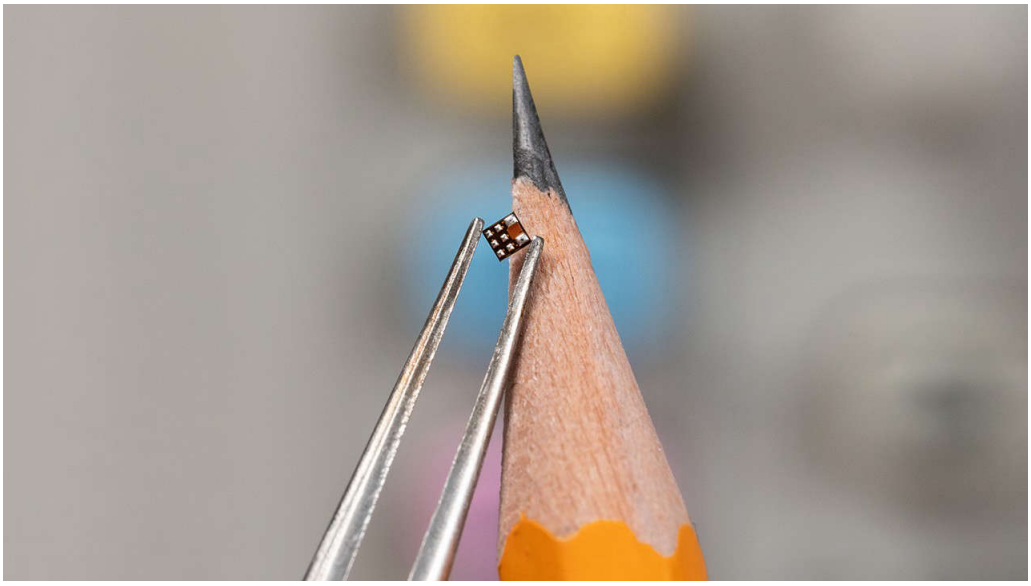

***Figure 15.*** *The INA700 current-sense amplifier with EZShunt™ package technology is available in a 1.2mm-by-1.33mm WCSP package, totaling an area of 1.637mm2. The integrated 2mΩ copper leadframe acts as a shunt resistor.*

## Precision solutions

Precision devices such as voltage references or clocks were traditionally housed in costly, low-stress ceramic packages. Today, it's possible to produce precision devices in more affordable plastic packages such as thin-shrink small outline packages (TSSOPs) while maintaining high levels of precision and performance. Additionally, low-stress molding compounds and buffer layers on top of the silicon further enhance performance. In oscillators, clocks and timing circuits, TI's **bulk acoustic wave (BAW) technology** reduces board space while improving timing accuracy at higher frequencies.

**Figure 16** highlights a cross-section of a BAW-based clock with low modulus material that decouples package stress to achieve high precision.

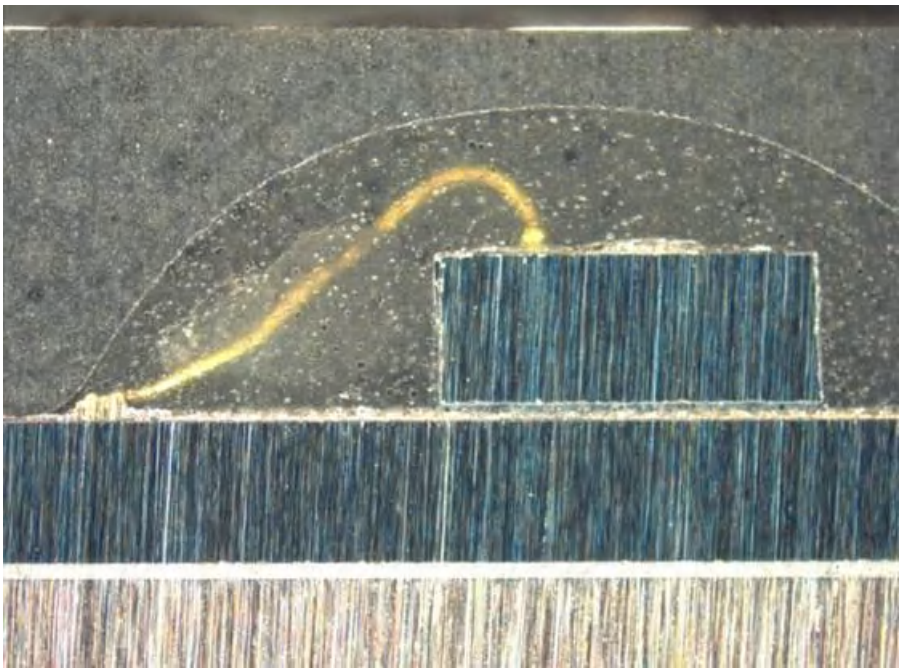

***Figure 16.*** *Cross-section view of a sensitive clock chip covered in low modulus material with TI's BAW technology decouples package stress from the silicon circuit, enabling consistent and accurate timing performance over a wide temperature range.*

## High voltage

Creating devices that operate at voltages exceeding 650V presents particular challenges. Preventing arcing outside the package requires adherence to strict industry standards for lead spacing and package design. Internally, materials such as specialized mold compounds must prevent dielectric breakdown over long periods of high temperatures, high humidity and a large bias voltage. Precise electric field analysis of package structures helps prevent arcing inside the package.

**Figure 17** shows the LMG3624 650V, 170mΩ GaN FET in a QFN package, which uses special high-voltage plastic and lead spacing. Additionally, the **LMG3650R035 650V, 35mΩ GaN FET** with integrated driver and protection supports currents up to 36A with greater thermal dissipation from a transistor outline leadless (TOLL) package with a thermal pad.

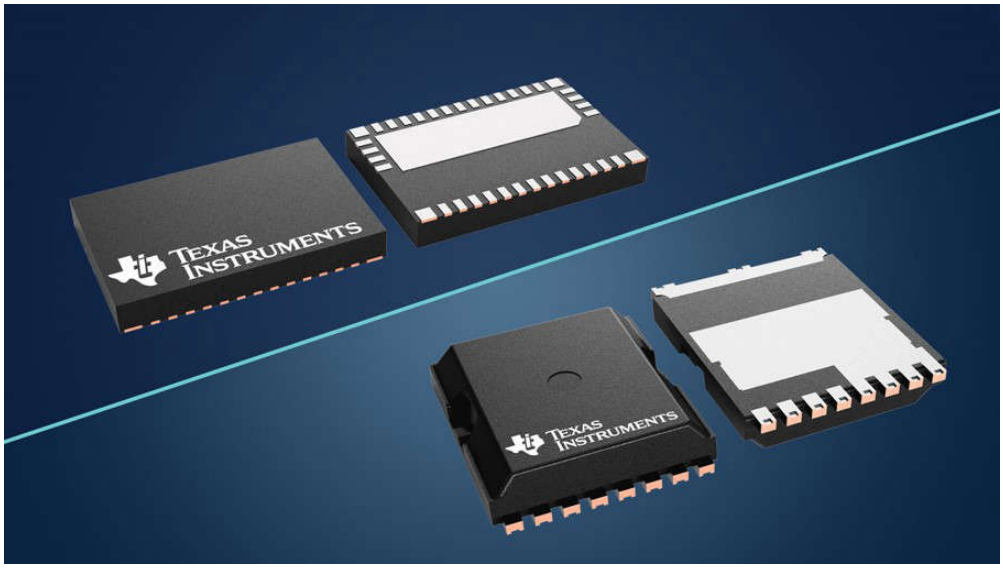


***Figure 17.*** *The 650V, 170mΩ GaN FET uses a QFN package for miniaturization while maintaining lead spacing to support high voltages. The 650V, 35mΩ GaN FET in TI's TOLL package with a thermal pad supports higher currents with improved thermal management.*

## Isolation

Isolation in electronics design is vital in electric vehicles, robotics and other applications where voltages can exceed thousands of volts. Isolation packaging helps facilitate safety and ensure system protection. For voltages over 200V, the shape of the wire-bonds and trajectory of the wire relative to the silicon are important. Wires too close to the silicon can create arcing paths across the isolation barrier. **Figure 18** shows the **TPSI3050-Q1 isolated switch driver**, which shares signal and power across the package, while the packaging isolates the voltage across the isolation barrier.

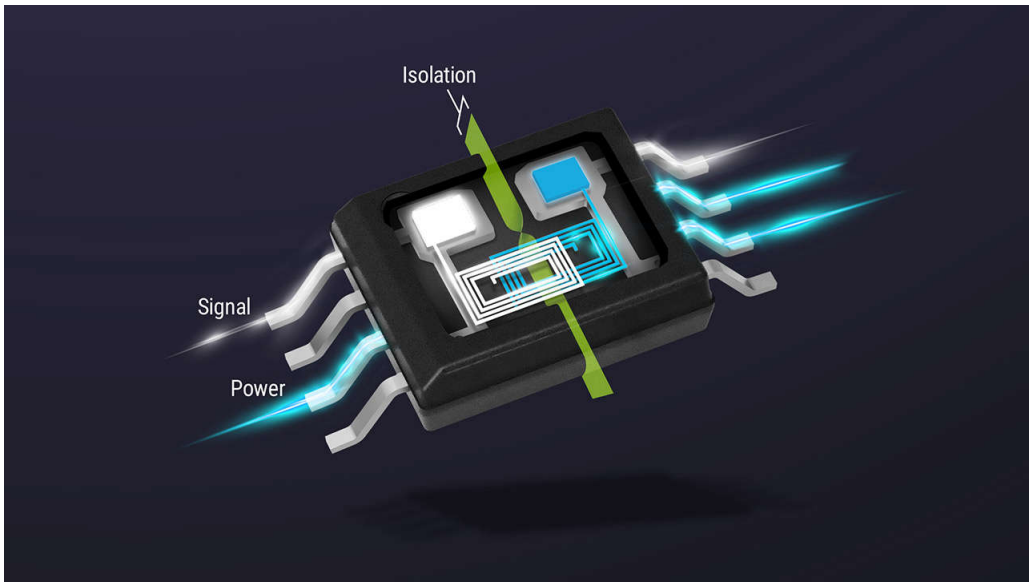


***Figure 18.*** *Using magnetic isolation to send both power and signals reliably across an isolation barrier.*

## Multiple chips in one package

Some designs benefit from the ability to integrate multiple silicon nodes into a single package. For example, battery-management chips such as the **BQ40Z50-R2** (see **Figure 19**) combine low-cost logic with flash memory and high-precision voltage measurement by stacking silicon.

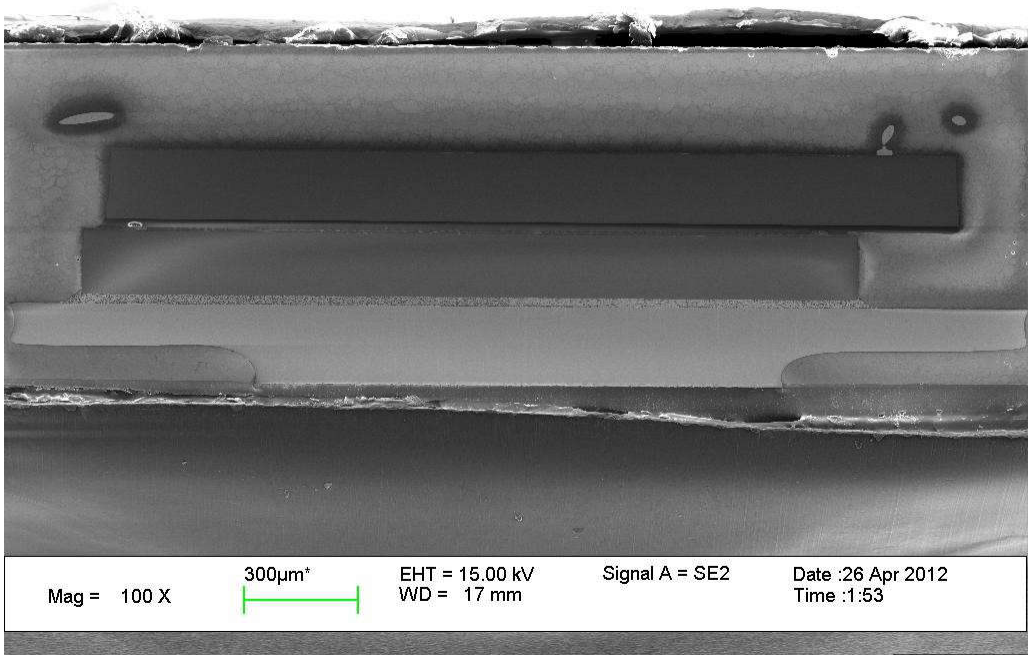


***Figure 19.*** *TI's BQ40Z50-R2 battery-management IC features two silicon technologies in a single package.*

Multichip packaging can also increase silicon density in a device. **Figure 20** demonstrates how the silicon area exceeds the physical footprint of the package by stacking multiple chips, doubling the available channels in an analog front-end device.

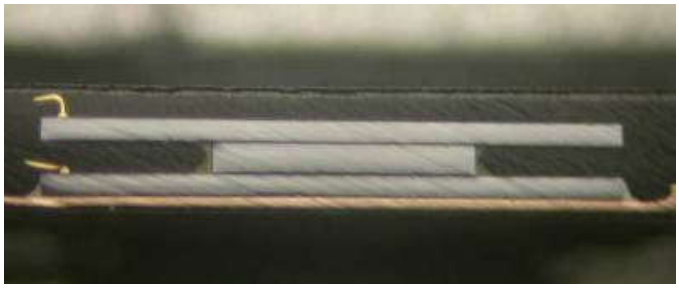

***Figure 20.*** *A multichip analog front-end package with increased density through silicon stacking.*

**Figure 21** shows a top view of an analog front-end package with two wires connecting each chip to each lead.

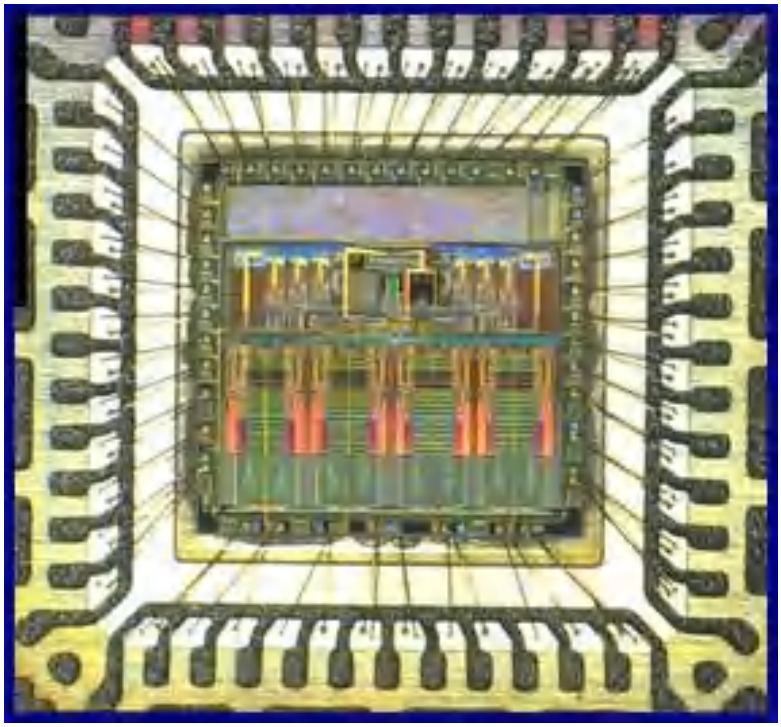

***Figure 21.*** *Top view of an analog front-end package.*

## Reliability testing for packaging

Reliability directly impacts product longevity, performance and overall system cost. TI implements **rigorous reliability testing** that meets industry standards such as Joint Electron Device Engineering Council (JEDEC), Automotive Electronics Council (AEC) and Qualified Manufacturers List (QML), to deliver quality products that operate consistently for long periods of time in applications such as automotive, factory automation and space.

TI has deep expertise in manufacturing analog products with a diverse range of package technologies, tailored to address the needs of different markets and applications. Whether designing for automotive environments with extreme temperature differences, industrial factory robots or tiny personal electronics, design engineers need IC packages that can withstand environmental stresses. TI develops packages to match strict design and safety requirements, including packages with thermal performance and long-term reliability.

**Figure 22** shows several packages undergoing high-temperature operation life testing.

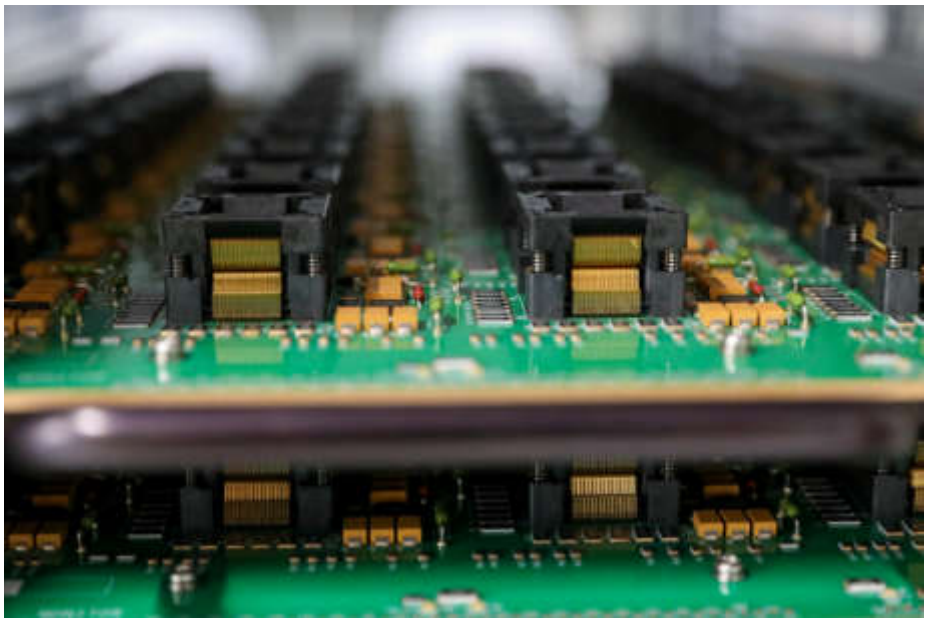

***Figure 22.*** *High-temperature testing in process at one of TI's assembly and test facilities, which includes multiple packages in test sockets on a board for high-temperature operation life.*

## Space-grade packages

**Space-grade devices** are designed with QML-certified packages, including QML Class V (QML-V) ceramic and QML Class P (QML-P) plastic packages designed to operate in the extreme conditions of space. **Figure 23** shows a QML-V ceramic package and QML-P plastic package.

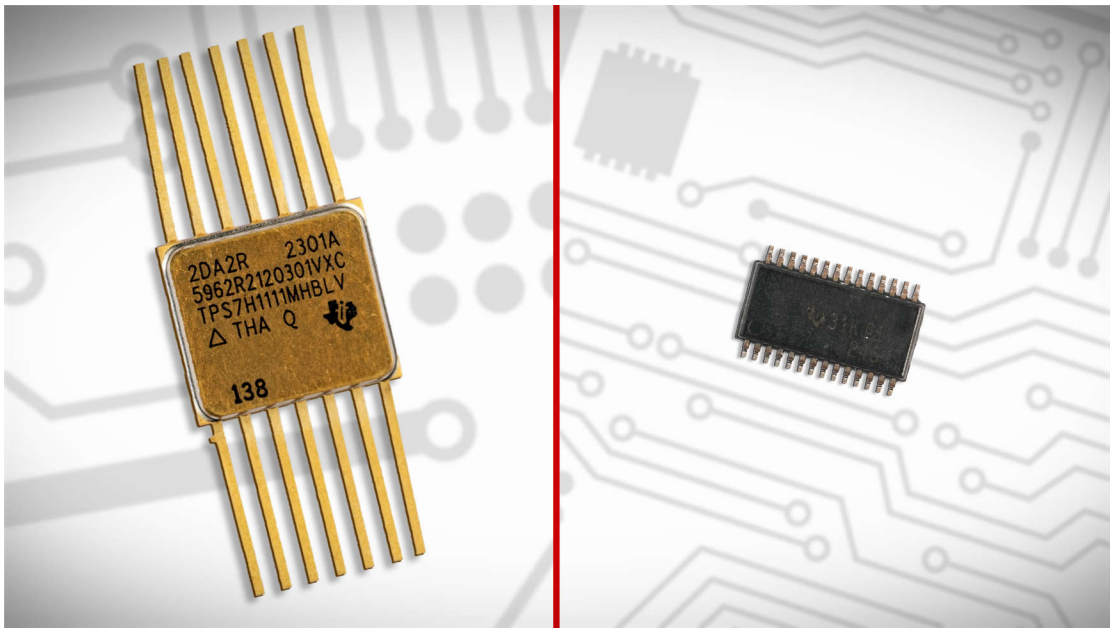


***Figure 23.*** *QML packaging capability allows TI to sell analog products for space-grade designs, including QML-V ceramic and QML-P plastic packages.*

Radiation-hardening techniques, including extended burn-in testing, and lot-by-lot qualification, enable space-grade components to meet stringent requirements of QML certification. **Figure 24** shows how space-grade packages are exposed to radiation for testing.

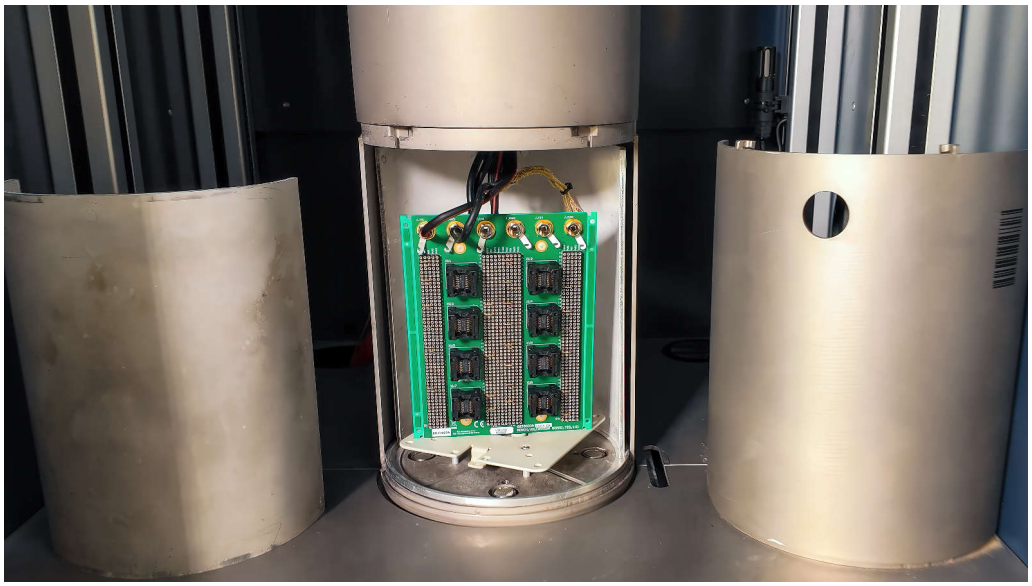

***Figure 24.*** *Radiation-hardened testing of high-reliability packages.*

Understanding how to balance reliability requirements is important when considering which devices and packages will perform the best on the PCB in certain applications. Ultimately, product and packaging tests help TI prepare products for shipment to customers all over the world. **Figure 25** shows the final test in TI's facilities before the company sends products to a product distribution center.

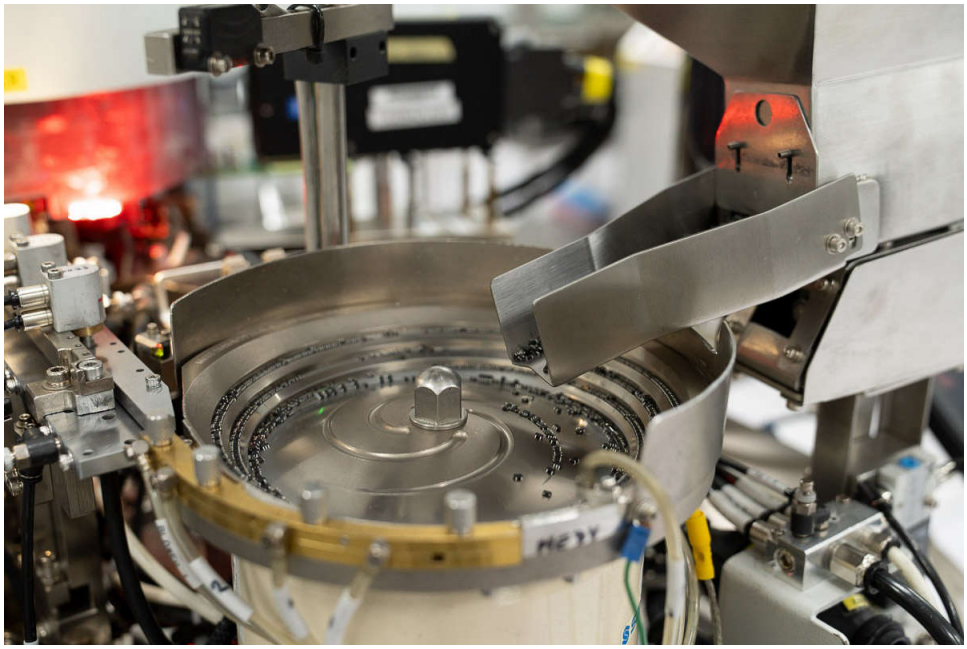

***Figure 25.*** *At the final step of packaging, every TI product is tested in preparation for shipment.*

## Conclusion

The trend of smaller, more compact design requirements will continue to grow. Advancements in analog packaging enable engineers to integrate more functionality into smaller form factors while maintaining high levels of precision and performance, enhancing user experiences and creating new design possibilities. Energy and computing systems now require devices packaged with specialized mold compounds that can withstand voltages exceeding 650V and maintain efficient operation over long periods of high temperatures, high humidity and large bias voltages. Automotive systems, industrial automation and health care devices rely on more reliable semiconductor solutions in packages that can withstand a range of environmental conditions such as adverse conditions, extreme temperatures, vibrations and electromagnetic interference.

TI's investments in internal manufacturing and technology have given the company greater control of its entire manufacturing process, while also lowering costs. By optimizing packaging solutions for specific application needs, TI can explore new design approaches and technologies while achieving the highest levels of quality and reliability – driving innovation and meeting changing industry demands.

## Additional resources

- Find TI **packages**.
- Learn more about **our innovative approach to packaging**.
- Read the company blog, **The power of packaging**.

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