Simplifying Power Conversion in High-Voltage Systems

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There are a lot of challenges to delivering efficient power conversion in high-voltage applications. However, component, topology and system-level innovations can significantly increase the high-voltage power-conversion system's efficiency and density, while simplifying designs.

At a glance

This white paper examines the challenges of efficient high-voltage power conversion and provides examples of component, topology and system-level innovations that help simplify power-supply designs in automotive and industrial applications.

1 Optimizing wide-bandgap FET performance with component innovations

Wide band-gap field-effect transistors (FETs) offer a higher-efficiency alternative to metal-oxide semiconductor field-effect transistors (MOSFETs) but require specialized companion devices such as isolated gate drivers and digital controllers for optimum performance.

2 Maximizing power density with topology innovations

Selecting the right topology can greatly influence the power density and efficiency of a high-voltage power design.

3 Achieving extreme efficiency targets with system-level innovation

System architecture innovations and control system innovations can help designers achieve higher efficiency and power density.

Power designers have their hands full. Not only do they need to keep up with constant increases in power levels, they also need to find creative ways to continuously improve the efficiency and power density of power supplies. At high voltages, these challenges become more prominent.

Delivering efficient power conversion in high-voltage systems requires an in-depth knowledge of high-voltage components, electrical and magnetic circuit modeling techniques, an understanding of insulation requirements for functional or safety isolation, expertise in electromagnetic compatibility, power-converter control techniques and more.

Simplifying high-voltage power design is a challenging task, but not an impossible one.

Why high voltage?

As the worldwide electrification trend continues to gain momentum, efficient energy transfer at higher power levels becomes an important consideration in today's power electronic systems. Resistive loss (I^2R) is the central factor limiting how much power a power supply can deliver. To improve system efficiency, increasing the voltages used to transmit and deliver power reduces the required current for the same power level and helps minimize losses through heat.

A few examples of high-voltage systems widely applied in today's power networks include residential AC distribution power systems, telecommunication and server power systems, DC microgrids in renewable energy systems, energy storage systems, and electric vehicle (EV) onboard and offboard chargers. As an example, EV batteries are currently 400 V but

increasingly trending toward 800 V in order to enable more instantaneous power transfer to the traction inverter for better acceleration performance.

Although operating under a higher voltage brings system efficiency benefits for power conversion, proper galvanic isolation and insulation are essential to allow a safe human interface. Moreover, a closed-loop system generally requires signal communication across the isolation boundaries. Add to this topology selection, magnetic circuit design, electromagnetic interference considerations, operating modes, thermal management, and layout and control optimizations, and you begin to understand some of the significant design challenges when working with high-voltage systems. Overall, innovations from three key areas – component innovations, topology innovations and system-level innovations – will increase high-voltage power-conversion system's efficiency and density, while simplifying designs.

Optimizing wide-bandgap FET performance with component innovations

Wide-bandgap FETs such as silicon carbide (SiC) MOSFETs or gallium nitride (GaN) FETs offer a higher-efficiency alternative to silicon MOSFETs. Wide band-gap FETs have very low or even not reverse recovered charge (Q_{rr}), as well as lower on-resistance under the same voltage levels as silicon MOSFETs, shown in **Figure 1**.

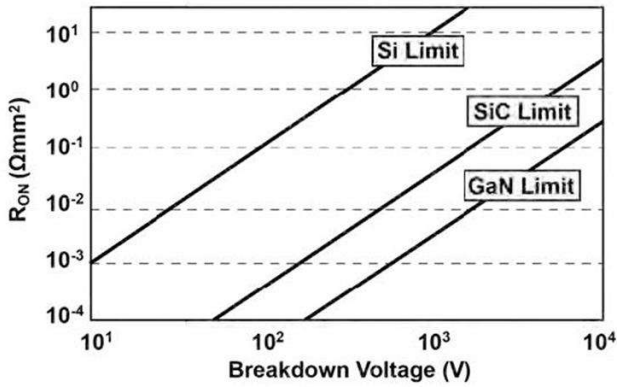


Figure 1. *Theoretical on-resistance vs. blocking voltage.*

In addition, almost all other parasitics including gate charge (Q_g) and output capacitance (C_{oss}) are much lower in wide band-gap FETs than silicon MOSFETs, leading to much faster switching speeds: an over 150-V/ns slew rate compared to a superjunction silicon MOSFET's less than 80-V/ns slew rate. With faster switching speeds, the time it takes for power switches to turn on or off is shorter, and switching losses are reduced.

Selecting the right gate drivers

Because of their electrical properties and the performance they enable, switching to wide band-gap technologies requires a thoughtful approach and careful companion component selection, presenting a completely different set of challenges than designing with silicon. To further minimize switching losses, wide band-gap FETs need an appropriate gate driver capable of rapidly charging and discharging the gate capacitance, since traditional silicon MOSFET gate drivers may not offer proper voltage regulation or be able to handle the high common-mode voltage transient in a wide band-gap design.

As shown in **Figure 2**, when a switching event occurs, the voltage change on the switching node will generate a current flow through the parasitic capacitance of the driver. If the driver does not have enough common-mode transient immunity (CMTI), the common-mode current could cause a gate-driver malfunction, as shown in **Figure 3**.

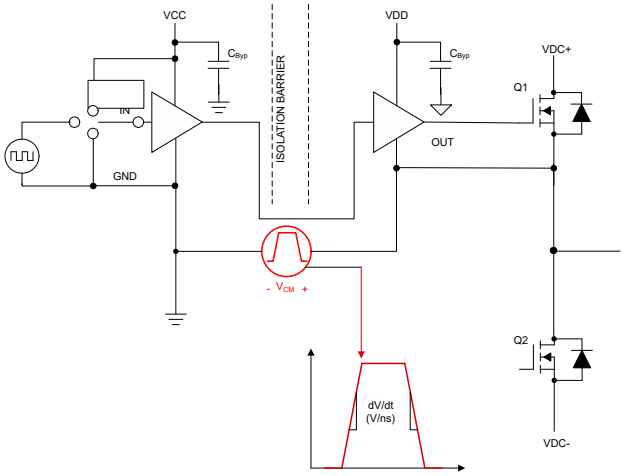


Figure 2. *Common-mode current caused by a switching event.*

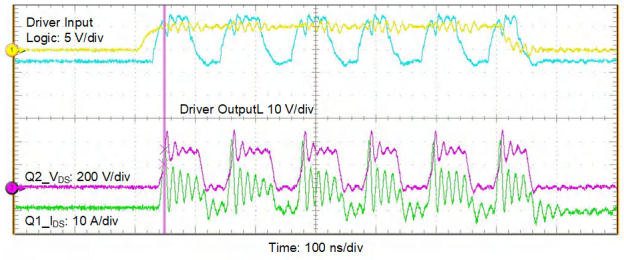


Figure 3. *Gate-driver CMTI failure example.*

To address gate-driver challenges and CMTI concerns, engineers can use new gate drivers with a Miller clamp, a high CMTI rating and adjustable slew-rate features to avoid shoot-through or a gate-driver malfunction. TI's **UCC5880-Q1** reinforced isolated gate driver has as much as 20 A of real-time variable gate-drive strength, a feature that enables you to increase power density and reduce system design complexity and cost while achieving your safety and performance goals. TI's 300-kW DC/AC **High-Power, High-Performance Automotive SiC Traction Inverter Reference Design** demonstrates how to balance efficiency and the challenges discussed here by adjusting driving speeds under different load conditions.

Faster switching means lower switching losses, but it can also lead to unwanted voltage ringing and common-mode noise issues. **Figure 4** shows a GaN FET with a discrete gate driver. There is not only parasitic inductance of the two devices themselves, but also the printed circuit board (PCB) trace inductance of the connection copper. The total inductance on the driving loop will slow the GaN FET V_{DS} transition, therefore limiting the switching losses that the GaN FET can reduce. This is why a TI GaN FET such as the **LMG3526R030** (see **Figure 5**) integrates a gate driver into the same package. With the gate driver integrated, there will be no PCB inductance (L_{g_pcb} and L_{s_pcb}). Also, the Kelvin source connection is made for the gate-drive loop (minimizing L_{cs}); therefore, the TI GaN FET can switch at a high transient voltage, which will minimize switching losses.

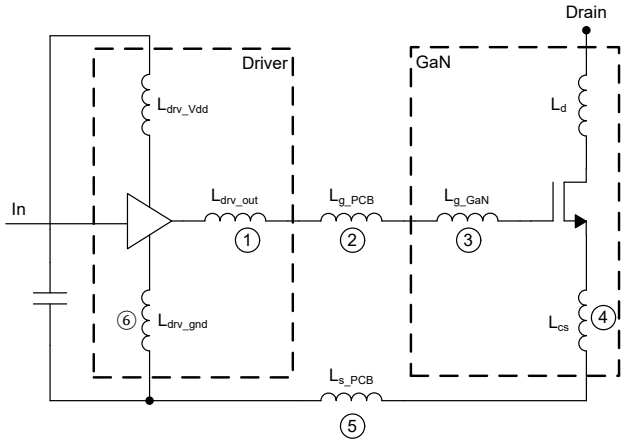


Figure 4. *A GaN FET with a discrete gate driver and parasitic inductance on the loop.*

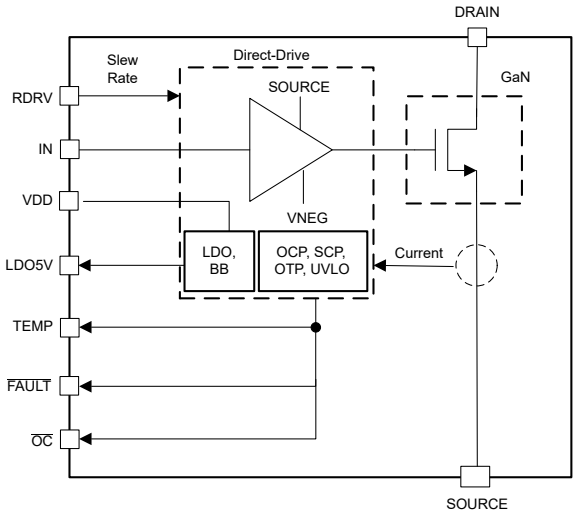


Figure 5. *Simplified LMG3526R030 block diagram.*

Selecting the right controllers

In today's high-voltage systems, magnetic components occupy a large portion of the overall power-conversion stage. To reduce the size of magnetic components, you must increase the operational frequency. What follows is a need for dedicated digital control to manage the diverse high-performance requirements of high-voltage systems. These controllers need to operate in real time, accurately measuring system parameters (such as voltage, current and temperature); applying control algorithms to calculate the output commands; and supporting the high frequencies needed to improve power density. The key to real-time control is to minimize the time between sensing, processing and control functions. Better real-time signal-chain performance results in a faster transient response, more stable and precise power conversion, and higher power density.

One challenge in real-time control is limiting cycling, which refers to the inability of the pulse-width modulation (PWM) output to physically converge on the mathematical solution to the control law. This causes the PWM output to oscillate around the true solution, resulting in instability in the control system. High-resolution PWM (HRPWM) modules on microcontrollers (MCUs) such as **TI's C2000™ real-time MCUs** have the ability to modulate the PWM edge in 150-ps increments. This represents a sixtyfold improvement over traditional PWM creation techniques based off of the system clock rate (see **Figure 6**) and can realize a higher order of accuracy in PWM edge placement. A waveform's period, phase relationship to its complement, and deadband insertion time can all help realize this high-resolution technology.

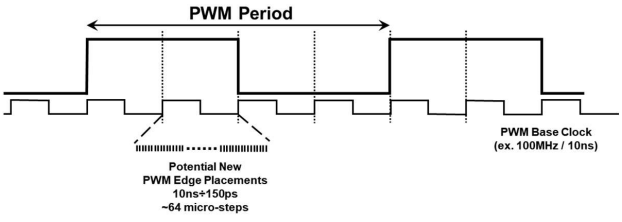


Figure 6. *HRPWM capability vs. traditional PWM generation methods.*

Another real-time control challenge comes with the need for unique fault protection in a three-level inverter topology. Instead of immediately switching all of the FETs off simultaneously in a two-level inverter, for a three-level inverter you must maintain the correct switch-off sequence in order to avoid damaging the FETs. In the past, some designers have used external hardware circuits such as a field-programmable gate array (FPGA) or complex programmable logic device (CPLD) to achieve this level of protection, but these circuits increase system costs and development efforts.

To solve this problem, the C2000 configurable logic block provides a mechanism for creating custom logic inside the chip through software, offering a simpler option to replace the functionality achieved by an external FPGA or CPLD, and helping lower system costs and development effort.

Wide band-gap devices can help greatly increase efficiency and power density – on paper. Without other component innovations such as the isolated gate driver and digital controller, you won't be able to fully realize efficiency improvements in your designs.

Maximizing power density with topology innovations

In addition to component-level innovations, topology innovations can help you simplify power conversion in high-voltage systems. The AC/DC rectifier is a great example of how wide band-gap technologies can elevate well-known topologies to improve power density and reduce design weight. Historically, engineers used a bridge diode rectifier with a capacitor to rectify the AC voltage into the DC voltage, as shown in **Figure 7**.

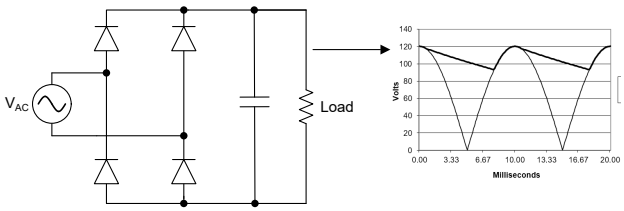


Figure 7. *A full-bridge rectifier.*

The power factor of such a rectifier is generally lower than 0.5, depending on the total impedance of output capacitor and load. This is not energy-efficient, as such a design generates too much unused power (reactive power).

To solve the low-power-factor issue, engineers came up with the idea of an active power factor correction (PFC) circuit. **Figure 8** shows a boost PFC circuit, which generally takes a universal AC voltage (90 V_{AC} to 264 V_{AC}) and boosts the voltage to a regulated 400-V voltage at the output. With input voltage sensing, the controller regulates the inductor current to follow the AC sinusoidal shape to get an almost unity power factor (0.99).

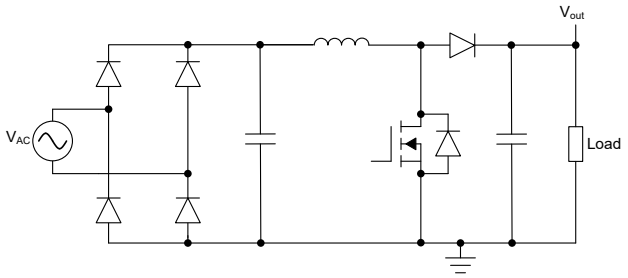


Figure 8. *Boost PFC circuit.*

This type of boost PFC rectifier is able to achieve really high efficiency (>98%) with a superjunction silicon MOSFET and a SiC diode.

The full-bridge diode rectifier in the boost PFC rectifier does consume more than 1% of overall efficiency losses in kilowatt-level high-voltage systems. For example, a more than 20-W loss on a full-bridge diode rectifier is expected in a 2-kW rectifier. It is very difficult to dissipate a 20-W loss from a single device. To reduce losses on the full-bridge diode rectifier, the totem-pole bridgeless PFC shown in **Figure 9** presents a good alternative. Because the rectifier function is integrated with the boost converter and has only two additional MOSFETs (instead of four diodes), the total rectifier loss (with the two low-frequency FETs) is much lower than in the original bridge rectifier example.

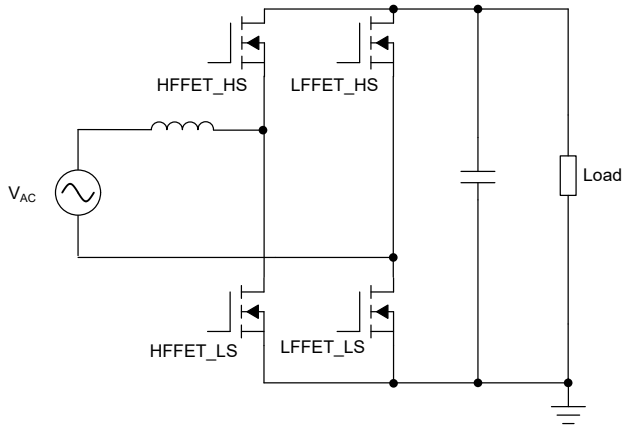


Figure 9. *A totem-pole bridgeless PFC circuit.*

A continuous-conduction-mode (CCM) totem-pole bridgeless PFC is a hard-switching converter, which is widely applied in high-voltage rectifiers. Therefore, if you apply a silicon MOSFET to a totem-pole bridgeless PFC, the silicon MOSFET will suffer from high switching losses caused by Q_{rr}. As shown in **Figure 10**, after the top-left MOSFET body-diode current conduction, Q_{rr} will generate a reverse-recovery current to charge the bottom-left MOSFET C_{oss} during the dead time of the left half bridge. Once the bottom-left MOSFET turns on, the Q_{rr}-induced energy will dissipate into the bottom-left MOSFET. The Q_{rr}-related loss consumes the loss reduction on the full-bridge diode rectifier.

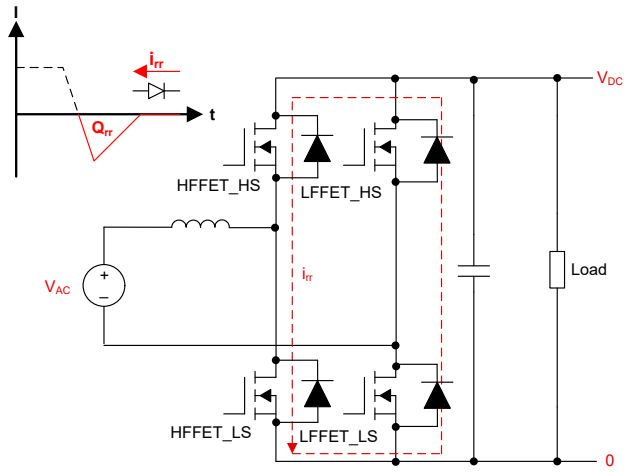


Figure 10. *Switching losses caused by reverse-recovery charge in a totem-pole bridgeless PFC.*

The existence of wide band-gap FETs can, for the most part, help solve Q_{rr}-related loss issues with the new totem-pole bridgeless PFC topology. A SiC MOSFET can achieve a 20 times smaller Q_{rr} than a superjunction MOSFET with the same on-resistance level – and a GaN FET can achieve zero Q_{rr}. When combining component and topology innovations in the rectifier example (in other words, applying wide band-gap FETs with a totem-pole bridgeless PFC), you can achieve over 99% efficiency (a >1% efficiency improvement), unlocking higher power density and lighter weight in your designs.

Achieving extreme efficiency targets with system-level innovation

Today's component and topology innovations enable power-conversion systems with much higher efficiency than ever before. An emerging DC grid system offers a much simpler, more efficient and more reliable high-voltage solution over traditional centralized AC grid systems. For example, a photovoltaic (PV) power system requires only one power-conversion stage from the PV panels to 120-V or 240-V AC grids. A distributed DC grid system could greatly simplify high-voltage power conversion and increase system availability and reliability.

Beyond system architecture innovations, control system innovations are another way to simplify and improve high voltage power-conversion systems. Let's continue using PFC as an example. In high-power applications involving AC, a CCM PFC should be the first choice because it allows a lower inductor ripple current; therefore, you will need a smaller differential electromagnetic interference (EMI) filter. Compared to a CCM PFC, a critical-conduction-mode (CRM) PFC has its PFC inductor current always start from zero or even negative with a smaller inductance, which enables much lower switching losses and higher efficiency, as the current of the power switches at the turnon instant is almost zero. The inductor current ripple will be much higher than a CCM PFC when delivering the same power, however, which can make EMI filter design difficult.

A third option offering the right balance between efficiency and differential EMI noise levels is multimode operation – a combination of CCM and CRM operations in every AC cycle. In multimode operation, the PFC inductor inductance should be smaller than the PFC inductor used in CCM operation but larger than the PFC inductor used in CRM operation in order to allow the PFC to have both CCM and CRM operation over an AC cycle. **Figure 11** illustrates the ripple current envelopes in these three modes.

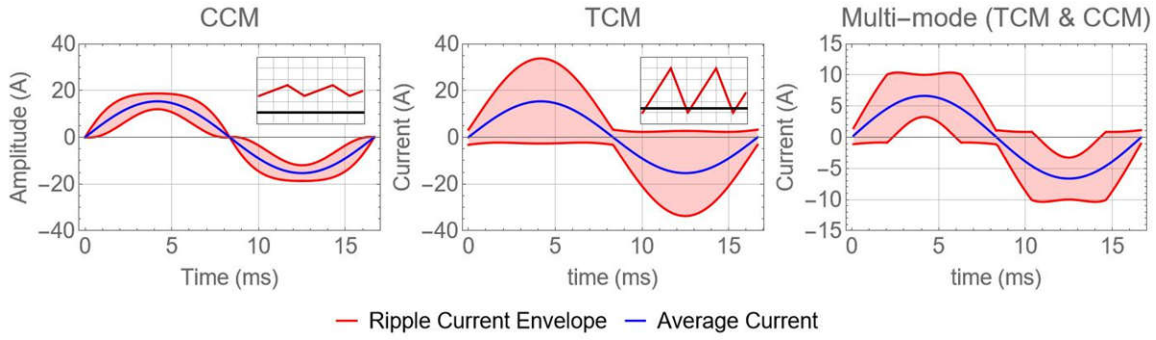
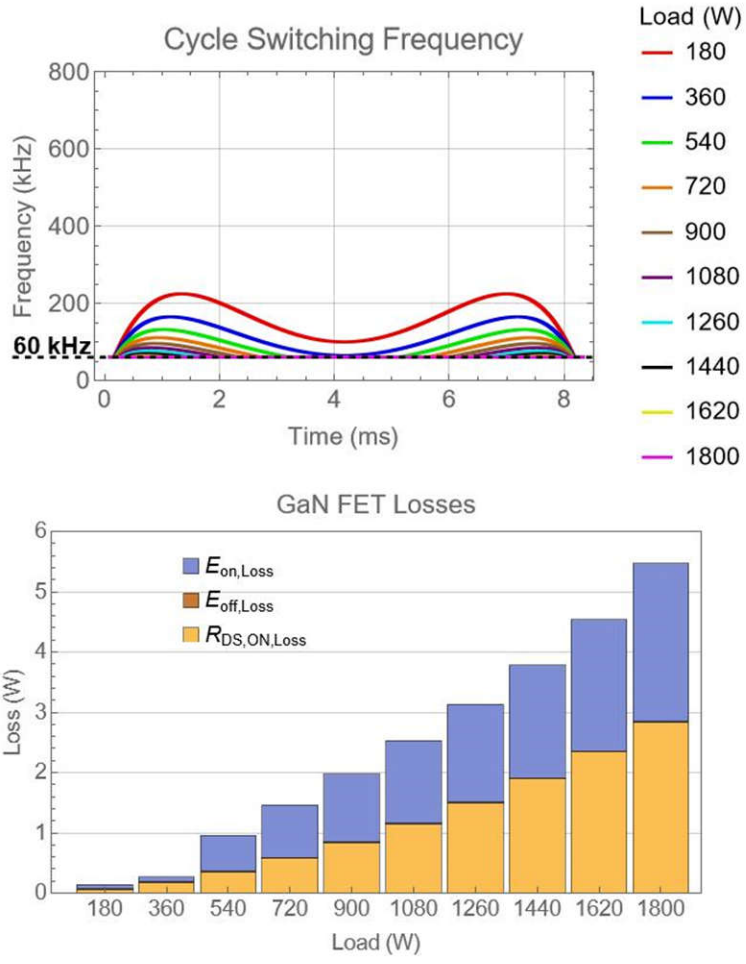


Figure 11. *PFC inductor currents (from left to right) under CCM, CRM and multimode operations.*

Figure 12 shows a loss comparison between a multimode PFC and a CRM PFC (assuming that zero voltage switching is guaranteed) with the same specification. The multimode PFC design has a 150-µH PFC inductor with an operational frequency ranging from 60 kHz to 250 kHz, while the CRM PFC design has a 25-µH PFC inductor with an operational frequency ranging from 75 kHz to 750 kHz. As a result, the CRM PFC reduces FET losses over 40% at a half load, with a higher operational frequency and a smaller inductor. This is an indication of where highly efficient high-voltage power-conversion systems should move – toward adopting soft-switching topologies.



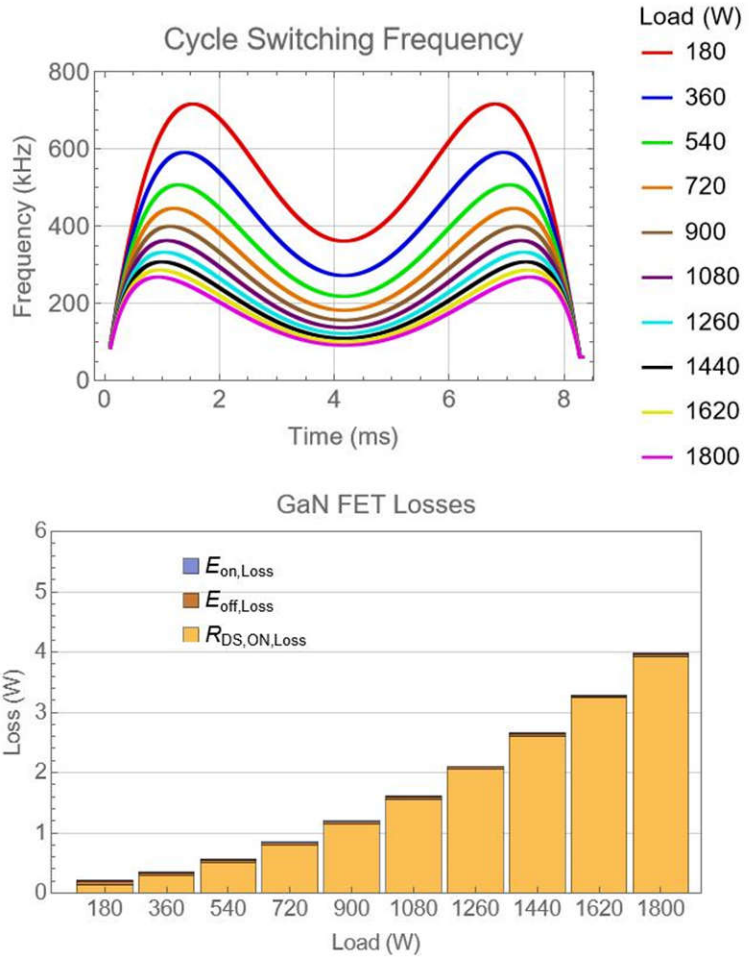


Figure 12. *Frequency spectrum and FET losses in a multimode PFC (left) and a CRM PFC in a 1.8-kW power-supply unit.*

Addressing EMI challenges

Engineers can address EMI filter design challenges by splitting the PFC inductor into two elements: one with the higher-inductance inductor (L_g) connected to an AC source, and the lower-inductance inductor (L_b) in series with a capacitor and placed in parallel with the power stage, as shown in **Figure 13**. The idea of splitting inductor setup is to allow the large AC ripple current to flow through the series inductor and capacitor (lower total impedance) and to minimize the current ripple on L_b (higher impedance) and the AC source. Therefore, EMI filter design becomes easier, as the differential mode noise is lower.

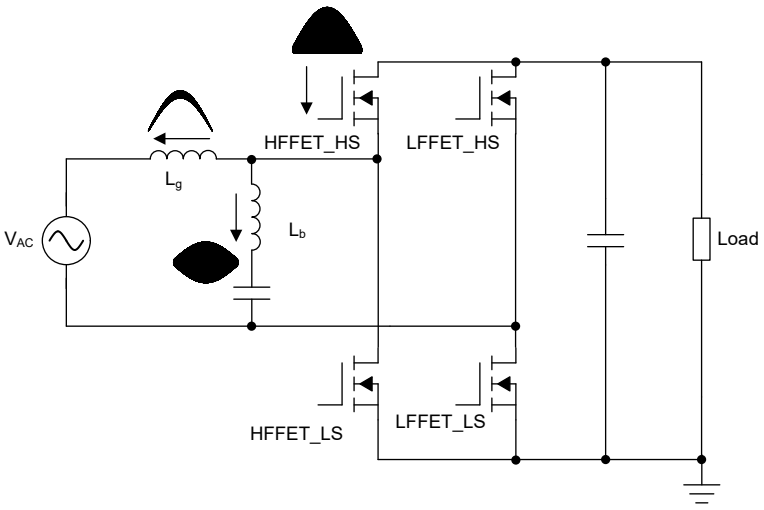


Figure 13. *A modified totem-pole bridgeless PFC circuit.*

Although the modified soft-switching CRM PFC does allow you to overcome EMI filter design challenges, the CRM PFC itself requires additional sensing and control efforts to determine PFC active switch turnon timing in order to ensure soft switching. One option is to add current-sensing devices such as a current transformer to detect the zero current point, which allows you to then calculate active FET turnon timing based on the FET C_{oss}. Propagation delay in sensing and control systems and component tolerance will result in active FET turnon timing errors. Since this control scheme requires cycle-by-cycle sensing and control, you should expect higher MCU resource usage.

An alternative way is to calculate the required FET's on- and off-time based on the input and output voltage-sensing results, along with the PFC inductance and FET C_{oss}. You can then use the FET drain-to-source voltage sensing to determine whether you've achieved soft switching. If the drain-to-source voltage doesn't go negative before the gate signal goes high, it means that the FET is in hard switching.

Take the FETs shown in **Figure 13** as an example, where extending the HFFET_HS on-time allows more negative current to discharge HFFET_LS C_{oss} in order to achieve soft switching. If the drain-to-source voltage goes negative before the gate signal goes high, it means that the FET is already soft switching. Reducing the on-time of HFFET_HS will minimize the root-mean-square current for better efficiency. This way, the FET on-time is no longer updated every cycle but is only adjusting when soft switching isn't occurring, which saves a lot on MCU resource usage.

Integrating the required soft-switching sensing circuit with the FET could further simplify the system. As shown in **Figure 5**, the **LMG3526R030** device integrates a GaN FET, driver, protections and FET drain-to-source voltage sensing into one package. Whenever the GaN FET is in third-quadrant conduction before channel conduction, the LMG3526R030 sends out a zero-voltage detection pulse as an indication of soft switching.

Figure 14 shows example waveforms of the LMG3526R030 with and without third-quadrant conduction.

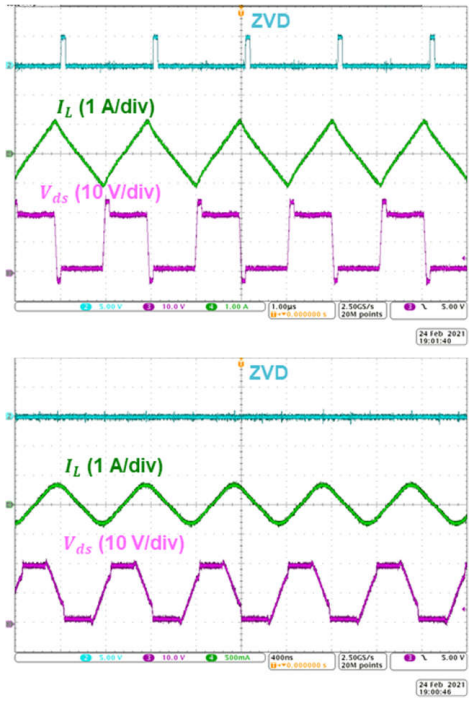


Figure 14. *Waveform of the LMG3526R030 with (upper one) and without third-quadrant conduction.*

Using the zero-voltage detection feature in **LMG3526R030**, The **Variable-Frequency, ZVS, 5-kW, GaN-Based, Two-Phase Totem-Pole PFC Reference Design** has demonstrated over 99.1% peak efficiency by combining component, topology and control system innovations.

Conclusion

Today, it is much easier to design high-voltage power-conversion systems than it was a decade ago, but with new technologies come new challenges. There won't be a single-point breakthrough to bring us a revolutionary high-voltage system – every piece of the design has to evolve together to help engineers maximize the efficiency, power density and performance of high-voltage systems.

TI's high-voltage power conversion technologies, spanning GaN ICs, isolated gate drivers, isolated DC/DC converters and modules and C2000 real-time microcontrollers, take advantage of component, topology and system-level innovations to simplify the design of high-efficiency, high-power-density, high-voltage power conversion systems. To learn more about TI's high-voltage technology, see the **TI.com/highvoltage**.

Additional resources

- **Gallium nitride (GaN) ICs**
- **Isolated gate drivers**
- **Isolated DC/DC converters and modules**
- **C2000 real-time microcontrollers**

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