Achieving Fast Load-Transient Response and Low EMI With the AECM DC/DC Control Topology

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No single control topology is a good fit for all applications. Designers requiring low electromagnetic interference (EMI) and fast load- transient response should consider advanced emulated current mode (AECM) – a new, constant-frequency and inductor-based control topology with smart loop-bandwidth control.

At a glance

1 What is AECM control?
AECM is a control topology based on a fixed-frequency modulation with emulated current information for the loop control.

2 PCM
PCM is a popular fixed-frequency control topology for DC/DC converters given its overload protection, accuracy and ease of compensation.

3 D-CAP2 control scheme
The D-CAP2 control scheme is a variation of adaptive COT control with an emulated ramp-generator circuit integrated inside the IC.

4 AECM control benefits
AECM control topology can help engineers simplify EMI filter design with fixed frequency and supports wide- output, large-duty-cycle applications with good load-transient performance

5 How AECM control works
AECM control offers mode-detection block to identify whether the DC/DC converter is in PWM mode or PFM mode. Its integrated oscillator generates the fixed clock in PWM mode, enables on-time generator and adjusts DC gain to achieve high bandwidth.

What is AECM control?

There are many types of control topologies addressing specific design challenges for non-isolated switching DC/DC converters and controllers [1], including peak current-mode control (PCM), voltage-mode control, constant on-time (COT) control, D-CAP2™ control topology and all of their derivatives. In accordance with the implementation of duty cycle, it is possible to separate these control topologies into two categories: the pulse-width modulation (PWM) technique and the pulse-frequency modulation (PFM) technique.

The PWM technique is common in DC/DC converters used to power communications, audio and automotive equipment. It has a fixed and predictable switching frequency, which is convenient when designing the output filter for low electromagnetic interference (EMI).

The PFM technique is common in DC/DC converters used to power digital applications such as graphic engines, memory, digital signal processors and field-programmable gate arrays because of its fast load-transient response. Control topologies do affect DC/DC converter design and may vary based on system-level requirements such as ripple, solution size, load-transient response, fixed frequency and light load efficiency. No single control topology is a good fit for all applications.

In this white paper, a constant frequency and inductor current-based control topology is introduced with smart loop-bandwidth control called advanced emulated current mode (AECM). This new control topology

combines the benefits of PFM and PWM techniques, showing a fast load-transient response with a true fixed switching frequency operation. AECM can help enhance the performance of applications currently using both the PCM and PFM techniques.

PCM

PCM is a popular fixed-frequency control topology for DC/DC converters given its overload protection, accuracy and ease of compensation. **Figure 1** iillustrates PCM control of a buck converter
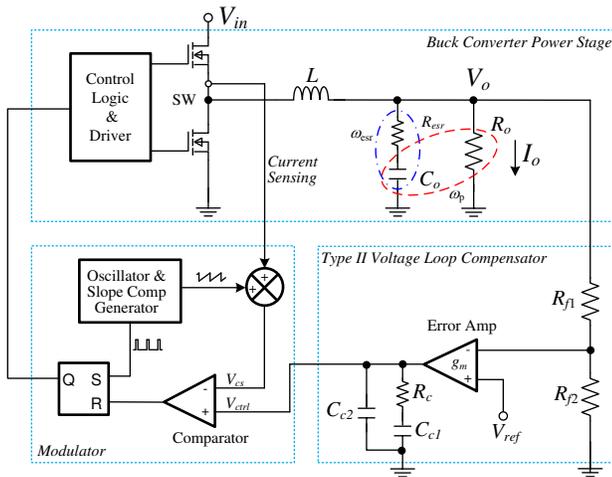

Figure 1. PCM control scheme block diagram.

The power stage consists of the power switches and output filter. The compensation block includes the output voltage divider network, error amplifier, reference voltage and compensation components. The pulse-width modulator uses a comparator to compare the inductor current information with the slope compensation ramp to the error signal, creating an output pulse-train that has a width controllable by the level of the error signal.

As shown in **Figure 2**, the internal clock initiates one pulse, and the high-side field-effect transistor (FET) turns on, with current increasing in the inductor. When the sensed current reaches the control voltage, the high-side FET turns off and the low-side FET turns on until the next rising edge of the clock. The next PWM pulse is generated at the next clock pulse. Thus, the switching frequency depending on the clock is truly fixed.
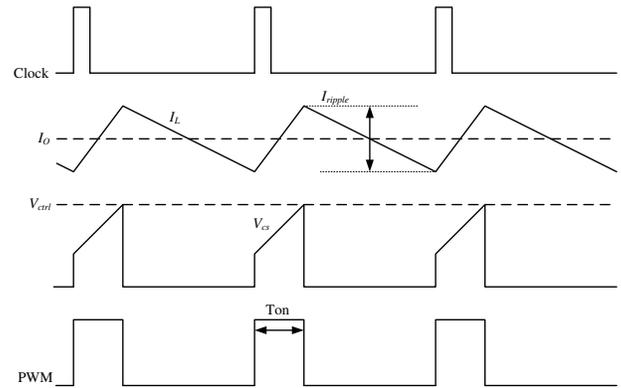

Figure 2. PCM control scheme waveform.

PCM control introduces one inner current loop, which transforms the inductor into a voltage-controlled current source. The power stage can be approximated as a current source feeding the parallel combination of the output capacitor and the load resistor, and produces a single low-frequency pole. The power stage also consists of a higher-frequency zero set by the output capacitor and its equivalent series resistance (ESR). Type-II compensation normally introduces one zero and one pole to compensate the output pole and output zero.

Engineers designing with traditional PCM control devices prefer external compensation to achieve good loop performance for wide output-voltage- range applications. However, external compensation complicates loop design and requires more external components. To simplify the design, a growing number of integrated circuit (IC) manufacturers have developed internally compensated PCM control devices that integrate Type-II loop compensation with R_c, C_{c1} and C_{c2}. R_c and C_{c1} generate a fixed internal zero to compensate the output pole, while R_c and C_{c2} produce a fixed internal high-frequency pole to compensate the output zero. Both the effective output capacitance and load resistance have an impact on the output pole, however. In order to support a wide output-voltage range or wide output-capacitance range, you must set the fixed internal zero relatively low to get good stability. What's more, the cross-frequency (f_c) of PCM control is designed to meet $f_{sw}/10 < f_c < f_{sw}/5$. Therefore, the error amplifier introduces some delay, which limits the load-transient response.

PCM also has these drawbacks:

- The lower the output voltage, the lower the load resistance under a certain output current. Getting the output pole close to the fixed internal zero requires a large output capacitance, resulting in a higher bill-of-materials cost.

- Some PCM devices that clamp the control voltage to achieve high efficiency at a light load may face multipulse issues, resulting in a large output ripple.

D-CAP2 control scheme

The D-CAP2 control scheme is a variation of adaptive COT control with an emulated ramp-generator circuit integrated inside the IC. This control scheme is popular in buck converters because of its simplicity and improved load-transient performance. **Figure 3** shows the block diagram for D-CAP2 control of buck converters, while **Figure 4** shows the corresponding control waveforms.

The ramp generator (ripple injection generator) emulates the inductor current information and brings this information back to the comparator. When the emulated ramp voltage and feedback voltage are lower than the reference voltage, the comparator output goes high to initiate an on-time pulse. The width of the on-time pulse (T_{on}) is constant, since it is calculated by the adaptive on-time generator based on the input voltage, output voltage, output current and frequency setting. The off-time relies on the voltage ripple, which has some variation during a line or load transient. As a result, the switching frequency is pseudo-fixed. During the on-time, the high-side FET turns on and the inductor current increases to charge the output voltage. After the on-time, the high-side FET turns off and the low-side FET turns on. The output voltage goes down until the generation of the next on-time pulse. Because D-CAP2 control topology does not integrate an oscillator or clock, the on-time may be affected by a propagation delay from logic to driver, resulting in poor jitter performance. That is the main reason why it is not easy for IC

manufacturers to design high-switching-frequency buck converters (2.1 MHz) with D-CAP2 control topology. Additionally, there are different offset voltages of the emulated ramp-generation circuit under different load conditions, resulting in poor output-voltage accuracy.
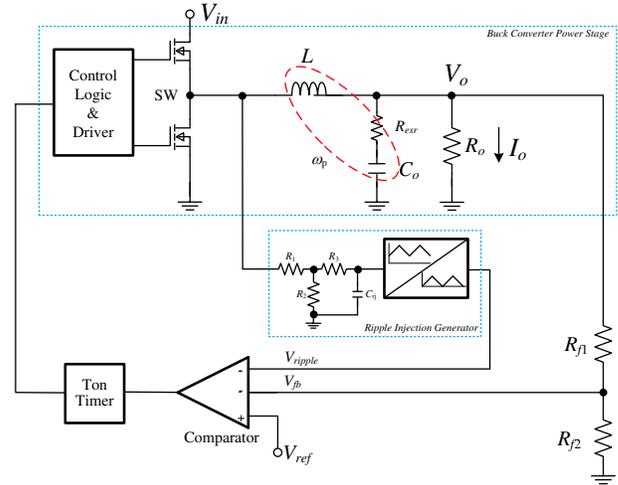

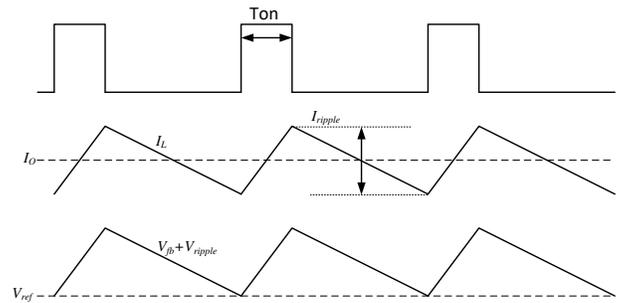*Figure 3. D-CAP2™ control scheme block diagram.*

Figure 4. D-CAP2 control scheme waveform.

The D-CAP control topology requires some ripple on the output where low ESR capacitors can become a problem. That's why engineers need D-CAP2 control. There is some limitation to the internal emulated ramp-generator circuit of the D-CAP2 buck converter as well, so the traditional D-CAP2 buck converter can only support an output up to 7 V. There is a minimum off-time requirement as well because of the valley voltage detection; thus, D-CAP2 control is not recommended for large duty-cycle applications.

Reference [2] proposed an open-loop transfer function of the D-CAP2 control topology. **Figure 5** shows the

corresponding Bode plot. The emulated ramp-generation block introduces one internal zero, which can eliminate the double pole set by the output inductor and capacitor, thus making the gain plot crossing the horizontal line 0 dB with a slope of –20 dB per decade, and boosting the phase margin at the crossing frequency. **Equation 1** expresses the DC gain of the open-loop transfer as:

$$G_{open}(0) = A_{cp} \times H_{FB}(0) \times A_{cp} \times \frac{V_{ref}}{V_{out}} \qquad (1)$$

where, $A_{cp} = \dfrac{(R_1 + R_2)}{R_2}$

Since A_{cp} and V_{ref} are constant, the DC gain is an inverse proportional of V_{OUT}. As shown in **Figure 5**, if $V_{OUT1} > V_{OUT0} > V_{OUT2}$, then the DC gain trend is Gain1 < Gain0 < Gain2. For a certain device, the internal zero is fixed. Assuming that the double pole for different outputs is the same, the bandwidth trend is $f_{BW1} < f_{BW0} < f_{BW2}$. Therefore, for a D-CAP2 buck converter, a higher output voltage would have a lower bandwidth.
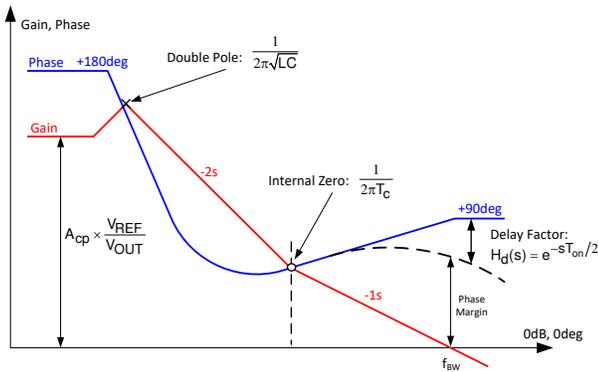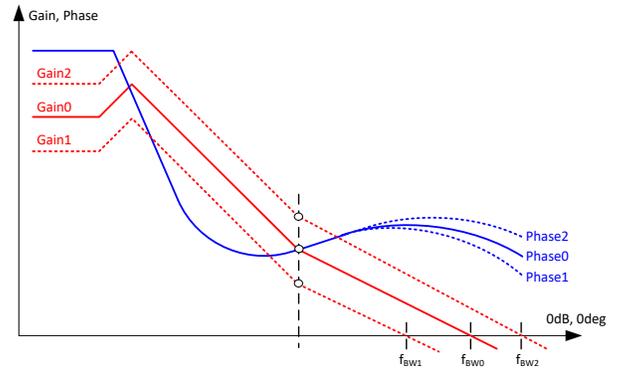

Figure 5. Bode plot with different VOUT conditions of a D-CAP2 buck converter.

Since A_{cp} and V_{ref} are constant, the DC gain is an inverse proportional of V_{OUT}. As shown in **Figure 6**, if $V_{OUT1} > V_{OUT0} > V_{OUT2}$, then the DC gain trend is Gain1 < Gain0 < Gain2. For a certain device, the internal zero is fixed. Assuming that the double pole for different outputs is the same, the bandwidth trend is $f_{BW1} < f_{BW0} < f_{BW2}$. Therefore, for a D-CAP2 buck converter, a higher output voltage would have a lower bandwidth.

Figure 6. Bode plot with different VOUT conditions of a D-CAP2™ buck converter.

Additionally, because the duty cycle cannot change with COT control, the on-time generator will produce a delay factor in the loop, causing a phase drop at high frequency. A larger duty cycle means a longer on-time, resulting in a bigger phase drop.

AECM control benefits

AECM is a new topology based on a fixed frequency modulator with emulated current information for the loop control, combining the fixed frequency of PCM control and the fast load-transient response of the D-CAP2 control topology. The key features and benefits of AECM include:

- True fixed-frequency modulation that can simplify EMI filter design and make it easy to achieve high-frequency modulation such as 2.1 MHz.

- An emulated ramp-generator circuit with smart loop-bandwidth control that can adjust the DC gain smartly, supporting wide-output and high-duty-cycle applications with good load transient performance.

It is possible to simplify AECM control for a buck converter, as shown in **Figure 9**. There are two basic operation modes, PWM mode and PFM mode, selectable by the mode-detection block. The integrator in the voltage loop can improve output-voltage accuracy issues. The integrated oscillator generates the fixed clock. Implementing slope compensation in the modulator avoids subharmonic oscillation when the duty cycle is higher than 50% in PWM mode. The emulated

ramp generator with the smart loop-bandwidth control circuit can adjust the DC gain to achieve high bandwidth over all output rails. And even though there is an integrator, unlike PCM control, the integrator in AECM control can improve output-voltage accuracy with no direct impact on loop response speed.
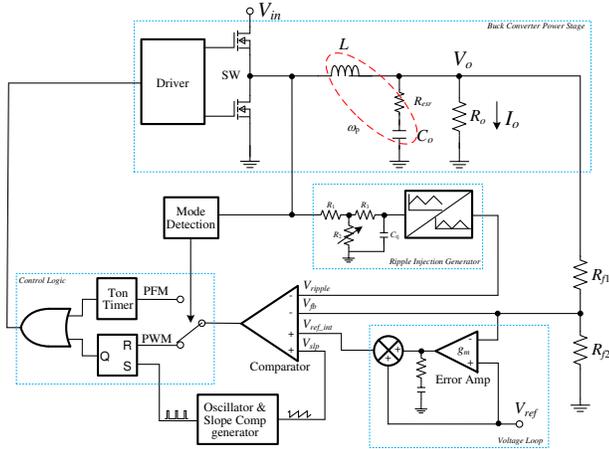

Figure 7. AECM control block diagram.

How AECM control works

The PWM mode control scheme is similar to PCM control. As shown in **Figure 8** on the following page, the internal clock initials one on-pulse; the high-side FET then turns on, with current increasing in the inductor. When the emulated ramp voltage, feedback voltage and slope compensation voltage reach the integrated reference voltage, the high-side FET turns off and the low-side FET turns on until the next clock cycle. Therefore, in PWM mode, the switching frequency is truly fixed.
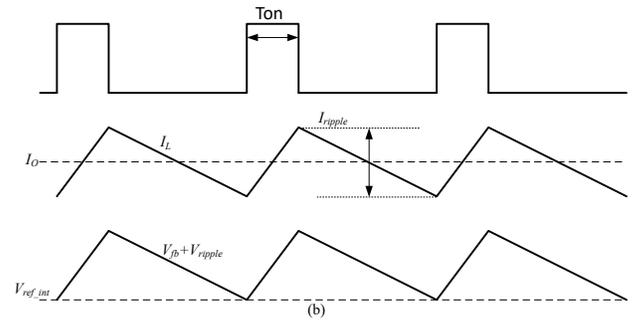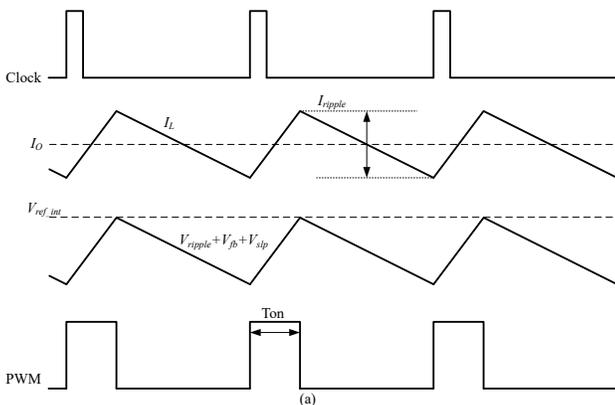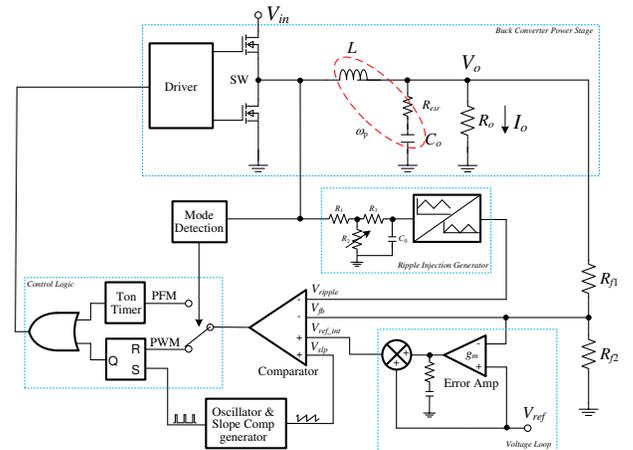

Figure 8. AECM control scheme waveform: PWM operation mode (a); PFM operation mode (b).

Figure 9 shows the load-transient behavior of the AECM device. The duty cycle increases or decreases with a decrease or increase of V_{OUT}.

PWM operation mode

The PWM mode control scheme is similar to PCM control. As shown in **Figure 10**, the internal clock initials one on-pulse; the high-side FET then turns on, with current increasing in the inductor. When the emulated ramp voltage, feedback voltage and slope compensation voltage reach the integrated reference voltage, the high-side FET turns off and the low-side FET turns on until the next clock cycle. Therefore, in PWM mode, the switching frequency is truly fixed.

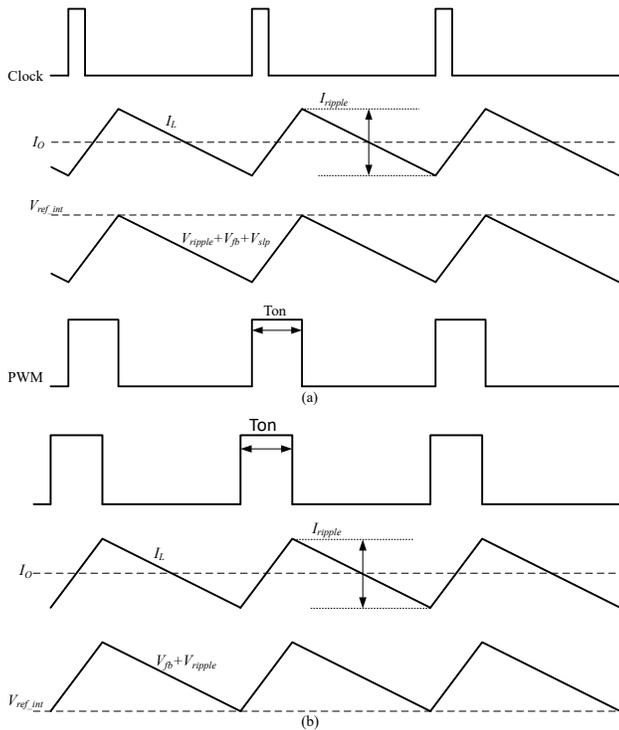*Figure 9.* AECM control block diagram.

Figure 10. *AECM control scheme waveform: PWM operation mode (a); PFM operation mode (b).*

Figure 11. *Duty-cycle changes with the load current: load step-up (a); load step-down (b).*

Figure 11 shows the load-transient behavior of the AECM device. The duty cycle increases or decreases with a decrease or increase of V_{OUT}.

PFM operation mode

AECM control implements PFM mode to achieve high efficiency under light loads. With a load current decrease, the device enters into discontinuous conduction mode (DCM) from continuous conduction mode (CCM). In both modes, the switching frequency is fixed; the width of the on-pulse (T_{on}) depends on the load current. Lighter loads have a shorter T_{on}. AECM has an on-time generator like the D-CAP2 control topology, but that generator is disabled in PWM mode. With the load current further decreasing, the Ton decreases down to the internal clamped on-time, while the AECM device steps into PFM mode with the internal clock blocked and the on-time generator enabled. As shown in **Figure 10**, the control scheme of PFM mode issimilar to the D-CAP2 control scheme. **Figure 11** on the following page shows the transition waveform between PWM mode and PFM mode.
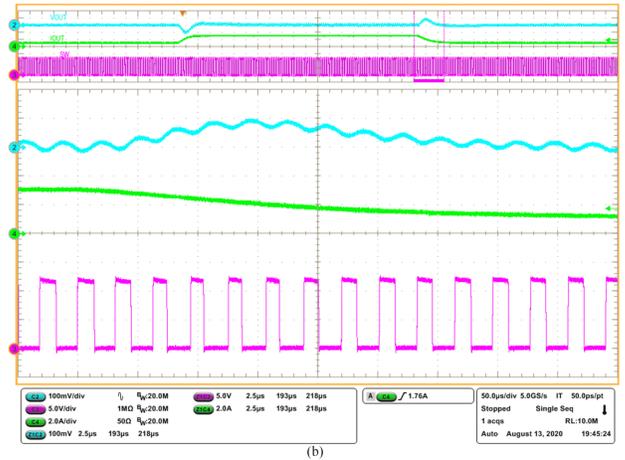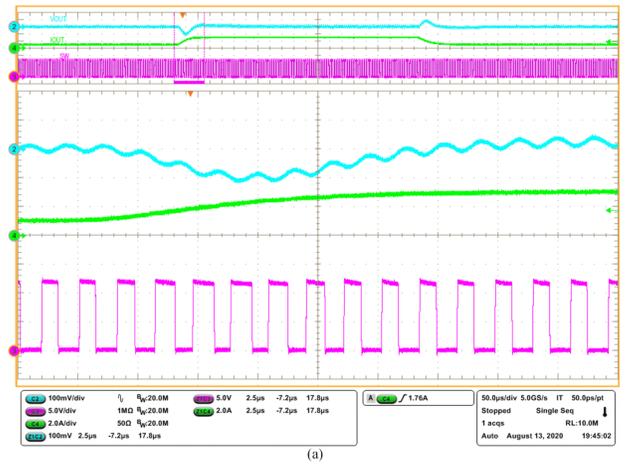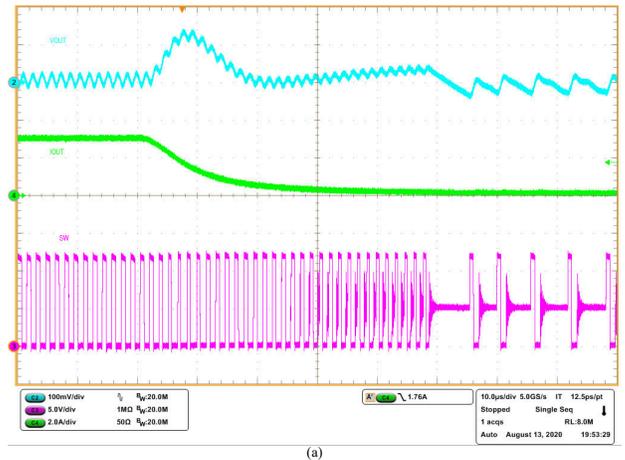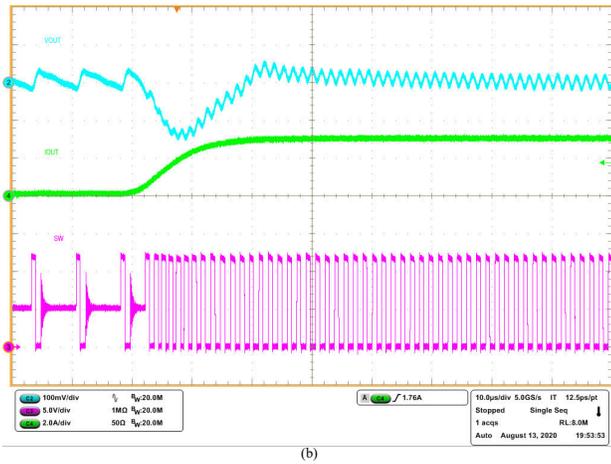
(b)

Figure 12. *Transition waveform between PWM mode and PFM mode of AECM: PWM mode to PFM mode (a); PFM mode to PWM mode (b).*

Smart loop-bandwidth control

Unlike PCM control, where direct inductor current information is in the loop, AECM uses emulated inductor current information. The output filter of AECM control introduces one double pole like the D-CAP2 control topology. Thus, the Bode plot of AECM control is similar to the D-CAP2 control topology.

In D-CAP2 control, the A_{cp} is constant and the DC gain of the open-loop transfer function changes with V_{OUT}. While in AECM control, the A_{cp} adapts to the

changing value of R_2 per the V_{OUT} setting to keep the $A_{cp} \times V_{OUT}$ a constant value for a fixed DC gain. As shown in **Figure 13**, assuming that the double poles for different outputs are the same, the loop bandwidths under different outputs should be much closer to each other when compared to the loop bandwidths of D-CAP2 control.
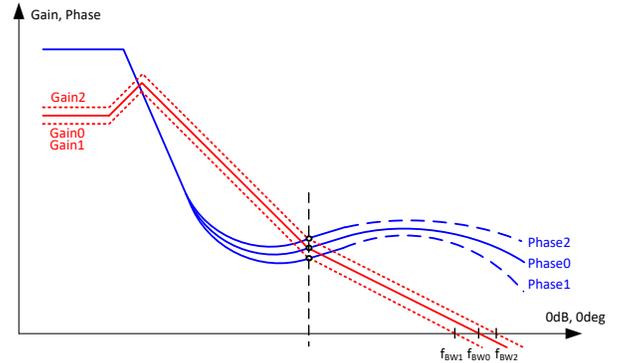

Figure 13. *Bode plot under different V_{OUT} conditions of AECM.*

Figure 14 shows the measured Bode plot of AECM control under different VOUT conditions. The DC gains are almost the same. The crossing frequency and phase margin have slight differences because of the output double-pole shift.
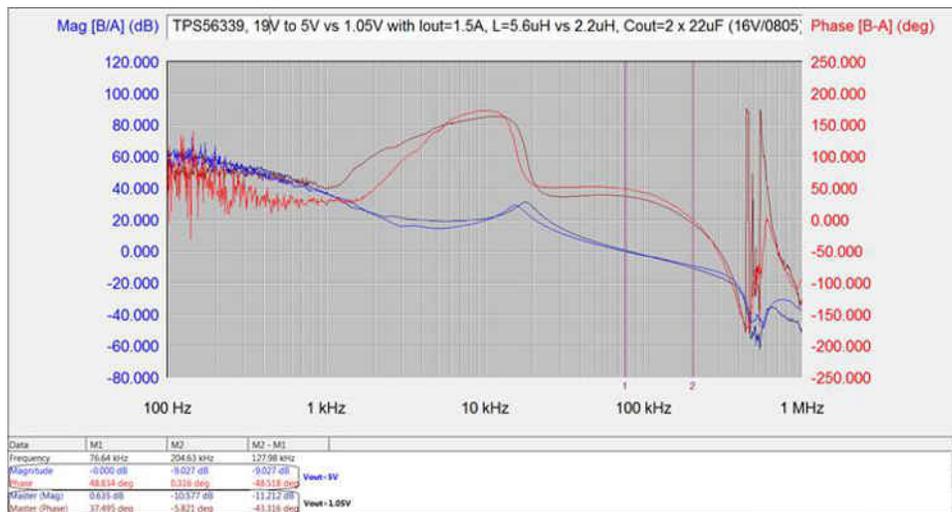

Figure 14. *Measured Bode plot of 5-V and 1.05-V outputs.*

	Traditional PCM Buck Converter (internal compensation)	AECM Buck Converter
Load-transient response	• Slow • The fixed internal zero is set relatively low. • Error amplifier delay.	• Fast • Smartloop-bandwidth control provides a relatively high internal zero. • No error amplifier delay.
Light load pulse	• Single or nonsingle. • Pulse controlled by the clamping control voltage.	• Single • Pulse controlled by the on-time under PFM operation mode.
Wide output stability	• Difficult • The fixed and relatively low internal zero makes it hard to support a wide output range.	• Easy • Smartloop-bandwidth control provides an adjustable bandwidth.

Table 1. Comparing PCM and AECM buck converters.

	D-CAP2 Buck Converter	AECM Buck Converter
Frequency	• Pseudo-fixed and hard to support high frequencies. • Frequency depends on the on-time generator, resulting in a large frequency variation.	• Truly fixed and easy to support a high frequency. • The frequency depends on the internal clock, resulting in a small frequency variation.
High V_{OUT}	• Less than 7 V • Limitation from the internal emulated ramp-generator circuit.	• Higher than 7 V • Improved internal emulated ramp-generator circuit and smart loop-bandwidth control.
Large duty cycle	• Difficult • Limitation from the internal emulated ramp-generator circuit. • Requires a long minimum off-time.	• Easy • Improved internal emulated ramp-generator circuit and smart loop-bandwidth control. • Requires a short minimum off-time. • On-time extension function.

Table 2. Comparing D-CAP2 buck converters and AECM buck converters.

Conclusion

Devices with the AECM control topology for DC/DC converters can achieve a fast load-transient response with a true fixed frequency, while maintaining a wide output voltage and low design cost. This new control topology has been implemented in several products with good performance, ease of use and small solution size.

References

1. Texas Instruments: *Control-Mode Quick Reference Guide: Step-Down Non-Isolated DC/DC*
2. Texas Instruments: *Optimize Output Filter on D-CAP2™ for Stability Improvement*

Additional Resources

- *Choosing the Right Fixed Frequency Buck Regulator Control Strategy*
- *Choosing the Right Variable Frequency Buck Regulator Control Strategy*

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