

Simple power-rail sequencing solutions for complex multi-rail systems



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Configurable power-rail sequencing techniques allow system designers using a single power management solution to address different processor-based applications.

Sequencing and monitoring of multiple power rails is one of the most critical power-management issues facing multicore processor applications in the consumer, automotive and industrial domains today. The latest families of multicore application processors need support for multiple peripherals, such as the dynamic random access memory (DRAM) controller, media/graphics co-processor, and many others.

As a result, power-management functions must be complex enough to handle the sequencing and monitoring requirements of the increasing number of peripherals and processor cores populating today's system platforms. Also, power management integrated circuit (PMIC) solutions should have enough configuration flexibility to minimize the number of hardware and software changes necessary during system development to decrease costs and reduce design delays when introducing new products.

Introduction

Power supply sequencing is an essential part of any design requiring power management. This sequencing is most critical in complex systems that use multiple power rails. For example, devices such as application-specific integrated circuits (ASICs), field programmable gate arrays (FPGAs) and microprocessors require multiple voltage rails just to power the memory, the core, and the input-output (I/O) (**Figure 1**). The main requirement is to have a very specific and deterministic voltage rail power-up and power-down sequencing.

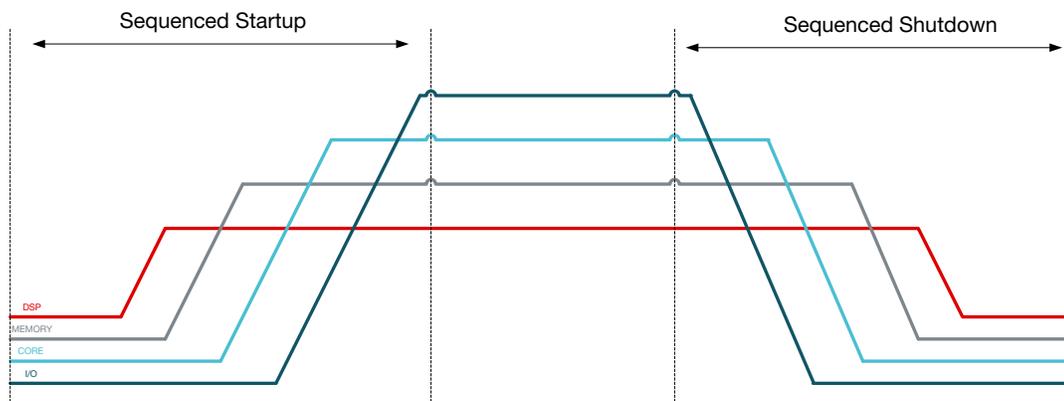


Figure 1. Power-up and power-down sequencing.

Determining whether or not a voltage rail is powered on or off in the correct order, with respect to the other rails and whether or not a voltage rail is within an operating regulating window, is critical to operational safety and reliability.

This paper discusses methods for configuring flexible sequencing of multiple power supply systems, along with the advantages and disadvantages of each when applied to different systems.

Why “power rail” sequencing is critical?

Other than causing problems at the system level, incorrect power sequencing can also cause problems at the semiconductor level. For example, an unexpected reverse bias across a complementary metal oxide semiconductor (CMOS) device [1] can damage the device or latch it into an erroneous state. Often these erroneous states can be released only by power-cycling the device. A workaround might be to use blocking diodes to latch-up [2] as they can limit the usable voltage range for analog input and, hence, correcting the supply voltage start-up sequencing, which is the preferred solution. Sometimes, multiple voltage semiconductor devices, such as microprocessors, often require their input/output (IO) voltage to be present before applying the core voltage. On a system level, for example, a central processing unit (CPU) must be powered-up before the graphic integrated circuits (ICs) to prevent uncontrolled outputs to the graphic display. Additionally, sequencing the supplies helps to stagger the inrush current during power-up.

PMIC central monitoring

Monitoring of power rails has become much more difficult due to power supply sequencing and the sharp increase in the numbers of power rails. Consider a system with 12 voltage rails that require a complex power-up and power-down sequence.

In addition to the undervoltage lockout (UVLO) and thermal shutdown, each rail must be monitored for undervoltage, overvoltage, overcurrent, and short-circuit faults. During a fault event, all voltage rails should be turned off, or a deterministic power-down sequence should be initiated – depending on the kind of failure. Fault flags must be generated depending on the status of the power supplies, if they are within or outside of regulation.

Configurability and flexibility are key

Flexibility is the key to successfully navigating a project from prototype to production. When a key FPGA or processor is in development, the supply voltage levels or sequencing requirements may change as silicon revisions are shipped. The ideal PMIC solution should minimize the hardware and software iterations during development.

PMICs need to be able to support multiple sequencing requirements for multiple applications through non-volatile memory (NVM) spins. Imagine a power management device that can be reprogrammed in a few minutes to account for a new sequencing requirement, versus having to physically change components on the board or, worse still, having to redesign the hardware. In summary, sequencing flexibility and configurability avoids device spins, saves costs and reduces time-to-market.

Sequencing techniques

There are many approaches to power sequencing. The techniques identified in this paper are mostly logic-based. In a logic-based approach the system uses the enable pin or other logic pins on the power devices, rather than controlling the power to them. Using the integrated logic pin in a PMIC provides a simpler, more compact and lower-cost solution.

1. RC-based sequencing

In a resistor-capacitor (RC) based approach, sequencing is done by using the enable pins on each voltage rail (VR). By looping back the output voltages

of the preceding rail to the enable input of the following rail, the VRs can be staggered. Small RC-based delay circuits can be implemented to generate timing delays for enabling the next VR, if required. As shown in **Figure 2**, the output of power supply 1 is looped back with an RC-delay circuit to delay the enabling of power supply 2. This achieves a power-up sequencing of power supplies 1 and 2.

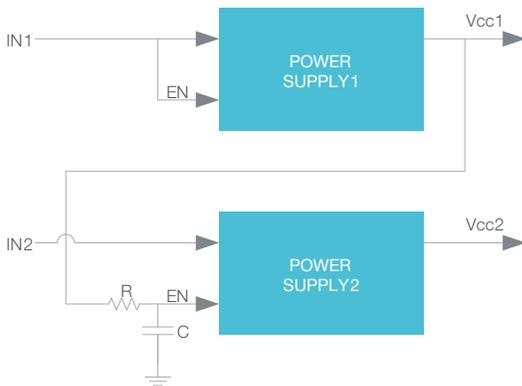


Figure 2. RC- based delay sequencing.

Using the RC-based sequencing approach has many limitations when it comes to cost and complexity. You have a high overhead due to external components and board area cost. While you can have a power-up sequence, you will have difficult and limited options for power-down. When accuracy is required in terms of

inter-rail delays, the RC-based delay approach does not suffice, and does not offer any kind of mechanism to easily deal with faults. Ideally, a fault in any VR should be able to turn off other VRs to prevent the power solution from damaging the system. There is no orderly power-down sequence when a fault is detected. In summary, this approach fails when complex sequencing and monitoring is required. This type of solution is not easily configurable as RC components must be replaced every time new sequences/delays are required.

2. GPIO sequencing

In a general-purpose input/output (GPIO) based approach, single or multiple VRs can be assigned to a specific GPIO and can be function of the power goods (PGs) of other VRs through programmable settings. Voltage rails can be staggered using programmable delay bits, as shown in **Figure 3**. These programmable delay bits will decide the delay from GPIO going high to VR being enabled, or GPIO going low to VR being disabled. For example, VR1, VR2 and VR3 can be assigned to GPIO1 with a 2-millisecond (ms), 4-ms or 6-ms programmable delay setting for powering down. When the GPIO1 goes high, VR1, VR2 and VR3 will be staggered 2-ms apart, both during power-up and power-down. The programmable settings can be stored in non-volatile memory on the PMIC.

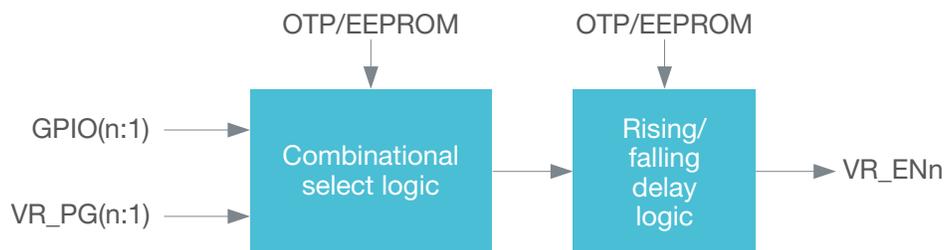


Figure 3. GPIO-based sequencing block diagram.

The GPIO-sequencing approach has only a few limitations. The main one is cost because GPIO pins cost more. Moreover, the system requires an external controller to toggle GPIO pins either high or low. There is logic redundancy. For example, delay counters needed to stagger rails will be replicated for every VR. There will not be any down-sequencing, if required, when a fault or system reset occurs.

3. Serial communication-based sequencing

A serial communication-based approach, used for inter-IC [I²C] and/or serial peripheral interface [SPI], is simple. Here the main controller/processor can enable/disable rails on the PMIC through an I²C or SPI in any order required for powering the system up or down. However, this approach has a major limitation in that the main controller/processor must be powered-up in a definite state to communicate through an I²C/ SPI

before the VRs are powered-up. Generally, this is not the case because the controller/processor may be dependent upon the PMIC to supply the necessary power. Additionally, the shutdown sequence is not guaranteed during faults and resets should something go wrong with the controller/processor.

4. Strobe/time-slot-based sequencing

With strobe/time-slot-based sequencing, the sequencer state machine in the PMIC generates multiple strobes (STROBE1 ... STROBE7 – see **Figures 4-5**) separated by a programmable delay (DLY1 ... DLY6) during power-up and power-down. Through programmable register bits, setting any VR can be assigned to any strobe (**Figure 4-5**), giving complete flexibility in terms of sequencing delay and order. All of the programmable register bit settings are stored on the non-volatile memory (NVM) chip.

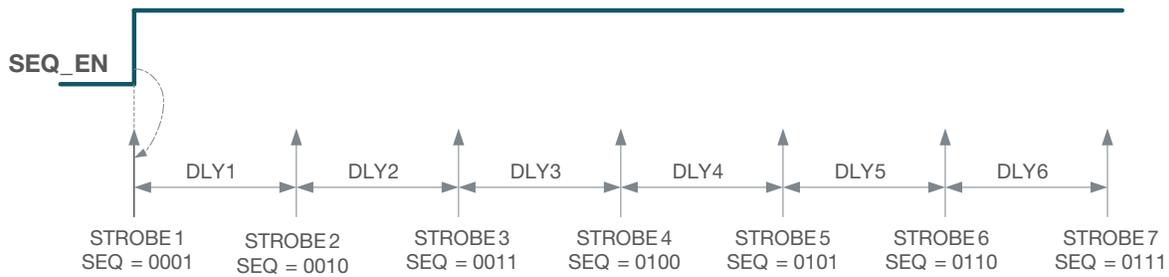


Figure 4. Time slot based up sequencing.

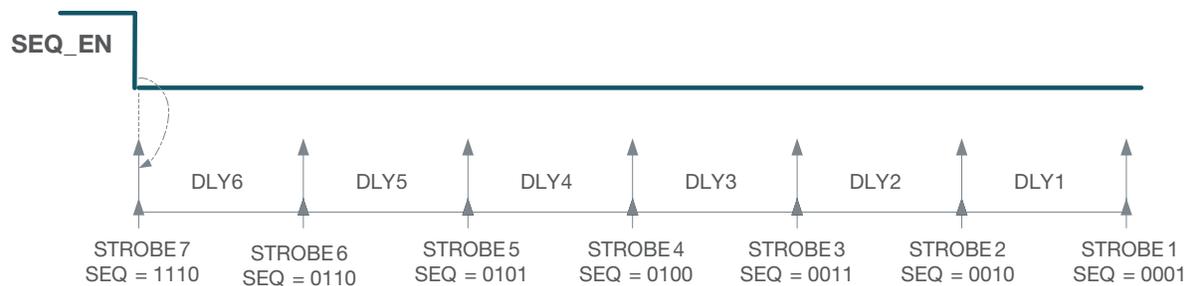


Figure 5. Time slot based down sequencing.

For example, assume there are three rails in the system called VR1, VR2 and VR3. DLY1, DLY2 and DLY3 are programmed to 2 milliseconds (ms), 4 ms and 8 ms, while the sequencing (SEQ) for VR1, VR2 and VR3 are programmed to binary 0001, 0010, 0011 – thereby assigning them to STROBE1, STROBE2 and STROBE3, respectively. During any power-up or power-down event, strobes get generated and rails VR1, VR2 and VR3 are enabled or disabled as per the delay and order in which the strobes are generated.

Strobe-based sequencing has a limitation in that it cannot handle multiple power-up and power-down sequences in the same PMIC for different power-up and power-down events. For example, if fault and reset events require a different power-down sequencing, then having two separate power-down sequencings – each for a fault and reset event – will not be possible. Similarly, if there are different power-up sequences, for instance, a cold boot and regular boot, a strobe-based sequencer fails because it cannot be programmed for multiple power-up sequences.

5. Instruction processor-based sequencing

In the instruction processor-based sequencing approach, a simple processor state machine in the PMIC called instruction processor, executes instructions from a specific memory segment.

Instructions such as ENABLE, DISABLE and WAIT are present on the chip NVM. As shown in **Figure 6**, depending on the event (power-up, power-down, faults, resets), the event detector module sets the memory pointer to a specific location from which a preprogrammed set of instructions are fetched. The instruction processor decodes the instructions from that memory location to set/reset the registers in order to enable/disable rails, generate POWERGOODs and RESETs after a programmable delay (through WAIT commands).

One disadvantage to this approach is the cost associated with on chip NVM for storing instructions is intensive. However, this approach can give complete flexibility and configurability in terms of different sequencing requirements.

Summary

The challenges in multi-core processor applications with complex sequencing and monitoring requirements for multi-rail systems in consumer, automotive and industrial domains are many. To address a designer’s full range of system needs with innovative, configurable, flexible sequencing while also monitoring, consider PMIC solutions such as the [TPS65217](#), [TPS65218](#), [TPS65913](#), and [TPS650860](#). These devices are designed for reliable operation, better efficiency and overall system health.

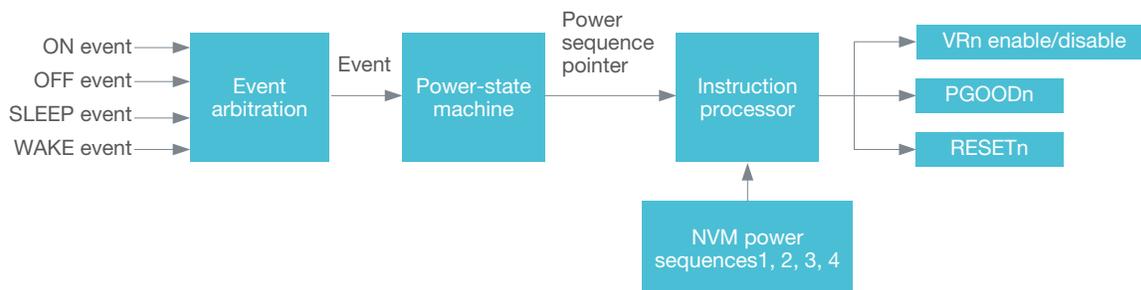


Figure 6. Instruction processor based sequencing block diagram.

References

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6. [Configurable Multi-Rail PMIC for 2S & 3S Li-Ion Battery-Operated Devices or Non Battery Operated](#), Texas Instruments.
7. For more information from Texas Instruments about [PMIC](#).

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