Build a true fidelity system using video signal conditioners

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Applying signal conditioners to high-speed video systems enables a true fidelity video system design with 4K display.

The ever-increasing sophistication of technology advancement has created an even greater appetite for higher quality video display. For example, in addition to ultra-high-definition 4K resolution, high-definition multimedia interface (HDMI®) version 2.0 doubles the frame rate from 30 to 60 frames per second (FPS) when compared to HDMI 1.4. HDMI 2.0 has effectively increased the video transmission data rate from 3.4 to 6 Gigabits per second (Gbps) per data lane.

Higher data rates that reach into the multi-gigabit level can significantly impact signal integrality when a signal travels through long traces, connectors, and long cables to the end receiver. The need for signal conditioners has never been more prominent in this multi-gigabit era. In this paper, we review and compare two popular video display standards: HDMI and DisplayPort. We also discuss the benefits of using a signal conditioner to enable a true fidelity video system design and what it takes to deliver a 4K display to consumers with each of these interface standards.

HDMI

HDMI is a popular video interface based on the Electronic Industries Alliance/Consumer Electronics Association-861(EIA/CEA-861) standard, which was established in 2003. HDMI can carry both video and digital audio signals from a source, for example, a video controller, to a sink device such as a high-definition television (HDTV) or monitor. HDMI is backwards-compatible with the digital visual interface (DVI) and uses transition-minimized differential signaling (TMDS) as the main communication channel.
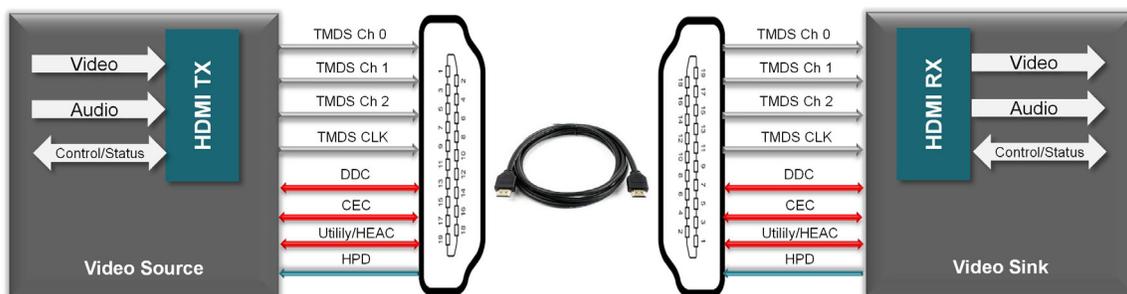

*Figure 1*. HDMI signal interface connecting a video source and sink through an HDMI connector.
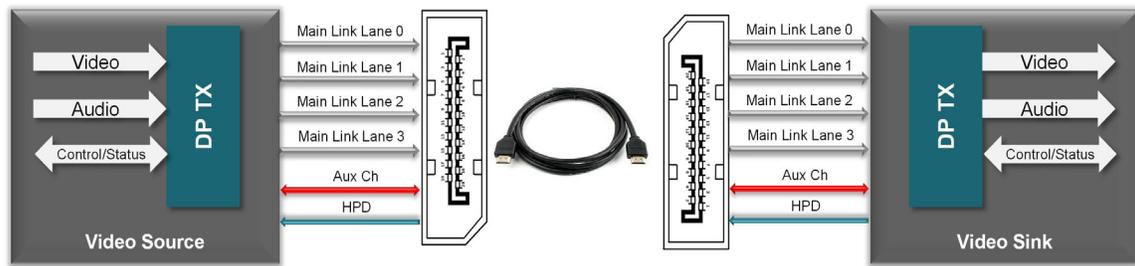
Figure 2. End-to-end DisplayPort signal interface.

While HDMI 1.4b has 30 FPS and HDMI 2.0 has 60 FPS, both can support 4K resolution. 4K ultra-high-definition (UHD) is a resolution of 3840 pixels × 2160 lines (8.3 megapixels, aspect ratio 16:9), and is one of the two resolutions of UHD television targeted towards consumer television. The other 4K resolution is 4096 pixels x 2160 lines with 8.8 megapixels for digital cinema projector. **Figure 1** shows an HDMI signal interface. HDMI includes four TMDS differential pairs with three pairs that carry data for video, audio and auxiliary data, and one pair that carries the clock. The physical layer for TMDS is DC-coupled. Using differential signaling can reduce the electromagnetic interference (EMI) and transmit the data serially over the data link.

For HDMI 1.4b, each TMDS data lane can support up to 3.4 Gbps. For HDMI 2.0, each TMDS data lane can support up to 6 Gbps. The display data channel (DDC) is based on I^{2}C for source to discover the sink's configuration and capabilities. The Consumer Electronics Control (CEC) protocol is used by HDMI devices to control each other, or to be operated by remote control devices. The HDMI Ethernet and audio return channel (HEAC) is optional to provide an Ethernet-compatible data network and an audio return channel from sink-to-source direction. A hot-plug-detect (HPD) signal notifies the source that a sink device is connected.

DisplayPort

DisplayPort is the newer display interface introduced by the Video Electronics Standards Association (VESA) in 2008. The aim of this standard was to replace VGA and DVI when connecting PC monitors and projectors. DisplayPort versions 1.2, 1.2a and 1.3 all support a resolution of 4K and above. The first two support high-bit rate 2 (HBR2) of 5.4 Gbps, while the third supports high-bit rate 3 (HBR3) of 8.1 Gbps. DisplayPort dual mode (or DP++) is comparable to HDMI 1.4b performance, which supports 4K at 30 FPS. DP++ can directly transmit HDMI TMDS signals using a simple adapter.

Figure 2 shows a DisplayPort signal interface. The main link consists of one, two or four AC-coupled differential lanes. AC-coupling enables DisplayPort source and DisplayPort sink to have different common-mode voltages. Each main link lane can support 8.1 Gpbs for DisplayPort 1.3, or 5.4 Gbps for DisplayPort 1.2a. The auxiliary (AUX) channel is a half-duplex, bidirectional channel used for link management and device control. The AUX channel has a data rate of 1 Mbps and uses Manchester II encoding. HPD is used to notify a source of the connection or generate an interrupt request by the sink device. DisplayPort provides link training, which allows sources and sinks to communicate and establish a robust audio/video link that other video technologies lack.
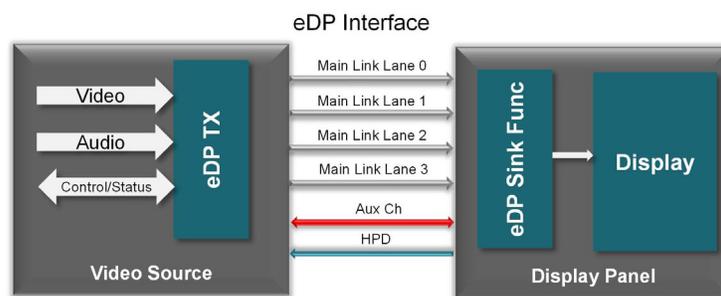
Figure 3. Embedded DisplayPort signal interface.

When DisplayPort ++ (DP++) was introduced in 2013, it was designed to enable DisplayPort interoperability with DVI and HDMI interfaces. This was achieved by adding three capabilities to DisplayPort and using a simple adaptor to output DVI and HDMI format:

- Adding a DP_PWR DisplayPort receptacle power pin provides power to a video adaptor
- Adding a CONFIG1 and CONFIG2 provides a discovery mechanism for dual-mode video adaptor
- Adding I²C over an AUX channel connects to an HDMI DDC interface

There are two types of dual-mode DP adaptors: Type 1 and Type 2. Type 1 supports a maximum TMDS clock rate of 165 MHz for both DVI and HDMI, and DDC signaling through I²C. Type 2 supports 165 MHz for DVI and 300 MHz for HDMI for a maximum TMDS clock rate, and both DDC and AUX-over-I²C signaling.

While DisplayPort defines the interconnect between different video sources and sink devices through an external cable connection, embedded DisplayPort (eDP) is defined for internal interconnect between the video source and display panel used in a notebook, for example. Typically the video source contains a graphics processing unit (GPU), and the sink device function is integrated into a display processor such as a notebook's liquid crystal display (LCD) timing controller (TCON). **Figure 3** shows the signal interface of an embedded DisplayPort.

Embedded eDP v1.4 is fully backwards-compatible with DisplayPort 1.2a. Generally, only one or two main-link lanes will be needed due to the small form factor and resolution needed for a laptop PC. Since eDP is internal to a system, the protocol can be flexible, depending on system requirements and dedicated display.

Signal conditioners

When signals traverse through a transmission media, such as over printed circuit board (PCB) trace, across connectors, over long cables, they are subject to the effects of noise, distortion and signal loss. Signal integrity and fidelity can be preserved at a low bit-rate and travel through longer distances. However, multi-gigabit signals such as DisplayPort and HDMI are subject to significant signal integrality degradation when signals traverse through long traces, across connectors or over long cables. The result could be reduced signal strength, a distorted or noisy signal at the receiving end, or a signal failing standard compliance.

Several techniques incorporated into a signal conditioner can be used to mitigate this signal integrity issue with DisplayPort or HDMI. Equalizers in both receive and transmit directions can be used to remove signal distortion in the frequency domain. A linear equalizer can process the incoming signal with a linear filter, and an adaptive equalizer can update the equalizer parameter as it processes the data to achieve the best performance.
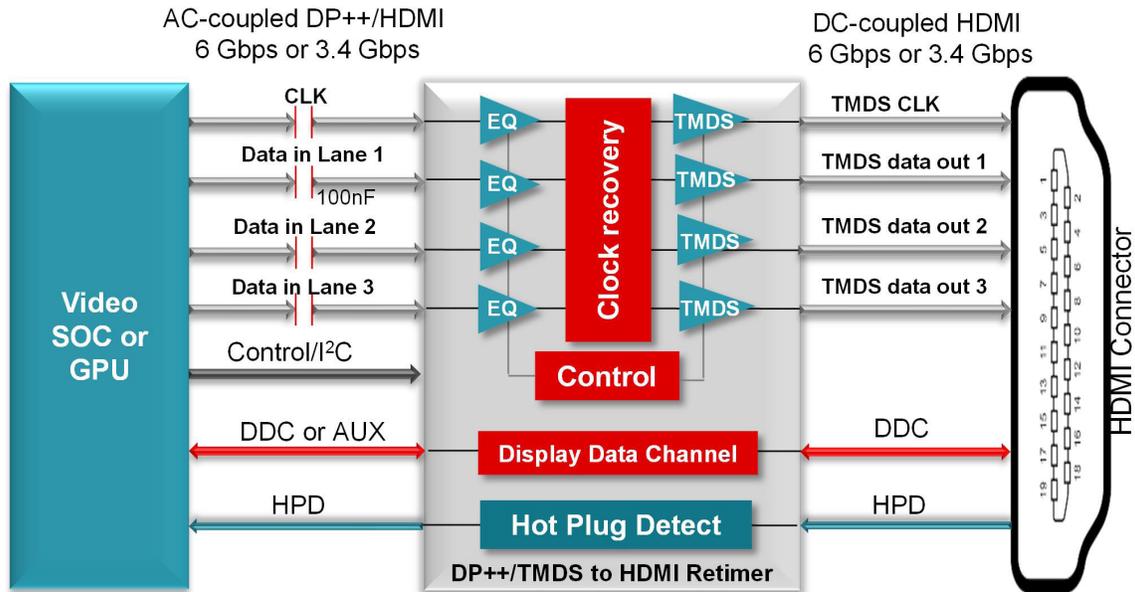
Figure 4. *Source-side retimer block diagram.*

Pre-emphasis is an often-used signal conditioning technique that can increase the magnitude of some frequencies to improve the overall signal-to-noise ratio (SNR). Clock and data recovery circuits can recover the clock at the receiver end, and recreate a cleaner signal with input noise, inter-symbol interference and jitter removed.

Redrivers and retimers, or repeaters, are typical signal conditioners. A redriver is an analog component used to restore an attenuated input signal through equalization and gain adjustment, and to re-transmit the signal based on signal specification. Redrivers also can be used to shift common-mode voltages, for example, going from an AC-coupled to DC-coupled signal.

A retimer is a mixed-signal component used to recover an attenuated input signal with clock data recovery circuits, compensate the phase and random jitter, then retransmit the signal based on the signal specification. A retimer usually includes redriver functionalities.

By using retimers and redrivers in DisplayPort or HDMI interfaces, the video system can maintain signal integrity over long traces or cables with improved signal quality. Retimers and redrivers enable design flexibility by extending the distance that a signal can travel across cables or traces. This enables a broad range of interoperability, as well as improved system performance, while helping a system to pass standard compliance.

Video source-side signal conditioner

As GPUs and other system-on-chip (SoC) devices migrate to lower geometry CMOS processes, they are moving away from supporting high common-mode, wide-swing physical layer technologies like HDMI. Their preference now is AC-coupled technologies like DisplayPort, PCIe, and USB 3.1. This, along with the distance between these SoC devices and HDMI connectors, makes it difficult to pass HDMI compliance. Increasing the data rate makes this process even more difficult. To pass compliance redrivers and retimers are needed. **Figure 4** shows a block diagram for a retimer that takes the AC-coupled input signal and converts it to DC-coupled TMDS signaling.
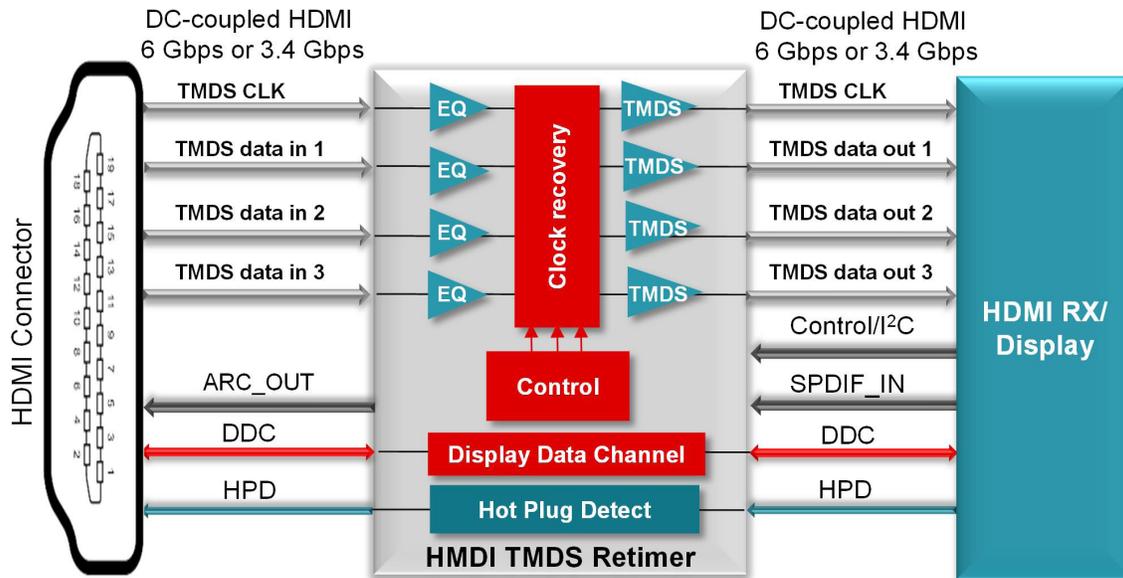
Figure 5. *Sink-side retimer block diagram.*

Signal conditioners, such as redrivers and retimers, can implement several features to improve signal integrity. They can support adaptive or fixed equalization to clean up inter-symbol interference jitter or loss from bandwidth-limited board traces to cables. Retimers use clock data recovery circuits (CDR) to cleanup random, phase and sinusoidal jitter. Good retimers have wideband CDR tracking and narrowband jitter cleaning, as well as the capability to work with wide frequency ranges. Retimers enable signal recreation without expensive external components, and the recovered clock can be forwarded to the sink. The transmitter provides several features for passing compliance and reducing system-level design issues like de-emphasis, which compensates for the attenuation when driving long cables or high-loss board traces.

Video sink-side signal conditioners

Where source-side redrivers and retimers are used to pass compliance at the source connector sink-side, signal conditioners must pass sink-side compliance, which is much more difficult.

Sink-side HDMI retimers need to support four TMDS channels, an audio return channel, and digital display control (DDC) interfaces. These retimers must support both HDMI 1.4b and HDMI 2.0, which provides a challenge. For HDMI 1.4b the clock rate is one-tenth the data rate and can be between 25 MHz and 340 MHz. When a system is HDMI 2.0, the clock rate is one-fortieth the data rate for data rates greater than 3.4 Gbps. The clock frequency for HDMI 2.0 overlaps HDMI 1.4b, 85 MHz to 150 MHz. This requires retimers to be more intelligent by having to read certain registers and bits on the DDC line. **Figure 5** shows a sink-side retimer block diagram, which can be found in an ultra-HDTV.

Figure 6 shows a source and sink application with a signal conditioner at both ends.
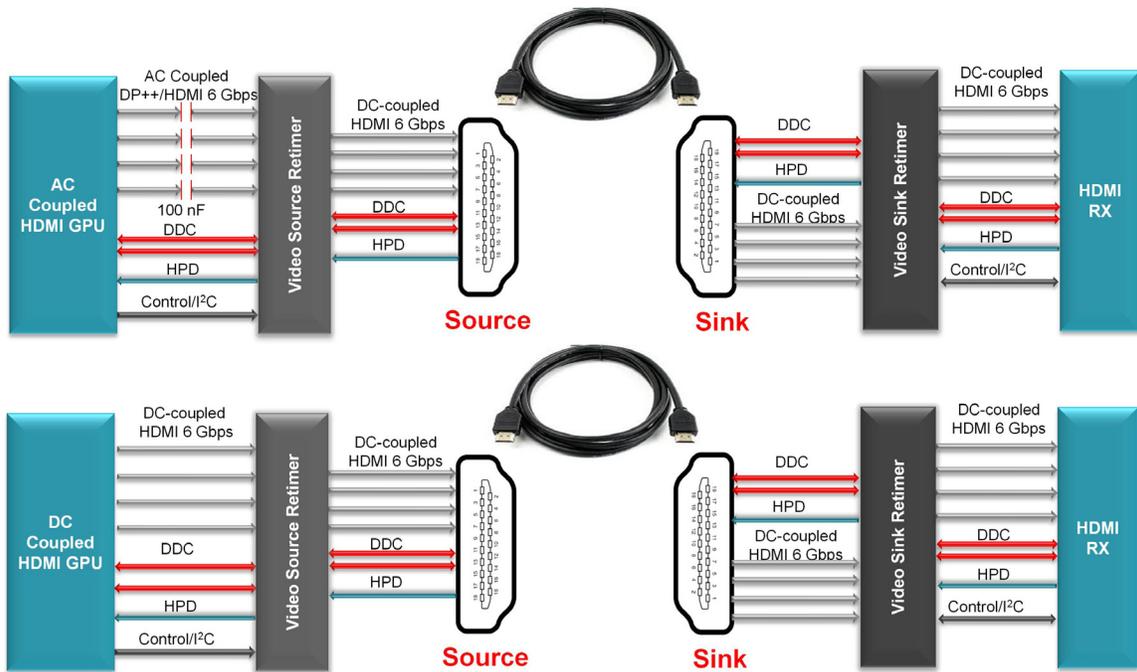
Figure 6. End-to-end system block diagram using video signal conditioner.

Conclusion

As cinema-quality, 4K resolution is becoming main stream, the need for signal conditioners to bring the desired video bandwidth over a Gigabit link continues to increase. Video signal conditioners such as the SN65DP159, SN75DP159, SN65DP149, SN75DP149, TMDS181I, TMDS181, TMDS171I and TMDS171 enable these 4K video systems. These video conditioners provide low-power consumption and state-of-the-art clock data recovery (CDR) technology for quality signal performance. These retimers have Eye Scan, a built-in real-time diagnostic tool that visualizes eye quality, which simplifies system design and debugging. Using TI video signal conditioners, a designer can overcome high-speed video signal design challenges, preserve 4K video signal fidelity, and increase system performance for a true 4K video experience.

References

- Learn more about these TI solutions: interface, retimers, redrivers

- Download these data sheets: SN65DP159, SN75DP159, SN65DP149, SN75DP149, TMDS181I, TMDS181, TMDS171I and TMDS171

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