GaN FET module performance advantage over silicon

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Learn how GaN improves energy efficiency, power density and solution size in next generation DC/DC converters.

Gallium-nitride (GaN) FETs are increasingly finding use as next-generation, high-power devices for power electronics systems [1]. GaN FETs can realize ultra-high-power-density operation with low power loss due to high carrier mobility in the two-dimensional electron gas (2DEG) channel, and high breakdown voltage due to large critical electric field. GaN FETs are a majority carrier device, therefore, the absence of reverse recovery charge creates a value proposition for high-voltage operation.

Introduction

All these characteristics are suitable for power electronics applications featuring reduced power loss under high-switching-frequency operation.

With GaN devices now being grown on affordable silicon substrates, compared to GaN on sapphire or bulk GaN, power GaN FETs will find an increasing rate of adoption for highly efficient and form factor constrained applications in the 30V and higher DC/DC voltage conversion space. In this paper we investigate the loss mechanisms in a hard-switched DC/DC converter and how a GaN FET power stage can outperform Si MOSFETs. In this paper we compare a 80V GaN FET power stage to 80V Si devices.

A GaN FET power stage device such as the LMG5200 is an 80V GaN half-bridge power module. This device integrates the driver and two 80V GaN FETs in a 6 mm x 8 mm QFN package, optimized for extremely low-gate loop and power loop impedance [2]. The inputs are 3V CMOS and 5V TTL logic compatible. Due to GaN's intolerance for excessive gate voltage, a proprietary clamping technique ensures that the gate voltage of the GaN FETs is always below the allowed limit. This device extends the advantage of discrete GaN FETs by offering a user-friendly package, which is easy to layout and assemble into the final product.

The LMG5200 meets the IPC-2221B and the IEC 60950 pollution degree 1 clearance and creepage requirements without any need for underfill. This is because the minimum spacing between high- and low-voltage pins is greater than 0.5 mm. This eliminates the need for boards to be manufactured with underfill and greatly simplifies board design and reduces cost. The pin-out also eliminates the need for a via-in-pad design as there is adequate spacing between the power pins for via placement. Additionally, this helps in to reduce board complexity and cost (**Figure 1**).

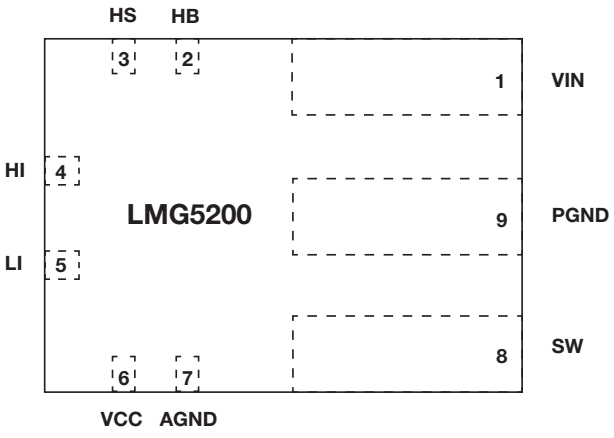


Figure 1. *Top-down view of a GaN FET power stage device, showing pin-out.*

DC/DC converter losses

In this section we briefly discuss mechanisms that cause losses in hard switched converters.

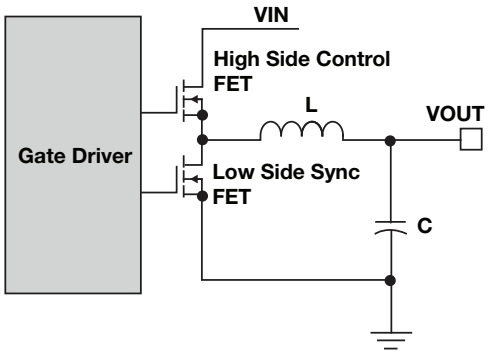


Figure 2. *Simplified view of the buck power stage*

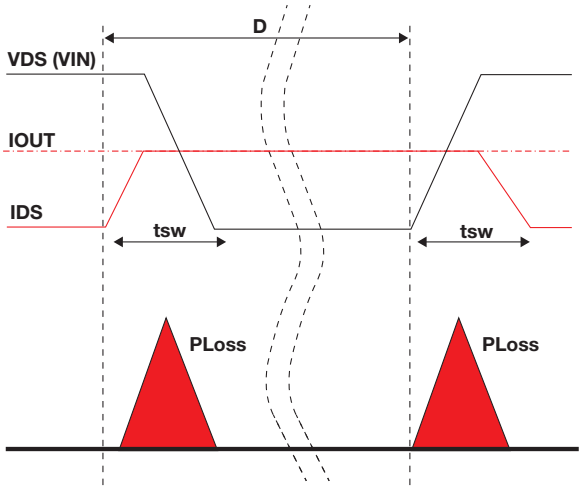


Figure 3. *Turn-on and turn-off losses during inductive switching*

In this paper, a synchronous buck converter (Figure 2) is used as a DC/DC converter to compare the losses in a hard-switched converter. The approach for comparing the loss mechanism can be applied to other hard-switched converters as well. Losses in a switched-mode converter can be broadly divided into conduction losses and switching losses. The high-side MOSFET dissipates most of the switching losses. Conduction losses are a function of the duty cycle and are shared between the high- and low-side devices. For low-duty cycle DC/DC converters, the low-side FET has a higher amount of conduction loss, which can be calculated as:

$$P_{COND(HS)} = R_{DS(ONHS)} \times I^2_{RMS(HS)} \quad (1)$$

$$P_{COND(LS)} = R_{DS(ONLS)} \times I^2_{RMS(LS)} \quad (2)$$

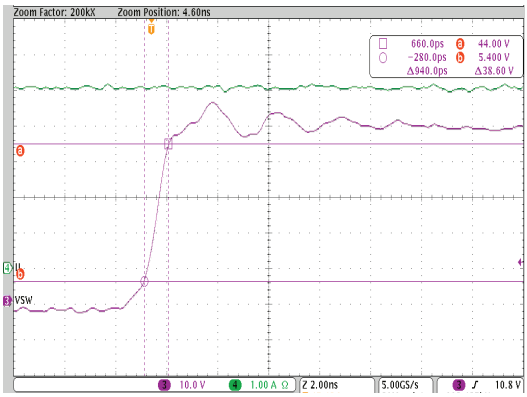
where $R_{DS(ONLS)}$, $R_{DS(ONHS)}$ is the low-side and high-side FET resistance, and IRMS(LS), IRMS(HS) are the low- and high-side RMS currents, respectively.

The switching loss (Figure 3) due to the I_{DS} current and V_{DS} overlap is in the high-side of a buck converter and can be estimated as:

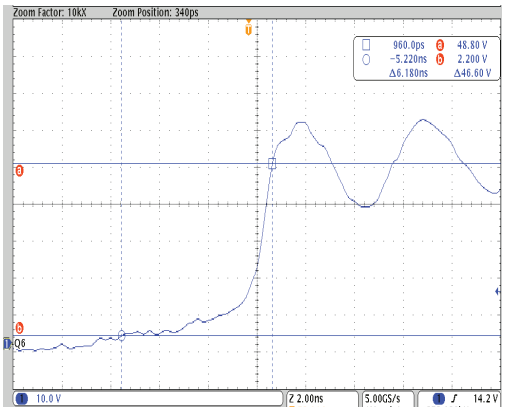
$$P_{SWHS} = V_{IN} \times I_{OUT} \times f_{SW} \times t_{SW} \quad (3)$$

where t_{SW} is the switching time. This includes the current commutation time through the FET and the time for the FETs drain-to-source voltage to rise / fall by V_{IN} during turn-off and turn-on, respectively.

The low-side FET does not have any switching loss due to zero voltage switching (ZVS) turn-on and turn-off. The actual waveforms for inductive switching are more complicated than those shown in Figure 3, however, the error in the calculated loss is acceptable as long as the correct switching time is used for the turn-on and turn-off.



a) LMG5200 switch node



b) Si7852DP 80v FET SW node

Figure 4. *Comparison of a GaN FET power stage switch-node to silicon switch-node voltage waveform*

The device construction of GaN allows very short, switching times due to small gate and output capacitance for the same RDSON. As noted in **Figure 4,** switching time for the GaN FET power stage is less than 1 ns compared to 6 ns for a Si FET with a comparable breakdown voltage (Si7852DP).

Faster switching edges means the switching losses are significantly lowered in the GaN module compared to the Si MOSFET-based buck converter. Also note that there is minimal overshoot in the GaN FET power stage switch-node waveforms due to an extremely small (<300 pH) power loop inductance. The gate loop and common source inductance are also minimized in the GaN FET power stage package to be below 200 pH. High parasitic inductance in these loops can cause a significant power loss [3].

Besides the high-side turn-on and turn-off losses, forced commutation of the low-side MOSFETs body diode is a significant source of switching loss in high-voltage DC/DC converters. This loss is primarily due to the reverse recovery charge (QRR) in the freewheeling low-side FET. The power loss due to reverse recovery is given by:

$$P_{RR} = fsw \bullet Q_{RR} \bullet V_{IN} \quad (4)$$

Because GaN is a majority carrier device, it does not have reverse recovery-based losses.

The body diode of the low-side MOSFET conducts during dead time. This causes a power loss in the diode associated with the forward voltage of the diode. GaN has a higher third quadrant conduction voltage (V_{SD} of 2V at 10A for LMG5200) compared to ~1V for Si FETs. Hence, the GaN device exhibits a higher power loss during dead time. It is critical to ensure that the dead time is small in order to minimize this loss [4]. The power loss associated with the body diode can be calculated as:

$$P_{BD} = fsw \bullet V_{SD} \bullet I_{OUT} \bullet \left(T_{DEADON} + T_{DEADOFF} \right) \quad (5)$$

The energy stored in the output capacitance of the MOSFETs is dissipated during turn-on. Since the output capacitance is a strong function of the drain-to-source voltage, the proper way to calculate this power loss PCAP is:

$$P_{CAP} = fsw \bullet Q_{OSS(VIN)} \bullet V_{IN} \quad (6)$$

where $Q_{OSS(VIN)}$ is the output charge of the MOSFET, evaluated at the input voltage. GaN devices, due to their small output capacitance for the same RDSON compared to Si, exhibit a much smaller PCAP loss as well.

Gate driver losses are another contributor to switching loss. A detailed explanation of losses associated with the gate driver can be found in the LM5113 application report [5].

Besides the active device-related losses in a hard-switched buck converter discussed in this paper,

there are losses associated with the inductor. These losses include core loss and AC- and DC-winding loss, which also should be taken into account when calculating system efficiency [6, 7].

Efficiency improvements compared to Si

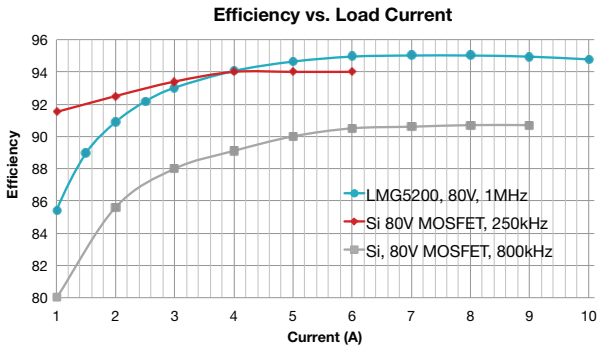


Figure 5. LMG5200 vs Si at different frequencies

Figure 5 shows the efficiency delta between a 48V:12V LMG5200 buck and 80v Si MOSFET-based buck. The LMG5200 is switching at 1 MHz while the Si-based implementation is switching at 250 kHz and 800 kHz, respectively. As shown, the LMG5200 has higher efficiency versus load than the Si solution switching at a lower frequency (1 MHz vs 800 kHz). This is indicative of the fact that switching and conduction losses in the GaN FET power stage are much lower compared to the similarly rated Si MOSFET. When the Si MOSFET-based converter is redesigned for a 250 kHz switching frequency, we see higher efficiency for Si designs at light loads as expected. However, as the load increases to 4A, the GaN FET power stage switching at 1 MHz shows a much higher efficiency.

A comparison with Si at 800 kHz shows that the efficiency of the GaN FET power stage is much higher across a wide load range, even while switching at 1 MHz.

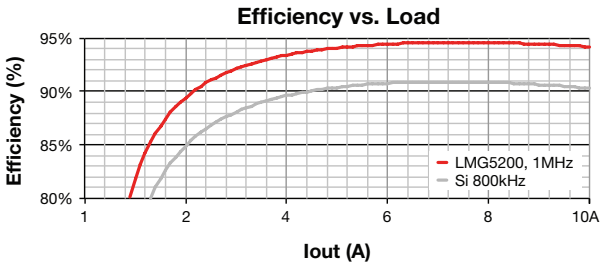


Figure 6. Calculated efficiency comparison between the GaN FET power stage design at 1 MHz and Si FET design at 800 kHz

A comparison of the efficiencies observed in the hard-switched buck with the calculated results indicates that the calculations are within the margin of error for the simplified model presented (Figure 6).

Summary

Power GaN FETs, due to their extremely low-gate charge and output capacitance, can be switched at extremely high speeds with significantly reduced switching losses and improved efficiency compared to silicon FETs. The LMG5200, an 80V GaN FET power stage, has been optimized for applications requiring high efficiency and/or small form factor. Its advanced package greatly simplifies manufacturability and board design while reducing costs. The LMG5200 can improve the performance across a wide variety of applications while reducing adoption risk. These applications include multi-MHz synchronous buck converters, Class D amplifiers for audio, and 48V to POL converters for data communications and telecommunications servers. GaN FET power stage devices provide significant efficiency benefits across a wide load range while improving switching frequency and power density.

To learn more about TI's GaN solutions, please visit **www.ti.com/GaN**.

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