Transient protection design for power switches to achieve robust, reliable power-path protection

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Introduction

Component integration in modern electronic systems enhances performance by increasing functionality. Most of these systems use sensitive and expensive electronic devices (field-programmable gate arrays, application-specific integrated circuits and microprocessors) that need protection.

Traditional protection solutions such as fuses, positive temperature coefficient resistors, diodes and discrete circuits (including fuses, metal-oxide semiconductor field-effect transistors and diodes) are inaccurate, slower to respond, and lack configurability and repeatability. Thus, active circuit protection using eFuse and hot-swap solutions have begun to replace discrete front-end protection circuits in many applications [1], [2].

Active-circuit-protection eFuses often need additional protection, however, to protect them from transient events. The most common transient events include hot plugging, abrupt current interruption, power surges, hard switching and reverse voltages.

Any of these transient events put electrical overstress on the device, leading to failure. In this article, we'll discuss electrical overstress (EOS) and the design process for transient protection components in a 200A eFuse enterprise server application, including placement and printed circuit board (PCB) layout considerations.

Understanding EOS

The Industry Council on ESD **defines electrical overstress** [3] as "when a maximum limit for either the voltage across, the current through, or the power dissipated in the device is exceeded and causes immediate damage or malfunction, or latent damage resulting in an unpredictable reduction of its lifetime." Of these conditions, it is the overvoltage that can open unintended current paths such as forward or reverse breakdown of diodes or oxides reaching their breakdown voltage within integrated circuits (ICs). Once an overvoltage opens an unintended current path, the resulting currents can cause damage that includes the melting of silicon; the fusing of metal interconnects; thermal damage to packaging material; and the fusing of bond-wires, leading to electrically induced physical damage (EIPD).

It is possible to relate EOS to the absolute maximum ratings specific to the voltage ratings of a device:

- Region A: The safe operating area.
- Region B: No guarantee on device functionality or parameter specifications. Although physical damage is not expected, extended operation may have reliability issues.
- Region C: Beyond the absolute maximum ratings, there is a severe degradation in device lifetime, and a risk of latent failure.
- Region D: Expected to suffer immediate physical damage.

As **Figure 1** illustrates, you should expect problems when the device operates beyond the absolute maximum rating. That's why suppressing transient overvoltages beyond the absolute maximum rating requires protection.

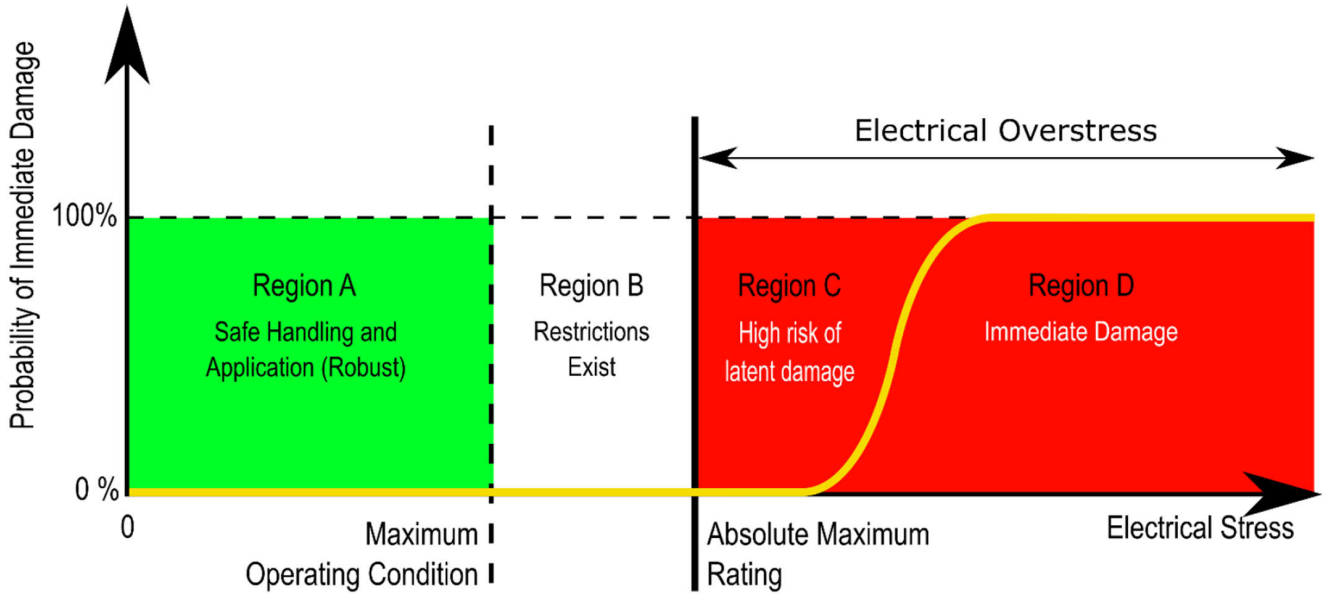

Figure 1. *Interpreting absolute maximum ratings to EOS.*

Enterprise server system example

eFuses are widely used in rack server modules at the front end for input protection and to enable hot-swapping functionality. **Figure 2** shows the typical power distribution architecture of a rack server, where the input comes from a 12V backplane and is then distributed from the eFuse to all downstream loads. The power path, which involves the backplane, PCB traces and interfacing connectors, introduces parasitic inductance (L) that then creates unintended transient voltages during fault events.

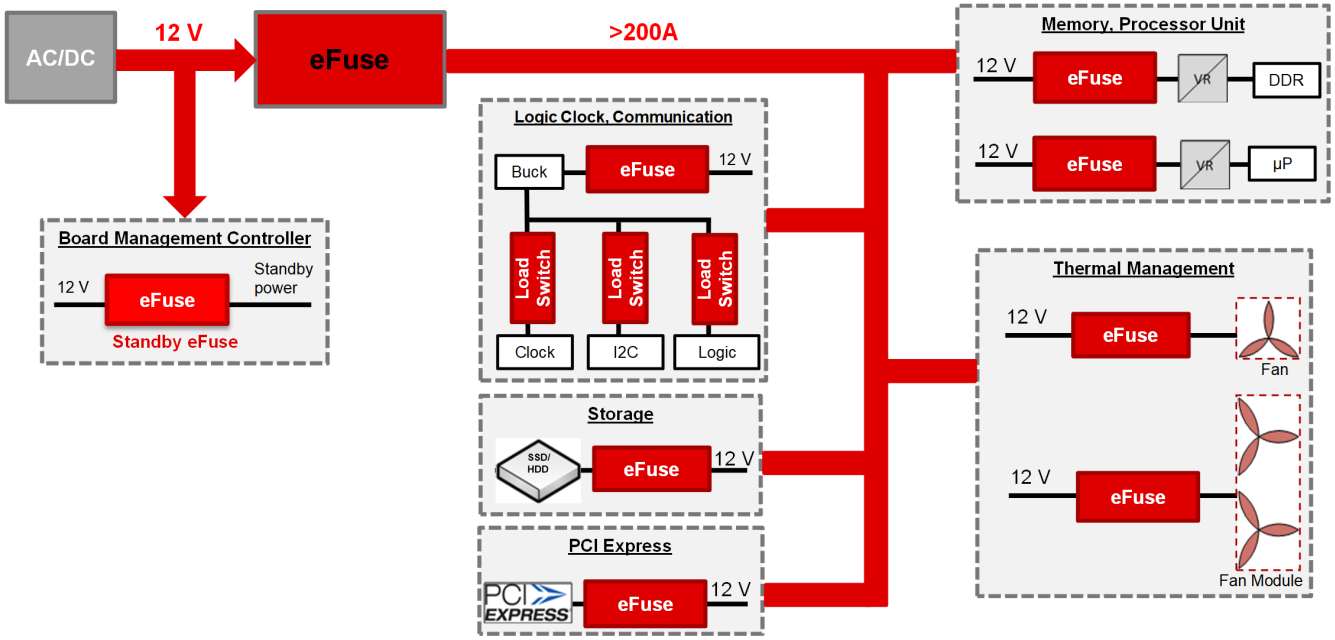

Figure 2. *A typical block diagram of the power distribution of a 12V rack server.*

Let's quantitatively analyze the impact of L on the eFuse, as illustrated in **Figure 3**. In the case of an output short circuit, the eFuse interrupts a large amount of current instantaneously from approximately 200A (overcurrent) to 0A (shutoff for protection) within 1µs, resulting in a large current transient (di/dt), as shown in **Equation 1**:

$$di/dt = (0A - 200A)/1\mu s = -2 \times 10^8 A/s \quad (1)$$

This current will be trapped as energy in the parasitic inductance and produce a surge, expressed by **Equation 2**:

$$VL = L \times di/dt = 100nH \ -2 \times 10^8 A/s = -20V \quad (2)$$

That –20V surge will be in series with the 12V input power supply and will effectively create a positive voltage spike of 32V, exceeding the 20V VIN absolute maximum rating of the TPS25984B eFuse from Texas Instruments (TI). Similarly, the output inductance creates a negative voltage spike on the output.

To prevent this, a transient voltage suppressor (TVS) diode will clamp the voltages on the positive side, while a low-forward-voltage freewheeling Schottky diode will clamp the voltages on the negative side. Careful selection of these components is necessary to ensure reliable system protection.

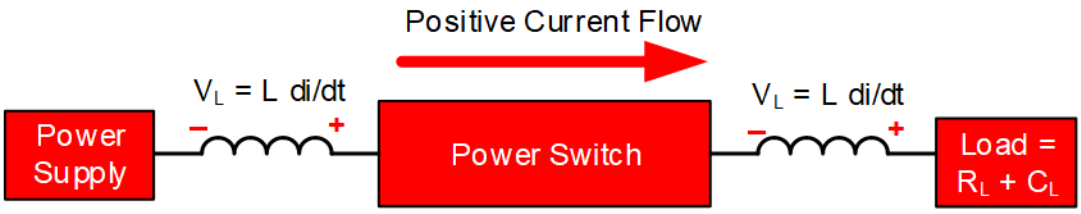

Figure 3. *Inductive kickback voltages caused by an abrupt interruption of fault current in a power switch.*

TVS diode selection

A TVS diode is designed to protect electronic components from voltage spikes. The TVS diode begins to operate once the voltage on the diode exceeds the avalanche breakdown potential. **Figure 4** is a graph of a TVS diode's current-voltage curve.

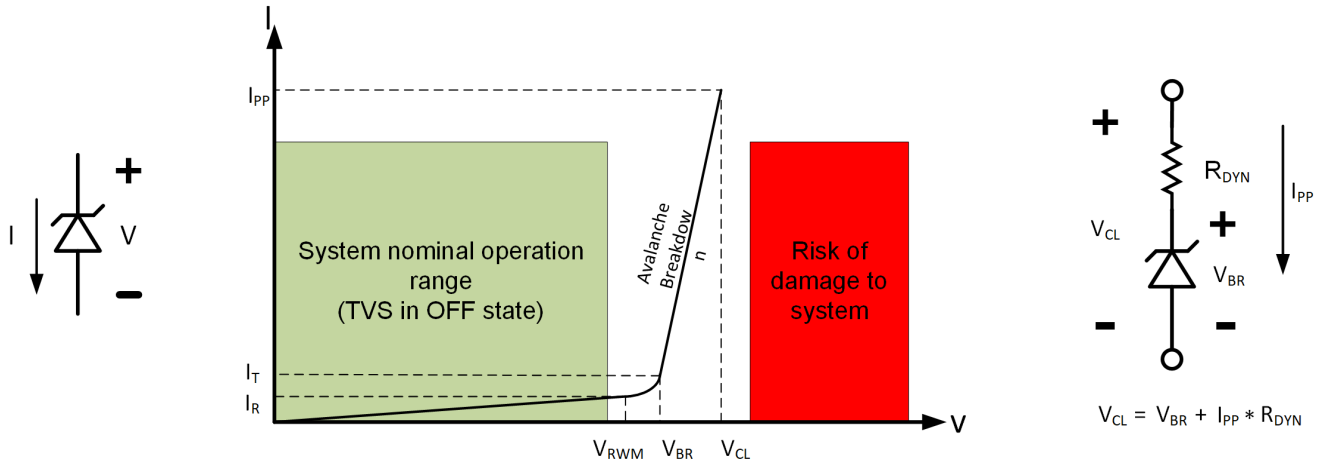

Figure 4. *TVS diode characteristics.*

As you can see in **Figure 4**, the final clamping voltage is a function of the current, which the TVS diode shunts, and the dynamic resistance (R_d) of the TVS diode. Again, the dynamic resistance is a function of diode package size and the time duration (t_P) that the TVS diode shunts the current.

For example, the SMAJ diode (13.52mm^2) has a higher R_d than the SMBJ diode (19.44mm^2), so the SMAJ diode leads to a higher clamping voltage at a given shunt current.

Use these values of R_d to calculate the clamping voltage, these values are available from the TVS diode manufacturer's data sheet.

For $t_p \leq 20\mu s$:

$$R_{d(t_P)} = R_{D(8/20\mu s)} \tag{3}$$

For $20\mu s < t_p < 1ms$:

$$R_{d(t_P)} = \frac{R_{D(10/1{,}000\mu s)} - R_{D(8/20\mu s)}}{980} \left[t_P - 20\mu s\right] + R_{d(8/20\mu s)} \tag{4}$$

For $t_p \geq 1ms$:

$$R_{d(t_P)} = R_{D(10/1{,}000\mu s)} \tag{5}$$

This multiparameter dependency leads to a challenging iterative design process. To ease design, TI released an online tool for TVS selection [5]. **Figure 5** illustrates the design methodology as a flow chart, while **Table 1** lists the typical specifications of a rack server.

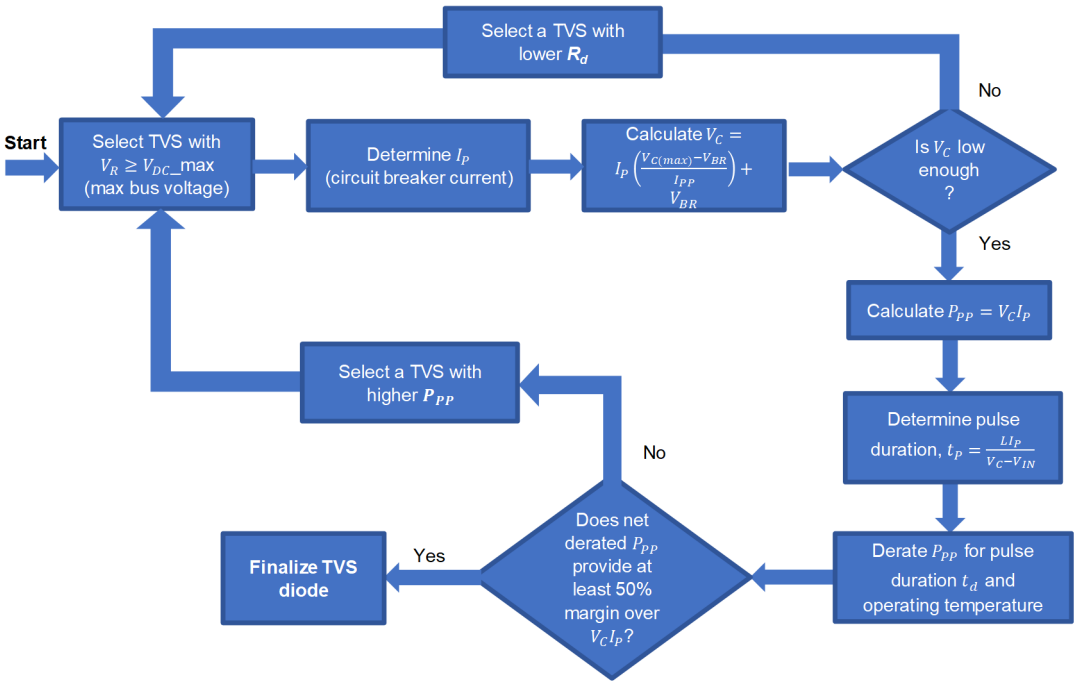

Figure 5. *Flow chart for TVS diode selection.*

Parameter	Value
Nominal operating voltage (V_{IN})	12V
Maximum operating voltage (V_{DC}_max)	13.2V
Circuit breaker current (I_P)	200A
Parasitic inductance (L)	100nH
Maximum tolerable voltage ($V_{C(max)}$)	20V
Maximum operating temperature	75°C

Table 1. *Typical system specifications.*

Design steps

When designing an input protection for the rack server, select the supporting component values for the TPS25984B eFuse from its data sheet and then follow the following design steps for TVS selection. First, select a unidirectional TVS with a reverse standoff voltage equal to or greater than V_{DC}_max. We chose the Littlefuse SMDJ12A diode [4] as a starting point. Next, determine the I_P, which is nothing but the circuit breaker current. Then calculate clamping voltage. Because R_d is a function of t_P, use **Equation 6** to find t_P:

$$t_p = \frac{LI_p}{V_{c(max)} - V_{IN}} = \frac{100nH \times 200A}{20V - 12V} = 2.5\mu s \quad (6)$$

For pulse widths below 20µs, you can approximate the dynamic resistance to that at an 8/20µs test pulse. From the SMDJ12A data sheet, our calculations were:

$$V_{BR(max)} = 14.7V \quad (7)$$

$$V_{C(max)} \text{at} I_{PP}(8/20\mu s) = 25.71V$$

$$I_{PP}(8/20\mu s) = 754A$$

Therefore:

$$R_{d(8/20\mu s)} = \frac{V_{C(max)} - V_{BR(max)}}{I_{PP}} = \frac{25.71 - 14.7}{754} = 14.6m\Omega \quad (8)$$

Now, using the R_d of 14.6mΩ, calculate the clamping voltage:

$$V_C = V_{BR(max)} + I_P \ R_d = 14.7V + 200A \times 14.6m\Omega = 17.6V \quad (9)$$

Because the clamping voltage is less than maximum tolerable voltage, $V_{C(max)}$ (the 20V absolute maximum rating of TPS25984B eFuse), you can proceed further with the SMDJ12A; otherwise, you will have to consider a TVS diode with a lower R_d, or parallel TVS diodes.

Calculate the peak power using:

$$P_{PP} = V_C \ I_P = 17.6V \times 200A = 3.52kW \quad (10)$$

Because the SMDJ12A supports a peak power of 60kW for 2.5µs (see **Figure 6**), you can proceed further.

Now, derate the power rating with temperature by using **Figure 6**. The maximum power support at 75° is:

$$P_{PP} \times \text{derating\_factor} = 0.8 \times 60kW = 48kW \quad (11)$$

Because 48kW > 3.52kW and V_C < 20V, the SMDJ12A is a good choice for this application.

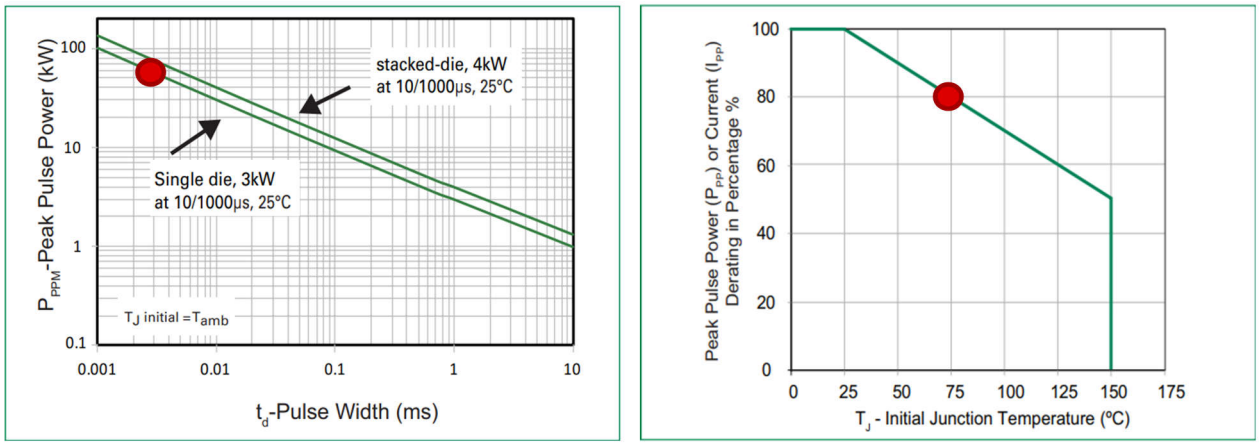

Figure 6. *Peak pulse power rating (left) and peak pulse power derating curve (right).*

Figure 7 shows the clamping performance of the SMDJ12A on the TPS25984B system.

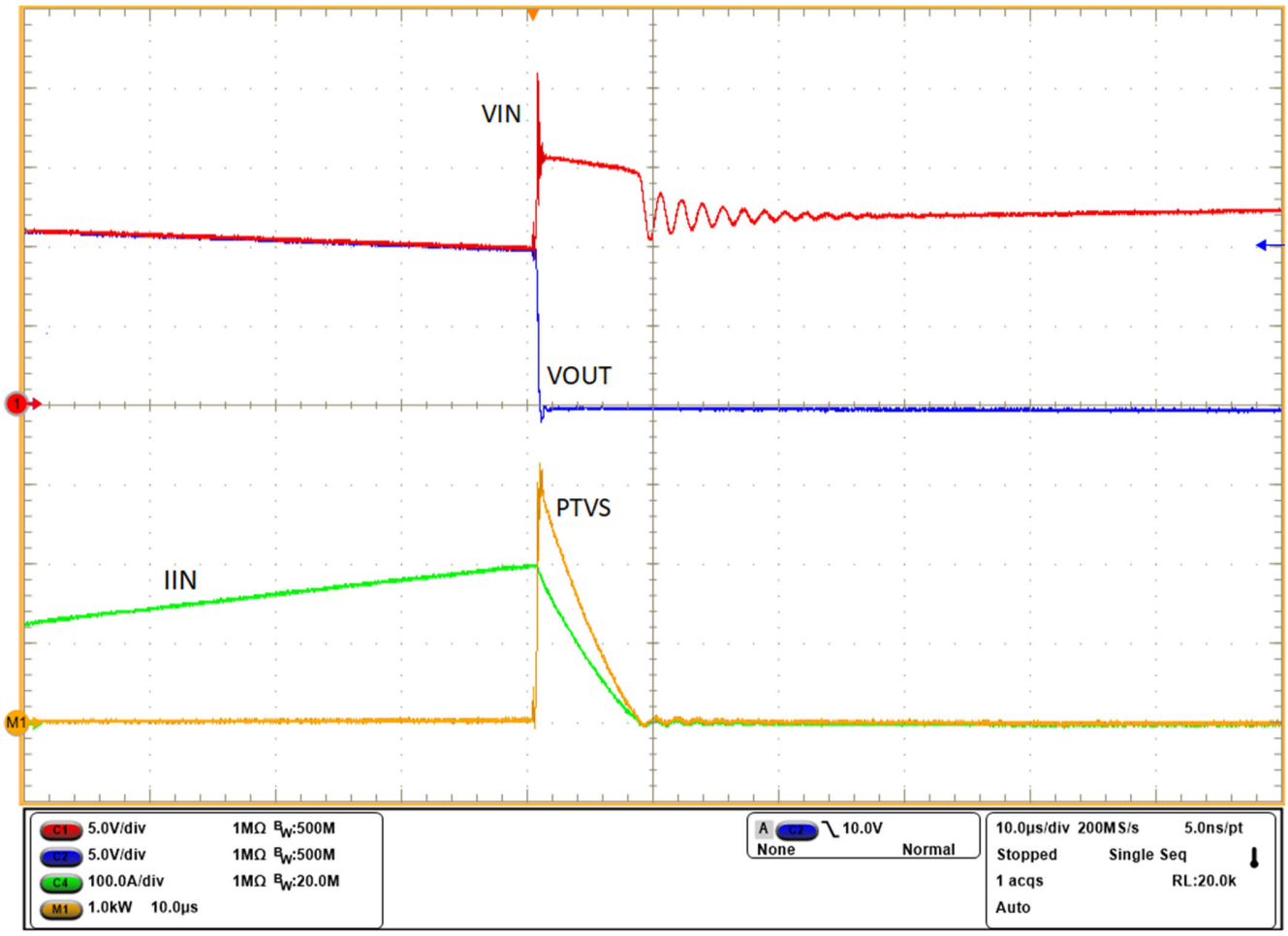

Figure 7. *Transient protection with the SMDJ12A diode at the input of the TPS25984B eFuse.*

Output Schottky diode selection

Figure 8 shows the sequence of events that could happen internal to the IC when taking the OUT pin below ground. The parasitic PN junction diode starts conducting, which injects free electrons into the substrate. These free electrons interfere with other control units that could reset the IC or cause a latch-up event. A large current conduction through the parasitic PN junction diode could cause EOS and lead to EIPD.

It is possible to prevent these issues by either reducing the peak negative voltage at the OUT pin or by limiting the current through the OUT pin. Adding an output capacitor close to the OUT pin will absorb some of the energy from the negative voltage spike and control the slew rate to limit the peak negative voltage. Adding a low-forward-voltage Schottky diode at the OUT pin provides an alternate path for current and limits the current through the IC.

Effective clamping requires a combination of capacitors and Schottky diodes. While a higher-output capacitor is helpful, use these guidelines when selecting a Schottky diode:

- The DC blocking voltage must be more than the maximum input operating voltage.
- The non-repetitive peak forward surge current of the selected diode must be higher than the I_P.
- The forward voltage drop at the I_P must be within the absolute maximum rating of the OUT pin (which is –1V for the TPS25984B).

We used two SBR10U45SP5 [6] diodes from Diodes Incorporated in parallel in this application.

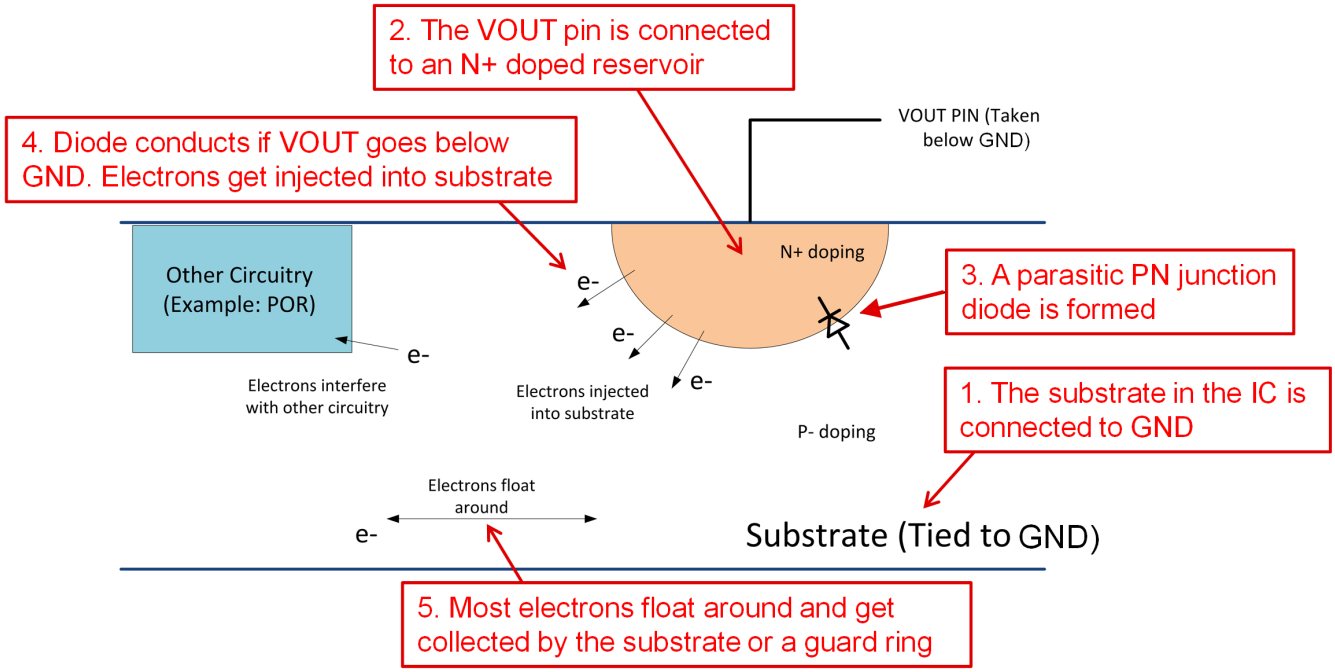

Figure 8. *Graphical illustration showing the consequences inside the IC when taking the output below ground.*

Figure 9 shows the output clamping performance with and without Schottky diodes in the TPS25984B solution.

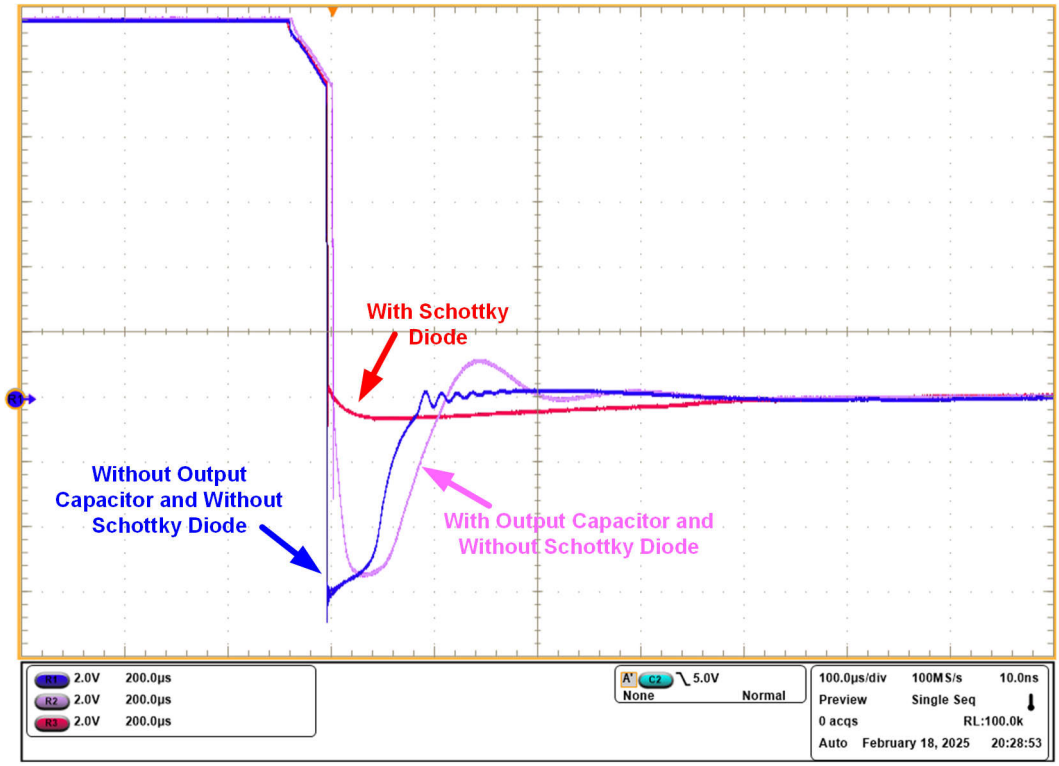

Figure 9. *Transient protection at the output of the eFuse.*

When dealing with high-current hot-swap solutions, secondary protection (shown in **Figure 10**) can minimize the Schottky diode requirement at the output. As you can see, D1 will absorb most of the energy from the negative voltage transient. Adding a small-value resistor (R1) such as 47Ω and a diode (D2) such as an SS13 will significantly limit the remaining energy.

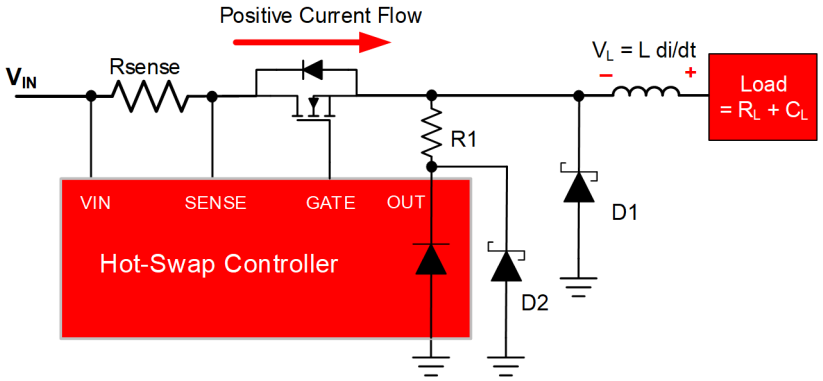

Figure 10. *Secondary protection in high-current hot-swap solutions.*

Placement and PCB layout considerations

You must place protection devices such as TVS diodes, decoupling capacitors and Schottky diodes physically close to the device they are intended to protect. The distributed inductance limits the bandwidth of the effectiveness of the shunt elements, such as decoupling capacitors and TVS diodes. It restricts the surge current flow and also leads to larger transient voltage spikes during clamping, as shown in **Figure 11**. Therefore, the layout should be such that these shunt elements have the least series impedance. When routing, use short traces and multiple vias to reduce inductance.

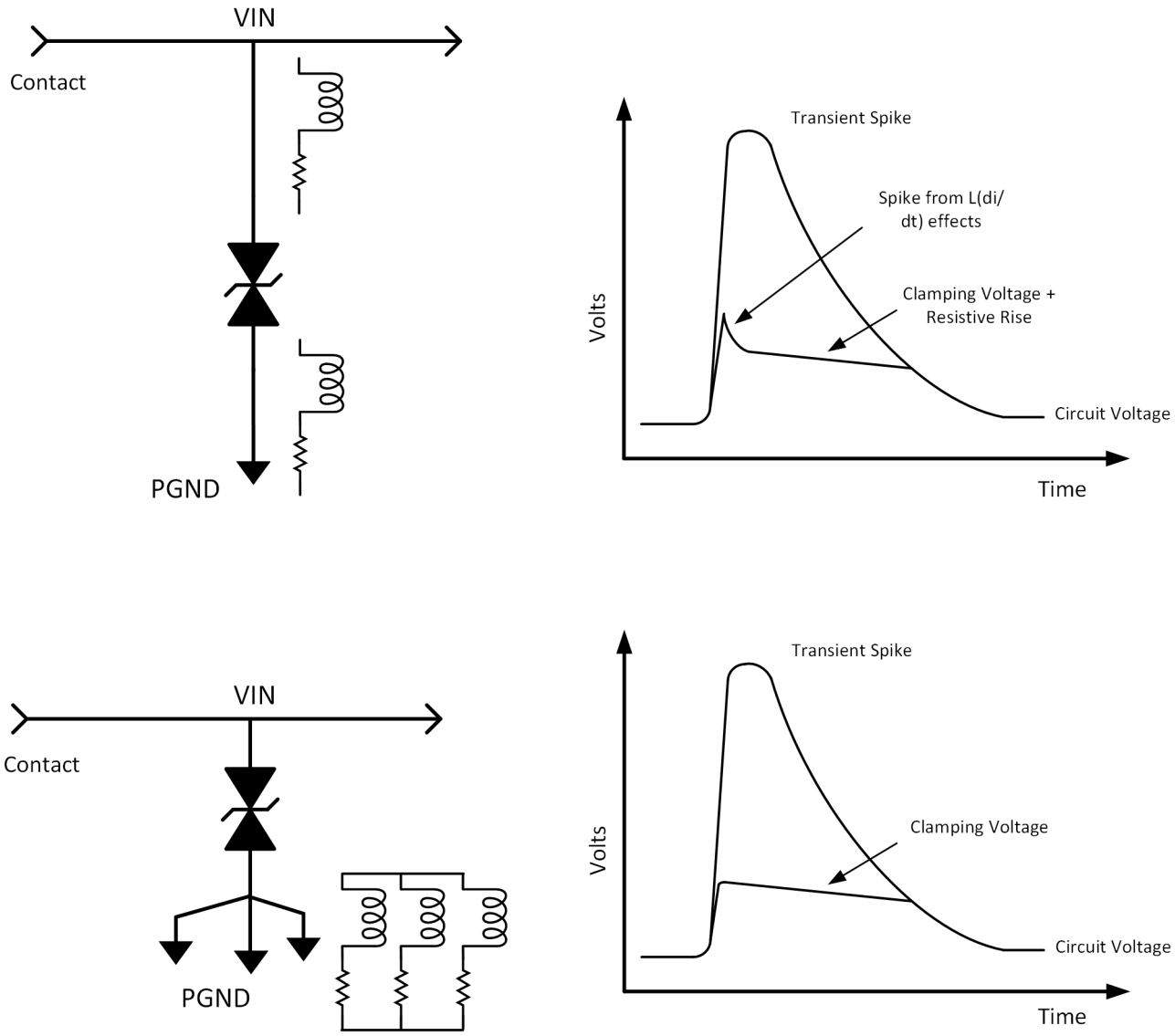

Figure 11. *Impact of TVS clamping performance with respect to PCB layout.*

Conclusion

Discrete front-end protection circuits are being replaced with active circuit protection devices such as eFuses to improve performance. However, an eFuse often needs transient protection to prevent its absolute maximum spec violation. The component selection guidelines and layout considerations discussed in this article can help you design a solution to ensure reliable power-path protection.

References

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4. "**SMDJ12A TVS 3KW 12V 5%UNI DO-214AB TR13 RoHS**." Littlefuse data sheet. 2025.
5. Texas Instruments. n.d. **TVS diode recommendation tool**. June 26, 2023.
6. "**SBR10U45SP5 10A SBR super barrier rectifier**." Diodes Inc. data sheet, literature No. DS31371, January 2024.

Related Websites

- **TPS25984B**
- **LM5066I**

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