Powering an offboard capacitive load in automotive zone-based power distribution systems

Dilip Jain
Systems Manager
Power Switches

Rakesh Panguloori
Applications Manager
Power Switches

Introduction

The transition of vehicle architectures from domain- to zone-based is significantly changing automotive power distribution, with semiconductor switch-based solutions (see **Figure 1**) replacing the traditional melting fuses used for wire harness protection. These solutions offer benefits such as less variability in fuse-time currents, which can then potentially reduce the cable diameter, weight and cost of the wire harness. Semiconductor switches are also resettable remotely, which means that the fuses do not have to be easily accessible, giving designers the ability to place the fuses in locations that can reduce cable lengths from the power source to the load.

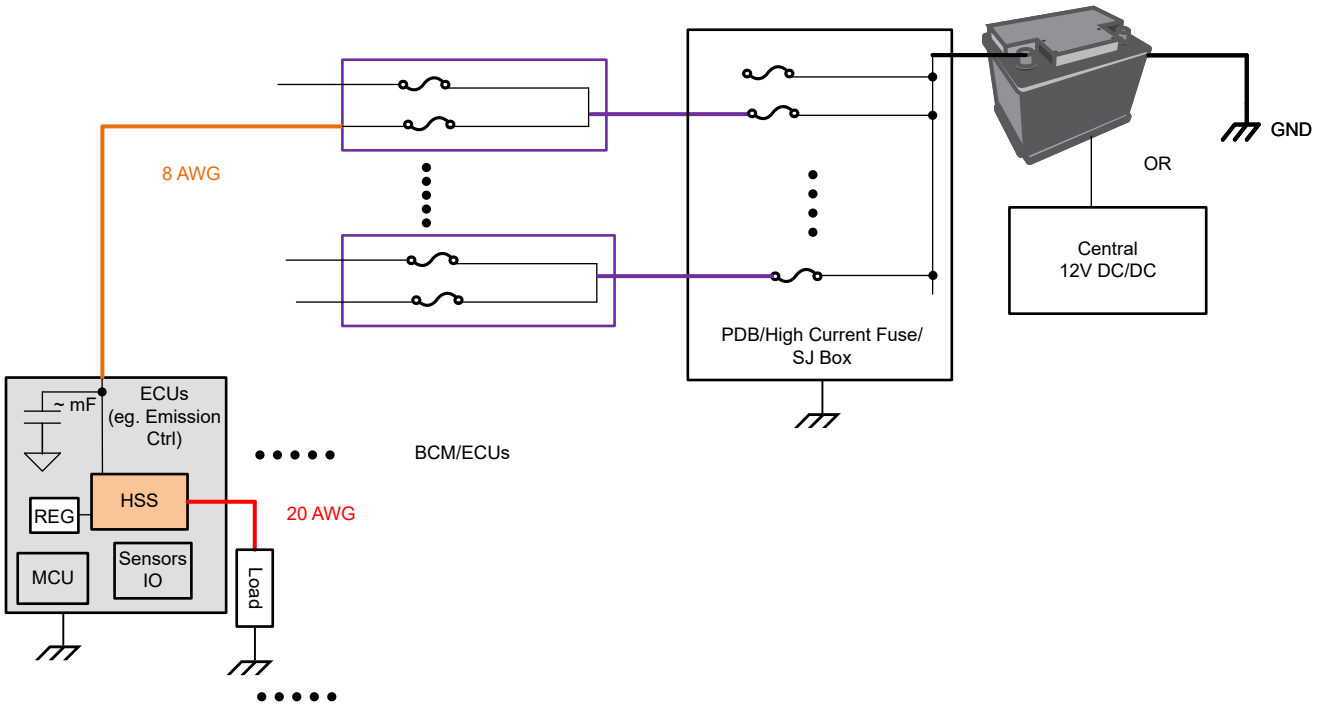

Figure 1. *Domain-based Power distribution architecture.*

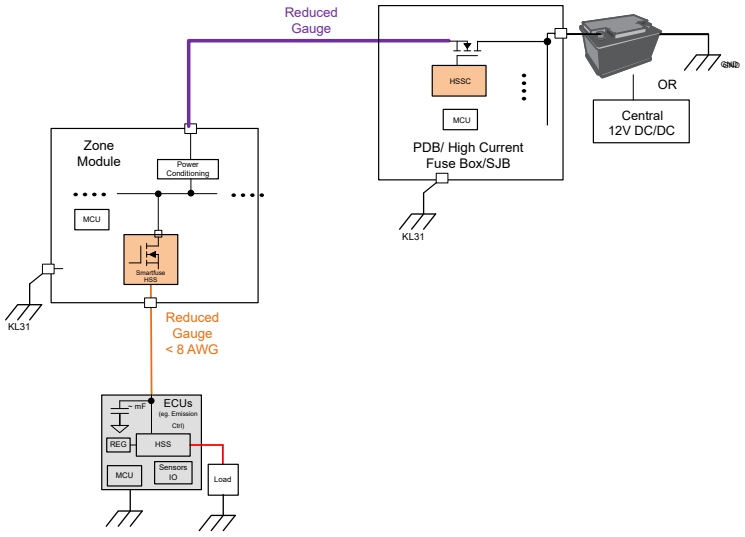

Figure 2. *Zone-based Power distribution architecture.*

The system design challenges when using semiconductor switches as smart fuse devices include lowering the quiescent current when the switch is in the on state, as well as turning on outputs powering large capacitive loads typically seen at the load (the electronic control unit [ECU] input). ECUs have an input capacitance ranging from 47µF to 5mF and startup time considerations (fast charging time <1ms, medium charging time <10ms, slow charging time <50ms) based on the ECU type and number of ECUs connected together on each Power Distribution Box (PDB) output. Charging these ECU input capacitors through the metal-oxide semiconductor field-effect transistor (MOSFET) switch within the ECU startup time is one of the primary system design challenges of a zone-based architecture.

In this article, we'll discuss various techniques to address the challenge of driving capacitive loads using high-side switch controllers.

Output-voltage slew-rate control

In this method, placing the capacitor (C) between gate-GND, the slew rate of the gate and the output voltage limits the inrush current. The circuit configuration with output voltage slew-rate control is shown in **Figure 3**.

Equation 1 and **Equation 2** calculate the inrush current and power dissipation at startup as:

$$I_{INR} = C_{OUT} \times \frac{dV_{OUT}}{dt} \quad (1)$$

$$P_{D(Vout = 0)} = V_{IN} \times I_{INR} \quad (2)$$

Because the MOSFET is operating in a saturation region, the inrush current should be low enough to keep the power dissipation within its safe operating area (SOA) during startup. MOSFETs can handle more energy (1/2 $C_{OUT}V_{IN}^{2}$) when their power dissipation is reduced and spread over longer durations. Thus, the inrush interval needs to stretch out over a longer period of time to support higher capacitive loads.

This method is suitable for slow charging requirements (for example, 5mF and 50ms), but the design must always include a trade-off between C_{OUT}, the FET SOA, the charging time and the operating temperature. For example, charging 5mF to 12V takes 40ms with an inrush current limit of 1.5A using TI's high-side, switching controller, the **TPS1211-Q1** as gate driver. Reference [**11**] iterates a procedure on how to check the FET SOA during startup using this method, while reference [**2**] is an online tool for estimating the SOA margin for a specific MOSFET.

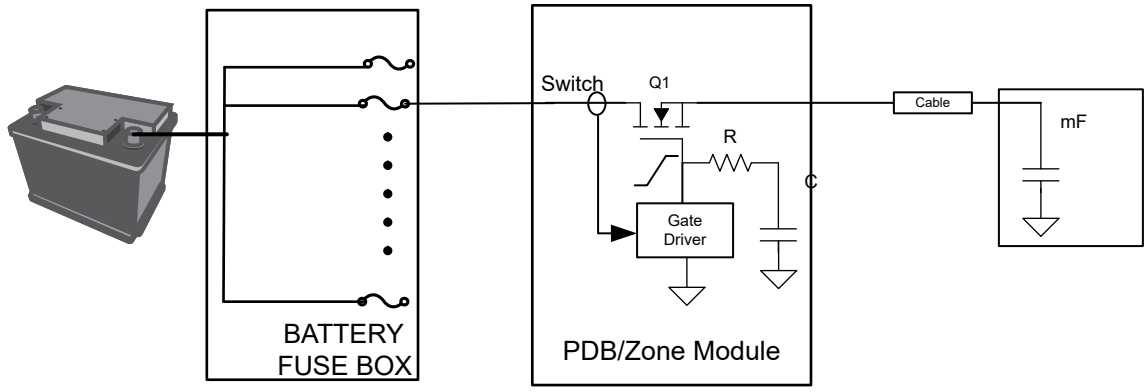

Figure 3. *Circuit for output voltage slew-rate control.*

Parallel precharge path

This approach is typically used in high-current parallel FET-based designs that need an additional gate driver to drive a precharge FET, as shown in **Figure 4**. You can use **Equation 3** to select the precharge resistor (Rpre-ch) in the precharge path to limit the inrush current to a specific value:

$$R_{pre-ch} = \frac{V_{IN}}{I_{INR}} \quad (3)$$

Because the precharge resistor handles all of the power stress during startup, it should be able to handle both average and peak power dissipation, expressed by **Equation 4** and **Equation 5**:

$$P_{avg} = \frac{E_{pre-ch}}{T_{pre-ch}} = \frac{0.5 \times C_{OUT} \times V_{IN}^2}{5 \times R_{pre-ch} \times C_{OUT}} \quad (4)$$

$$P_{peak} = \frac{V_{IN}^2}{R_{pre-ch}} \quad (5)$$

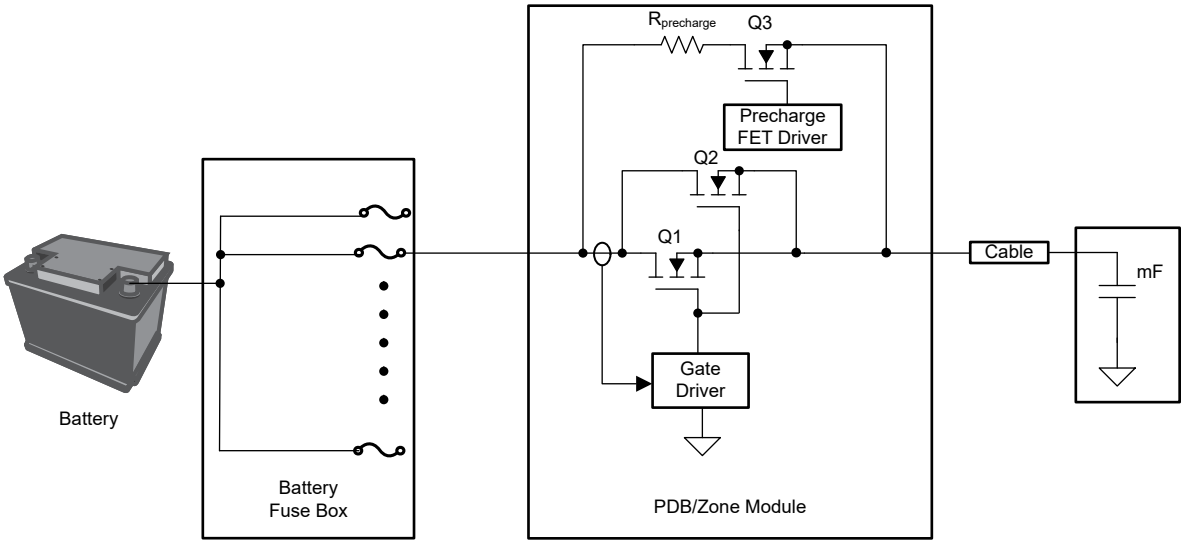

Figure 4. *Circuit with a precharge resistor and FET in a parallel path.*

In this case, fast output charging is possible – at the cost of a very bulky precharge resistor. For example, charging 5mF to 12V in 10ms would require a 0.4Ω precharge resistor at a 36W rating with a peak power-handling capacity of 360W, resulting in a bulky wire-wound resistor. Thus, this solution is not viable for many types of end equipment, as there are many channels on the same PCB. Each channel would need a bulky resistor, resulting in a space-inefficient solution.

Automatic PWM-based capacitor charging

As shown in **Figure 5**, the high-side driver outputs in the PCB connect to remote ECUs through lengthy cables varying from 1m to several meters. As an example, a 50A wire (8AWG) harness has 2mΩ-per-meter and 1.5µH-per-meter characteristics. The D1 diode is a part of the system design that allows the freewheel path for the cable harness inductive current. The high-side drivers have strong gate-drive outputs capable of driving FETs in parallel with short (<1µs) turnon and turnoff times, providing overcurrent and short-circuit protection. The cable parasitic, D1 diode and high-side MOSFETs form a typical buck regulator configuration.

During startup, the uncharged output capacitor draws inrush current and triggers a short-circuit event when the inrush current hits the short-circuit protection threshold (I_{SCP}). The high-side driver turns off the power path and reinitiates turnon after a retry period ($T_{AUTO-RETRY}$). This process continues until the output capacitance is fully charged, as shown in **Figure 6**, after which the high-side driver goes into normal operation and drives the load.

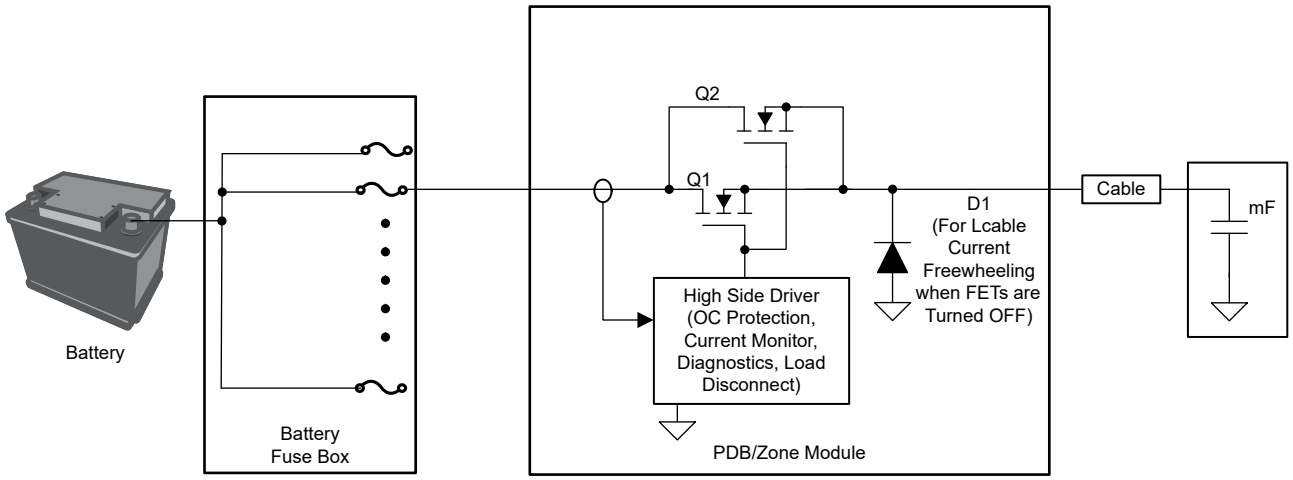

Figure 5. *Circuit representation for pulse-width modulation (PWM) charging using a high-side driver.*

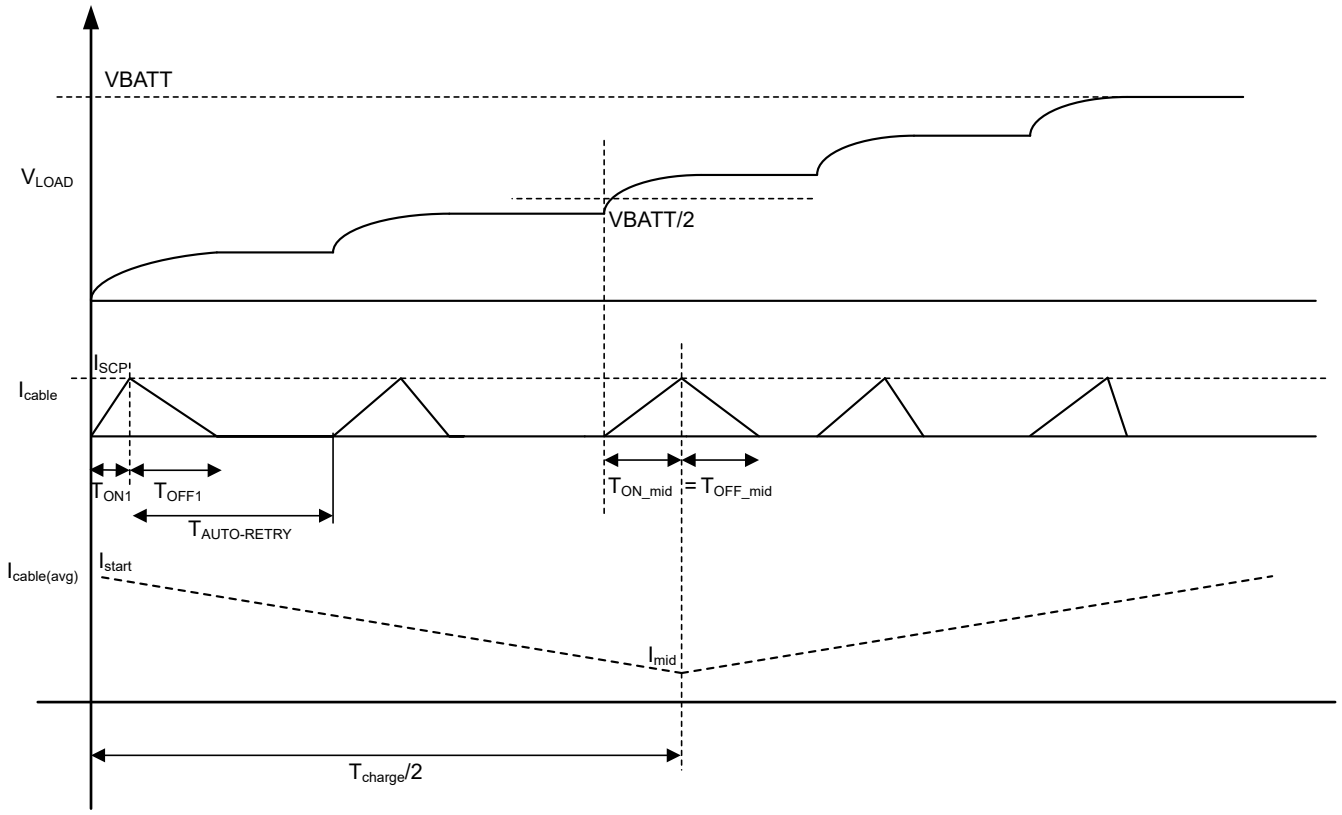

Figure 6. *PWM charging method conceptual waveforms during startup.*

Figure 7 illustrates the control operation. As you can see, this approach has two variables, I_{SCP} and $T_{AUTO-RETRY}$, which need to be set for the high-side driver based on the input voltage (V_{IN}), load capacitance and required charging time. A higher I_{SCP} threshold or a shorter $T_{AUTO-RETRY}$ delay allow faster output charging, making the solution universal for any value of load capacitance.

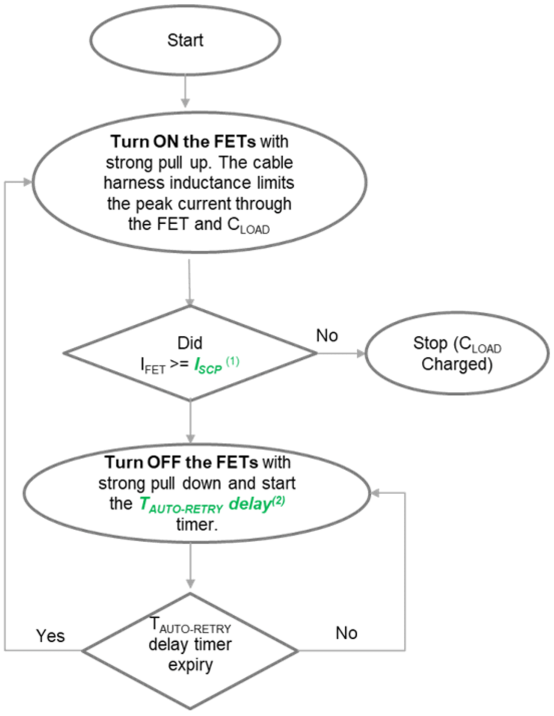

Figure 7. *Flow chart of the PWM charging control method.*

This solution leverages the existing available real estate in a typical high-side driver system (the cable harness inductance and D1 diode) and creates an efficient charging method by operating the high-side MOSFETs in switching mode. Unlike traditional approaches, the proposed solution no longer depends on the FET SOA and does not require bulky precharge resistors, nor a precharge FET and driver. The solution uses the inherent short-circuit protection feature of the high-side driver and runs autonomously without any external control signals or complex algorithms.

Design considerations and test results

Consider this system design example for a 50A load:

- Battery voltage (V_{BATT}) = 12V.
- Load capacitance (C_{LOAD}) = 5mF.
- 1.5m cable = 8AWG connecting the high-side driver to the ECU, leading to L_{cable} = 2.25µH.
- Charging time (T_{charge}) = 10ms
- Freewheeling diode drop (V_{D1}) = 0.7V.

The design involves selecting the I_{SCP} and $T_{AUTO\text{-}RETRY}$ parameters. For a 50A load design, the I_{SCP} threshold is usually set at 20% above the maximum load current, so in this example, that would be 50A × 1.2 = 60A.

Now, to compute $T_{AUTO\text{-}RETRY}$, see **Figure 6** and use the current-voltage relationship of the capacitor at the midpoint of $T_{charge}/2$ to get **Equation 6**:

$$\frac{(I_{start} + I_{mid})}{3} \times \frac{T_{charge}}{2} = C_{LOAD} \times \frac{V_{BATT}}{2} \quad (6)$$

where:

$$I_{start} = \frac{I_{SCP} \times (T_{ON1} + T_{OFF1})}{2 \times (T_{ON1} + T_{AUTO-RETRY})} \quad (7)$$

and

$$I_{mid} = \frac{I_{SCP} \times 2 \times T_{ON\_mid}}{2 \times (T_{ON\_mid} + T_{AUTO-RETRY})} \quad (8)$$

The time intervals TON1, TOFF1 and TON_mid can be calculated using **Equation 9** to **Equation 11**:

$$T_{ON1} = \frac{L_{cable} \times I_{SCP}}{V_{BATT}} \quad (9)$$

$$T_{OFF1} = \frac{L_{cable} \times I_{SCP}}{V_{D1}} \quad (10)$$

$$T_{ON\_mid} = \frac{L_{cable} \times I_{SCP}}{\left(\frac{V_{BATT}}{2}\right)} \quad (11)$$

Substituting the known parameters V_{BATT}, L_{cable}, I_{SCP}, V_{D1} and C_{LOAD} and solving for $T_{AUTO\text{-}RETRY}$ gives a retry delay of <200µs to achieve a charging time of 10ms.

Figure 8 and **Figure 9** show the application schematic and test setup to charge a 5mF load capacitance using the TPS1211-Q1 high-side driver. $T_{AUTO\text{-}RETRY}$ is 180µs, which results in a charging time of 7ms, as shown in **Figure 10**.

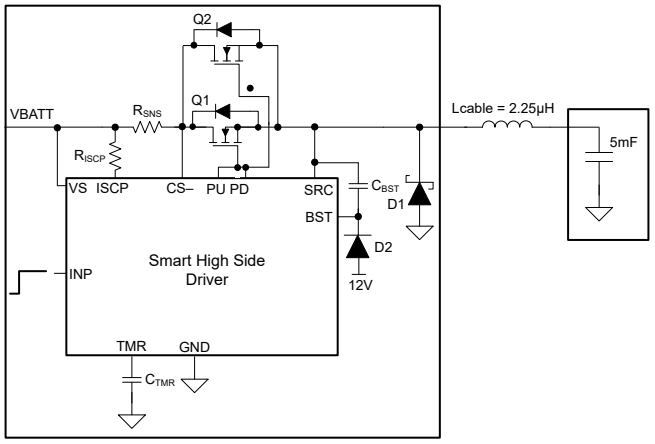

Figure 8. *Typical application schematic for driving a capacitive load.*

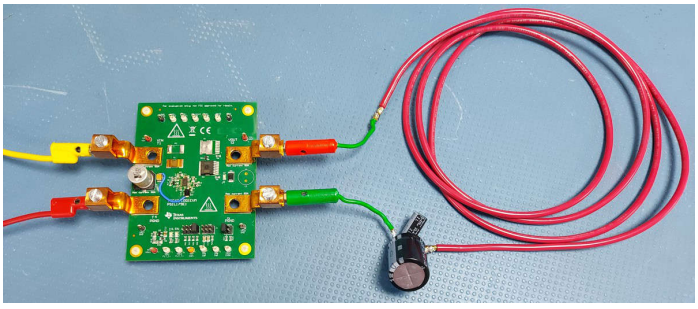

Figure 9. *Test setup using the TPS1211-Q1 evaluation module with a 1.5m cable harness.*

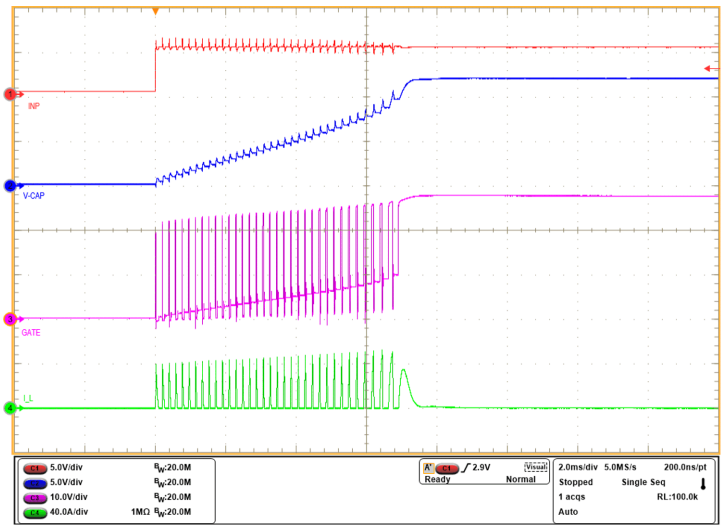

Figure 10. *Startup with a 5mF load capacitance using the TPS1211-Q1 in switching mode.*

Conclusion

Semiconductor-based smart fuse solutions are gaining popularity over traditional melting fuses in automotive power distribution given their significantly improved fuse time-current characteristics and resettability through software. These benefits enable a reduction in overall cable harness weight because the cables are thinner and shorter.

One of the system design challenges with semiconductor-based smart fuse solutions is whether the capacitor load charging can meet the system startup time requirements. TI's high-side switch controller devices offer various techniques to address the challenges of capacitive load driving.

References

1. Rogachev, Artem. 2014. "**Robust Hot Swap Design**." Texas Instruments application report, literature No. SLVA673A, April 2014.
2. **FET SOA Margin Calculator for dv/dt-Based Startup**

Related Websites

- **TPS1211-Q1**
- **TPS1200-Q1**

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