Solving AC dropout recovery in a high-density GaN-optimized PFC converter

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Introduction

A loss of power in data center server power-supply units can interrupt everything from entertainment to financial transactions to home security systems. Specifications such as the V2 Power Shelf Specification from the Open Compute Project (OCP) [1] emphasize the need to reduce server downtime with robust AC dropout control algorithms. In addition, the need for cost-effective solutions in data centers to improve power factor correction (PFC) light load and peak efficiency while shrinking passive components is becoming difficult with conventional continuous conduction mode control [2-8].

To address this problem, TI developed a gallium nitride (GaN)-based high-density design using two-phase integrated triangular current mode (iTCM) PFC (**Figure 1**) [9]. Low-value inductors operating at a high frequency have enabled the high efficiency (>99%) and power density (120 W/in^3) of this design. These small inductors present a unique problem to AC dropout recovery in that only a few microseconds of switch on-time can result in over 70 A of switch current. In addition, any delays in timing can also result in significant reverse current, further exacerbating PFC recovery. Keeping the current levels at a safe magnitude and preventing reverse current required the development of a new solution to the AC dropout and recovery problem. This article discusses this solution with lab verification data based on the Variable-Frequency, ZVS, 5-kW, GaN-Based, Two-Phase Totem-Pole PFC Reference Design [10], for which **Table 1** lists the primary components and system specifications.

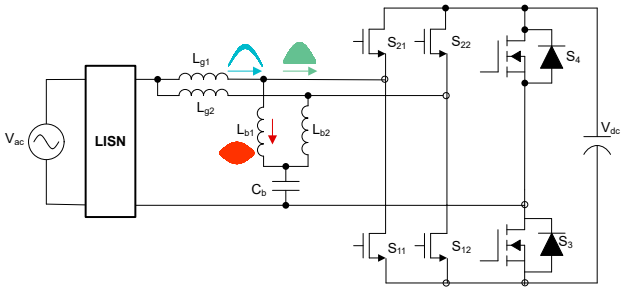

Figure 1. *iTCM topology with inductor and current envelopes.*

Parameters	Value
AC input	90 V-264 V
Line frequency	50-60 Hz
DC output	400 V
Maximum power	5 kW
Holdup time at full load	20 ms
L_g, low-frequency inductor	140 µH
L_b, high-frequency inductor	14 µH
C_b, high-frequency blocking capacitor	1.5 µF
Total harmonic distortion (THD)	OCP v3
Electromagnetic interference (EMI)	European standard (EN) 55022 Class A
Operating frequency	Variable, 75 kHz-1.2 MHz
Microcontroller	TMS320F280049C [11]
High-frequency GaN field-effect transistors (FETs) (S_{11}, S_{12}, S_{22}, S_{21})	LMG3526R030 [12]
Low-frequency silicon FETs (S_3, S_4)	IPT60R022S7XTMA1
Dimensions	38 mm ´ 65 mm ´ 263 mm
Power density	120 W/in^3

Table 1. *iTCM topology with inductor and current envelopes.*

Topology overview

The topology uses two phases operating 180° out of phase with a single DC blocking capacitor, C_b, taking advantage of the ripple current cancellation provided by the two-phase architecture and reducing the root-mean-

square (RMS) current stress in C_b. L_{b1} and L_{b2} are sized to process the high-frequency AC ripple current necessary for TCM operation, removing the DC bias burden required for the inductor used in TCM, as defined in [5]. Using ferrite cores for L_{b1} and L_{b2} ensures low loss in the presence of the high flux swings necessary for zero voltage switching (ZVS). L_{g1} and L_{g2} are larger in value than L_{b1} and L_{b2} (approximately 10 times larger), preventing most of the high-frequency current from flowing into the input source and subsequently improving EMI. In addition, the reduced ripple current in L_{g1} and L_{g2} enables the possible use of lower-cost core materials. **Figure 1** also illustrates the ripple current envelopes for the inductors and switch nodes.

AC dropout technical challenges

The first challenge that I want to highlight is reverse-current generation when the AC input voltage disappears. Since all of the switches in the totem-pole PFC topology are bidirectional, it is essential that the FETs operating as synchronous rectifiers shut off as quickly as possible when removing AC. This shutoff prevents the generation of a negative current that will cause the output voltage to discharge and reduce the available holdup time. **Figure 2** illustrates the path for generating this negative current for the synchronous conduction interval during the positive half cycle. In addition, any substantial delays in turning off the synchronous rectifiers can also result in a large current spike capable of activating overcurrent protection (OCP). For example, if the synchronous rectifier stays on when no input voltage is present, you can solve $V_{dc} = L_{b1} \cdot \frac{dI_1}{dt}$ for the amount of time it takes to generate 70 A of current, namely 2.5 µs. This short time presents a significant problem for the AC dropout detection to identify the problem and stop switching before the system hits OCP or causes damage.

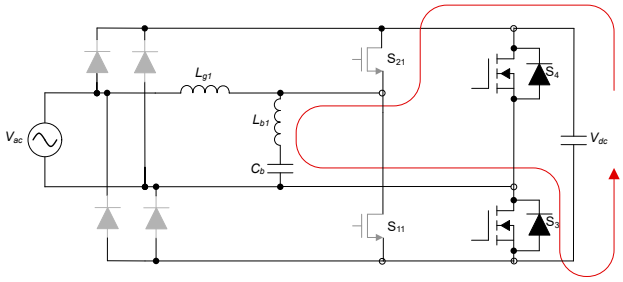

Figure 2. *Synchronous rectifier S_{21} delayed turnoff V_{dc} discharge path.*

The second challenge is resuming operation of the PFC after restoring AC. The central issue of this event comes from the fact that the bypass diodes on the PFC charges the output voltage to the peak of the input sine wave, which occurs most readily at high line when the output voltage has fallen well below this peak value. During these events, the converter has no mechanism to stop the current, making the surge current very large. Improper control of the switches during these events can make things much worse by saturating the inductors, creating OCP events and further discharging the output voltage. The need for a precise control algorithm during this time is again multiplied by the high-frequency operation point of the iTCM topology with the small-value inductors used for L_{b1} and L_{b2}.

AC dropout solution

In order to precisely determine the presence and absence of the AC input, the solution uses a virtual AC input signal that monitors the integrity of the actual AC input. This virtual signal is generated by measuring the input voltage amplitude, frequency and phase, such that during normal operation it tracks the 50- and 60-Hz component of the actual AC input nearly perfectly. The system can easily recognize the presence and absence of the AC input voltage by comparing the actual input to the virtual input. Any sudden changes in the difference between these two signals indicates an input transient event. It is this transient event that is used to detect both the loss and restoration of the AC input voltage. **Figure 3** illustrates the virtual AC input, along with the actual input during a dropout event.

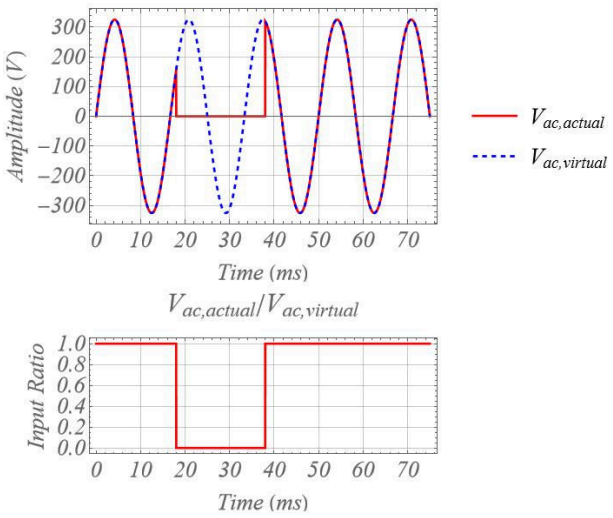

Figure 3. *AC input dropout with the virtual AC signal.*

Figure 4 illustrates the state machine that governs the dropout and restore process. During startup, the system goes through an initialization cycle (Sync Init) where it determines the RMS input voltage magnitude. It uses a software phase-locked loop (SPLL) to ensure that the phase of $V_{ac,virtual}$ matches $V_{ac,actual}$. Once the SPLL is locked (Sync On), the processor monitors the ratio between $V_{ac,actual}/V_{ac,virtual}$ (see **Figure 3**). If this ratio is less than the target threshold, then a dropout event is declared and switching stops immediately (Stop State). From here, the system clears any faults that occurred and goes into a standby state (Ready), where it monitors the $V_{ac,actual}/V_{ac,virtual}$ ratio to determine when it goes above the resume threshold. Once the state machine has determined that AC is restored, it resumes switching immediately and resynchronizes the SPLL (Resume State). By using the $V_{ac,actual}/V_{ac,virtual}$ ratio in concert with the SPLL, the algorithm is able to determine the AC dropout and restore times for any input voltage or frequency. In addition, since the algorithm always monitors the ratio $V_{ac,actual}/V_{ac,virtual}$, it is able to respond more quickly than a traditional level-based-solution that detects when the AC input voltage goes to zero. Level-based monitoring for dropout can create delays that can result in large current spikes and significant reverse current.

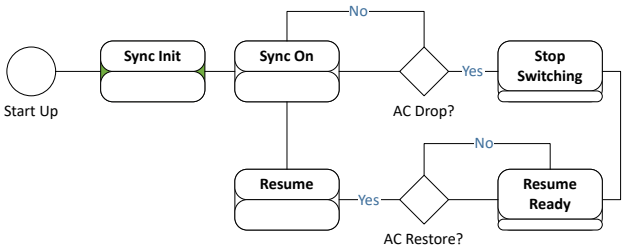

Figure 4. *AC dropout and restore state machine.*

Results

Figure 5 illustrates the performance of the two-phase iTCM totem-pole PFC with the aforementioned algorithm during an AC dropout and restore event. The AC input voltage is 230 V_{RMS} at 60 Hz and the output voltage is 400 V. The load is 5 kW (400 V, 12.5 A) of constant current with a 20-ms AC dropout event. In order to produce the worst-case stress for the system, AC was removed such that it would return at the peak of the AC line cycle. This is the worst case for inrush current, in that the input bypass diodes will cause significant inrush current into the output capacitors when the AC line peak exceeds V_{OUT}.

The waveform in **Figure 5** also provides an image zoomed in on the recovery portion of the event. It is clearly visible that the PFC switch current is well controlled and below the GaN FET OCP limit [12]. Minimized reverse current prevents unnecessary discharge of V_{OUT}. In addition, there is no abnormal behavior from the bypass diode conduction intervals, since the algorithm is able to easily determine whether the input voltage is above or equal to the output voltage.

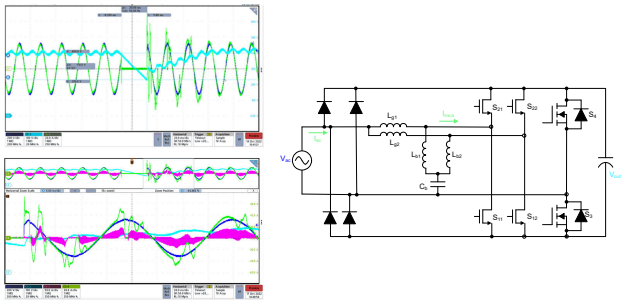

Figure 5. *AC dropout and restore performance at 5 kW.*

In addition to AC dropout, the design also delivers low THD, high efficiency, high power density and fast load transient response.

If you are interested in more details on this algorithm or other aspects of this design, you can find the full schematics, layout, bill of materials, test results and code for the two-phase totem-pole PFC reference design in reference [10].

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