Achieving high converter efficiency with an active clamp in a PSFB converter

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Introduction

Phase-shifted full-bridge (PSFB) converters (see **Figure 1**) are widely applied to high-power applications, mainly because a PSFB converter can achieve soft switching on its input switches and thus facilitate high converter efficiency [1]. Although soft switching greatly reduces switching losses, the output rectifier parasitic capacitance resonates with the transformer leakage inductors – modeled as L_r in **Figure 1** – resulting in voltage ringing with high voltage stress [2].

The voltage stress of the output rectifier could be as high as 2 x V_{IN} x N_S/N_P, where N_P and N_S are the transformer's primary and secondary windings, respectively. Traditionally, applying a passive snubber [2] (such as the resistor-capacitor-diode [RCD] snubber in **Figure 1**) at the output rectifier prevents the rectifier voltage from going too high and enables the use of a lower-voltage-rated component with a better figure of merit for lower power dissipation.

When applying metal-oxide semiconductor field-effect transistors (MOSFETs) as a synchronous rectifier (SR), you can expect lower C_{oss} and $R_{DS(on)}$ on lower-voltage-rated MOSFETs at the same cost level compared to higher-voltage-rated MOSFETs. However, using a passive snubber means that part of the energy that caused the voltage ringing will dissipate in the passive snubber and result in an efficiency reduction.

This article introduces an active (rather than a passive) snubber and its related control, which minimizes rectifier voltage stress to achieve higher converter efficiency while also greatly reducing energy dissipation in the snubber circuit and without sacrificing operational range.

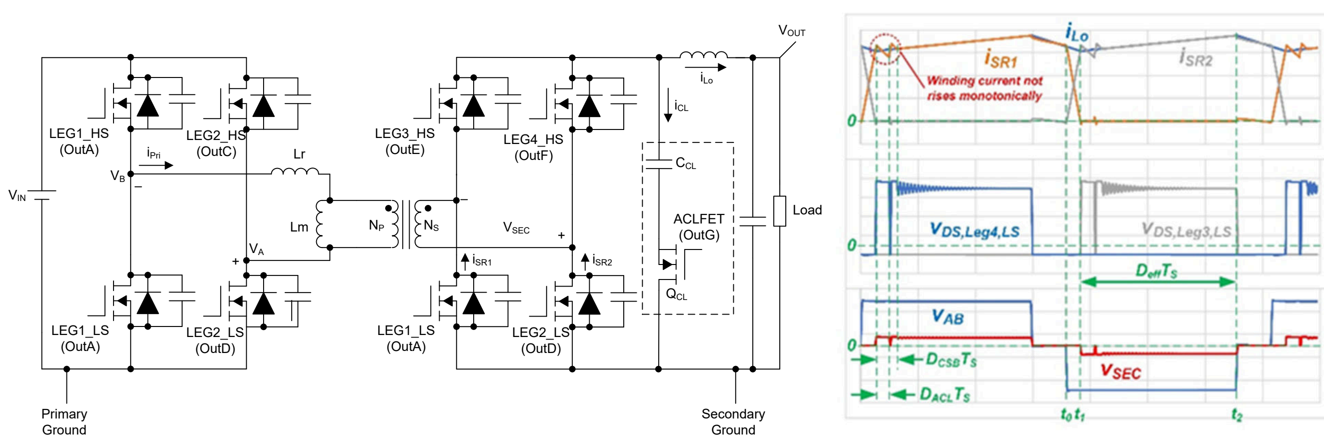

Figure 1. A PSFB power stage with a passive clamp and key waveforms.

A PSFB converter with an active clamp

As shown in **Figure 2**, inserting an active clamp leg formed by a capacitor (C_{CL}) and a MOSFET (Q_{CL}) before the output inductor enables active clamp leg current conduction within the effective duty-cycle (D_{eff}) period, thus clamping the secondary winding voltage (V_{SEC}) and rectifier voltage stress to the C_{CL} voltage – V_{CL}. In order to have low voltage stress on the output rectifier, you must select a large-enough C_{CL} for low capacitor voltage ripple. A rule of thumb is to select the inductor-capacitor (LC) resonant period formed by L_r and C_{CL} to be much longer than the switching period (T_s) [3] expressed by **Equation 1**:

$$2\pi\sqrt{\left(\frac{N_S}{N_P}\right)^2 L_r C_{CL}} \gg T_S \quad (1)$$

The rectifier voltage stress will clamp to around $V_{IN} \times N_S/N_P$ with the active snubber, which is about half of the voltage stress without any clamp circuit.

Unlike a passive snubber, an active snubber doesn't dissipate the ringing energy on the power resistor. Instead, it circulates the energy in the LC resonant tank as a lossless snubber. When the output winding voltage becomes nonzero, energy will transfer from the primary winding to the secondary winding to energize the output inductor and conduct current through the Q_{CL} body diode, even if Q_{CL} isn't turned on. Turning on Q_{CL} after its body has already conducted current will ensure zero voltage switching (ZVS) on Q_{CL}. Therefore, you can expect higher converter efficiency on a PSFB converter with an active snubber over a PSFB converter with a passive snubber in an identical specification.

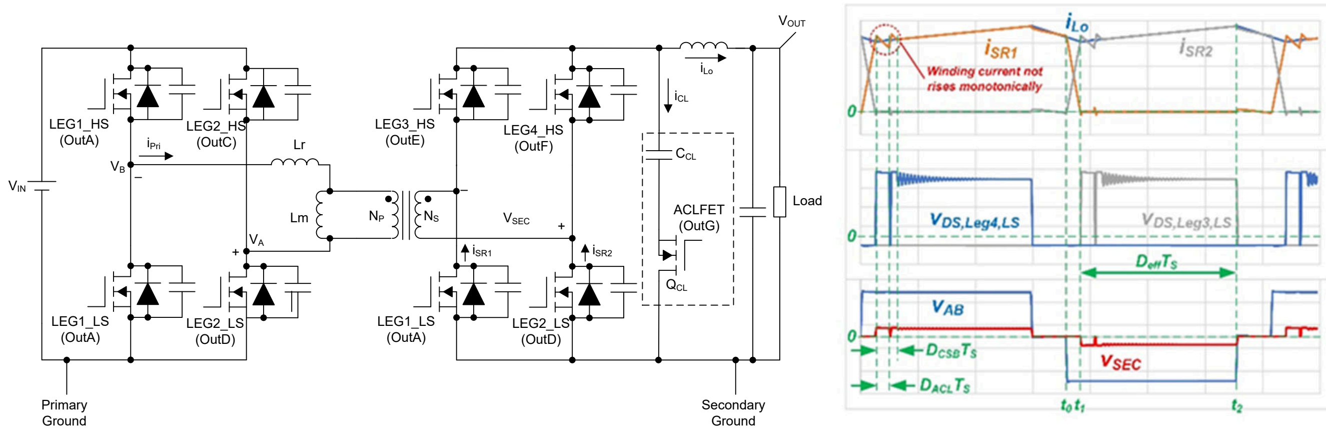

Figure 2. *A PSFB power stage with active clamp and key waveforms.*

Active clamp leg design considerations

With the active snubber implemented in a PSFB, the transformer winding current will no longer rise monotonically during the effective duty cycle (D_{eff}) period (T_S) (non-zero output winding voltage period) like output inductor current. This is because the active snubber capacitor energy also participates in energizing output inductor rather than solely rely on energy transfer from the input side. The non-monotonic current ramp characteristic could make peak current mode control difficult as input or transformer winding current are generally utilized for peak current detection and higher input or transformer winding current does not necessarily represent larger duty cycle.

In order to allow peak current detection happens when current is rising monotonically, we must ensure $D_{eff}T_S$ is always greater than the duration where current-second balance is completed – $D_{CSB}T_S$ – under whole operational voltage and load ranges. As high efficiency is expected for a PSFB with larger D_{eff}, PSFB is generally designed to have larger D_{eff} at mid-to-heavy load where $D_{eff} >> D_{CSB}$ is expected. At light load, converter is expected to operate under discontinuous conduction mode where D_{eff} will be smaller than D_{eff} under continuous conduction mode at the same input/output voltage condition. In order to keep $D_{eff}T_S$ greater than $D_{CSB}T_S$ even at light load, we have implemented frequency reduction control based on load current.

The duration of $D_{CSB}T_S$ becomes an important factor for peak current mode control. How long does it take to complete current-second balance is now the one-million-dollar question. To answer this question, you'll need to calculate current flow through the active clamp leg.

Assuming that V_{CL} is a constant and $L_m = \infty$, **Equation 2** expresses the rectifier current changing rate during the duty-cycle loss period (the period where $V_{SEC} = 0$ and i_{SR1} and i_{SR2} are commuting) as:

$$\frac{\Delta i_{SR}}{\Delta t} = \frac{N_p}{N_S}\frac{V_{Lr}}{L_r} = \frac{\frac{N_S}{N_P}V_{IN} - V_{CL}}{\left(\frac{N_S}{N_P}\right)^2 L_r} \quad (2)$$

where V_{Lr} is the voltage across L_r.

Equation 3 calculates the changing rate of the output inductor current:

$$\frac{\Delta i_{LO}}{\Delta t} = \frac{V_{CL} - VOUT}{L_O} \quad (3)$$

Using **Equation 2** and **Equation 3** along with Kirchhoff's current law, **Equation 4** calculates the changing rate of the active clamp current:

$$\Delta i_{CL} = \Delta i_{SR} - \Delta i_{Lo} = \left[\frac{\frac{N_S}{N_P}V_{IN} - V_{CL}}{\left(\frac{N_S}{N_P}^2\right)L_r} - \frac{V_{CL} - V_{OUT}}{L_O}\right] \quad (4)$$

Δt

Since $V_{CL} \approx V_{IN} \times N_S/N_P$ [**3**], you just need to apply the total active clamp leg conduction time as Δt in **Equation 4** to solve Δi_{CL}. However, you still need to know the peak value of i_{CL} in order to calculate the i_{CL} root-mean-square (RMS) value. As shown in **Figure 3**, if $i_{SEC} = i_{Lo}$ (after charging C_{oss} to V_{CL}) at time t_2 and $i_{SEC} = i_{SR}$ at time t_3 (start to charge C_{CL}), **Equation 5** derives $i_{CL,peak}$ as:

$$i_{CL,peak} = \Delta i_{CL}\,|_{t3-t2} = i_{CL}|_{t3} = (i_{SR} - i_{LO})|_{t3} - (i_{SR} - i_{LO})|_{t3} = i_{SEC}|_{t3} - i_{SR}|_{t2} = \Delta i_{SEC}|_{t3-t2} - 2i_{SRS}|_{t2} \approx -2i_{SRS}|_{t2} \quad (5)$$

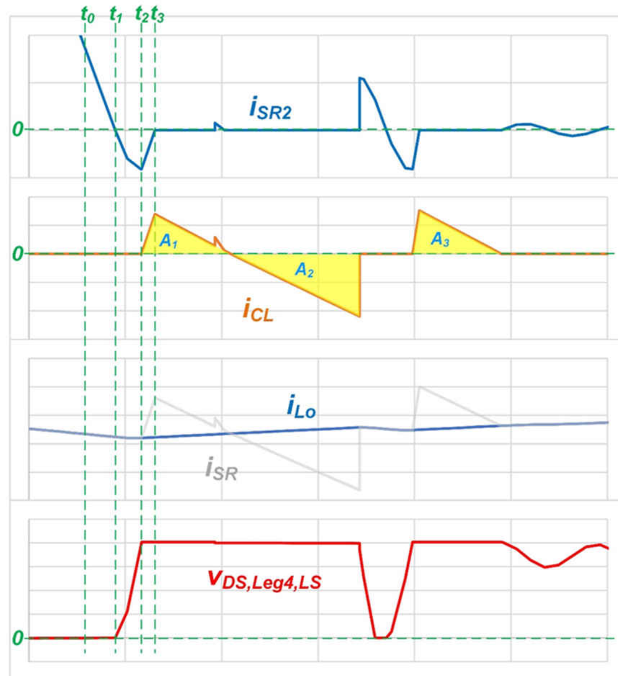

***Figure 3.** Key waveforms around the active clamp current conduction period.*

With **Equation 6** deriving the i_{SR2} value at t_2 as:

$$i_{SR2}|_{t2} = \frac{V_{IN}}{\frac{N_S}{N_P}L_r} - (t_2 - t_1) \quad (6)$$

Assuming that the i_{SR2} current decreasing rate from t_0 to t_2 is the same, **Equation 7** derives the time duration of t_2-t_1 as:

$$(t_2 - t_1) = \sqrt{2C_{OSS}\frac{N_S V_{CL} L_r}{N_P V_{IN}}} \quad (7)$$

Since C_L needs to maintain a current second balance, the sum of areas A1 and A3 will equal area A2.

As shown in **Equation 7**, SR C_{oss} controls the peak current on the active clamp leg. If you select a low C_{oss} SR FET, the active clamp leg RMS current is lower and thus helps improve converter efficiency.

Here are some design guidelines when designing a PSFB converter with an active snubber:

- QCL must turn on only after the duty-cycle loss duration in order to avoid CCL energy backflow to the primary side.
- QCL must be turn on while the body diode is still conducting current for ZVS.
- A longer QCL on time will reduce VCL as well as SR voltage stress, but the QCL RMS current will increase.
- A lower SR Coss will not only help reduce the active clamp leg RMS current, but also help reduce SR voltage stress.

The active clamp method isn't limited to full-bridge rectifiers; it is applicable to other types of rectifiers such as current-doubler [4] or center-taped rectifiers. **Figure 4** shows a PSFB converter with an active clamp on a center-taped rectifier, which is implemented in the **3-kW Phase-Shifted Full Bridge with Active Clamp Reference Design with >270-W/in^3 Power Density**.

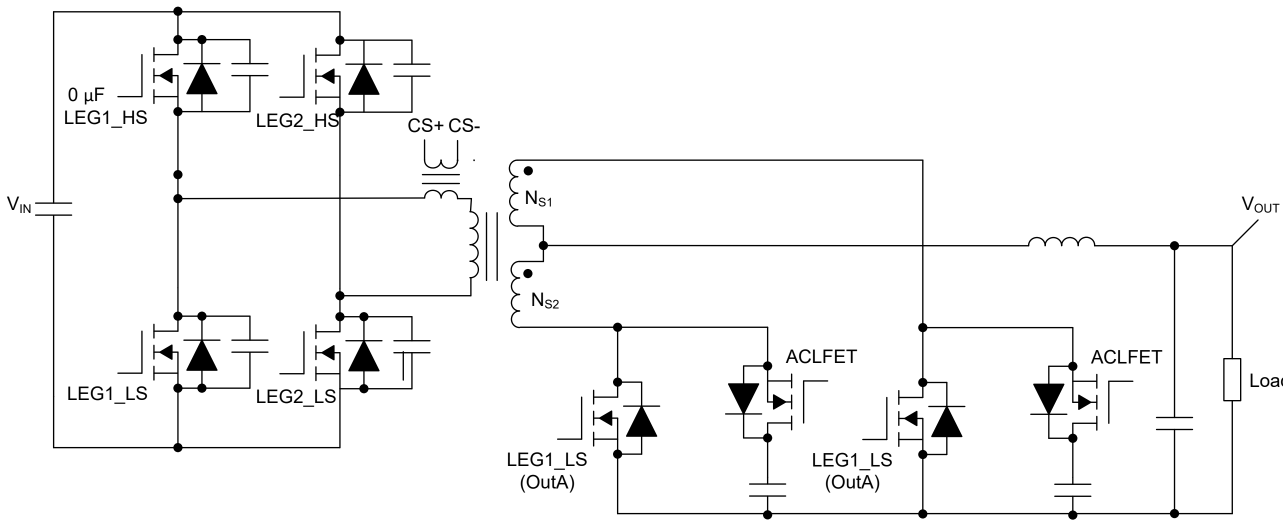

Figure 4. *A PSFB converter with active snubbers on a center-taped rectifier.*

As shown in **Figure 5**, it is possible to clamp SR voltage stress under 40 V with dual active clamp legs, with negligible clamping loss (very minor conduction loss) at a 250-A load current.

Figure 5. *Steady-state waveform of a PSFB converter with a center-taped rectifier and active snubbers at a 12-V/3-kW output.*

Summary

A control method allows PSFB converter to work with active snubber under peak current mode control is discussed in this paper. The active snubber allows lower voltage stress on the output rectifier with negligible power dissipation on the snubber circuit that greatly improves converter efficiency. The current disturbance introduced by the active snubber makes peak current mode control difficult. With the active snubber power switch on-time fixed and frequency reduction control implemented, a high efficiency and peak current controlled PSFB converter can be realized. A 400Vin, 12Vout/3kW PSFB prototype is built with the proposed control method has been verified across whole operational load range with output rectifier voltage stress limited below 40 V at 250A full load.

References

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