Common mistakes made in controller designs for power converters

By Mathew Jacob
Applications Engineer, CCP, Santa Clara

Introduction

In the course of my work as an applications engineer, I've encountered situations where designers who are used to working with converters with integrated field-effect transistors (FETs) begin using controllers as their current needs increase. It's at this point that there are tendencies to overlook some design aspects, much like blind spots while driving. This article describes the most common mistakes in controller-based designs, with some best practices that can help prevent those mistakes.

Why choose a controller?

Controllers typically come into play when the output current requirements exceed 5 A. The primary reason is obviously thermal management. In some cases, the goal may be to hit an efficiency number and a controller must be chosen that provides flexibility in sizing the FETs. Another case may be that the current requirement is 10 A. Either a converter or a controller would work well, but a controller is selected because it's reusable. A 10-A controller design can be modified for a 20-A rail by changing external components such as FETs and the inductor. Such designs are often used as a building blocks for various output voltages and currents. However, mistakes can happen when a building block is copied over to another design.

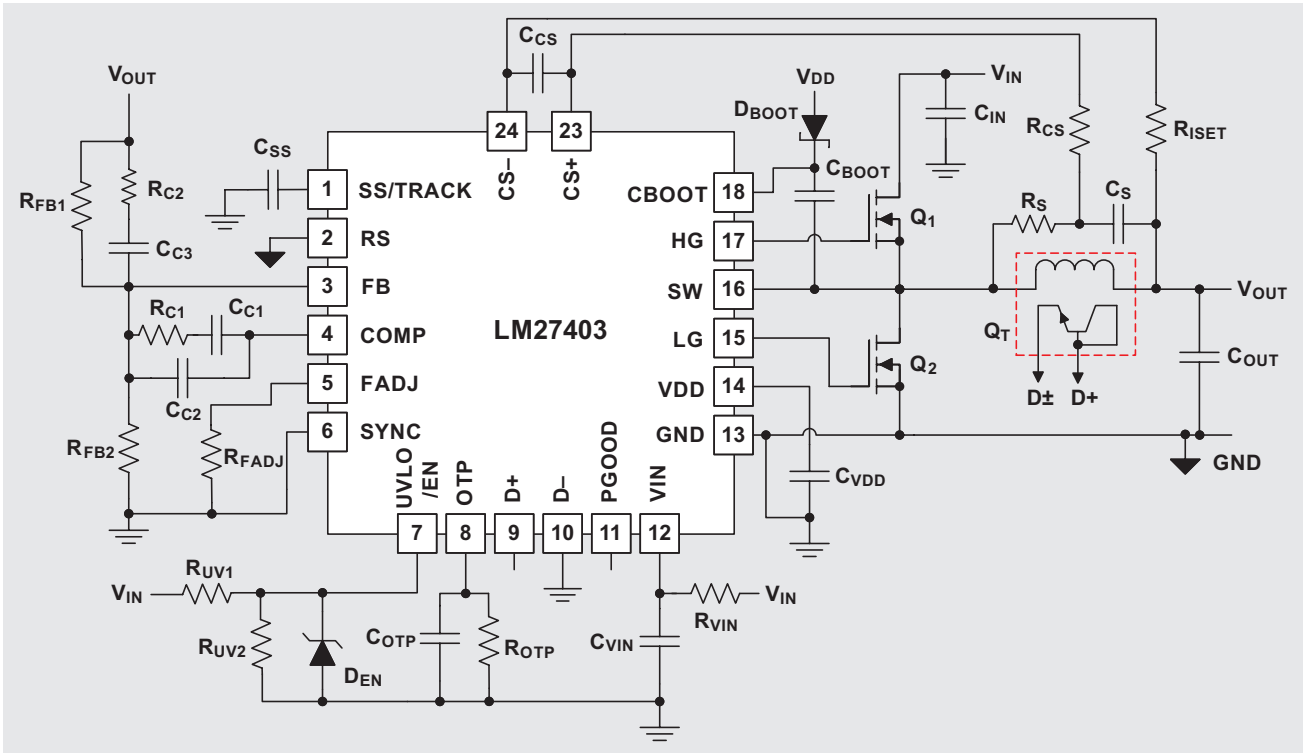
Mistake No. 1: Mismatch of the controller's V_{CC} current capability, operating frequency and chosen FET

As an example, TI's LM3495 specifies a V_{VLIN5} = 25 mA. This is the maximum current capability of the internal 4.7-V linear regulator. In this example, the operating frequency is set at 1.5 MHz and the control FET selected is the CSD86360Q5D NexFET™. The total gate charge (Q_g) of the control FET is 10 nC, the Q_g of the synchronous FET is 23 nC and the current demand from the linear regulator is $(Q_{g\_control} + Q_{g\_sync}) \times f_{SW}$. In this case, $(10 + 23) \times 10^{-9} \times 1.5 \times 10^{6}$ = 50 mA.

The 50-mA current demand exceeds the 25-mA current capability of the LM3495 and would cause a large droop in the linear regulator output, which means the FET gate-drive voltage will be much lower (or zero) in operation. A similar configuration would be acceptable for the LM27403, which has a V_{DD}/linear regulator output current capability of 106 mA.

In order to use the CSD86360Q5D with the LM3495, a lower switching frequency is required to operate within the capabilities of the internal linear regulator of the LM3495. For example, reducing the switching frequency to 300 kHz reduces the current demand to 10 mA. Thus, it is important to confirm that the MOSFET selected and the current capabilities of the on-device V_{CC} regulator are compatible with the design objectives.

Figure 1. Typical schematic for a LM27403-based controller design



Mistake No. 2: Component values of the DCR current-sensing filter

The key components for the direct-current resistance (DCR) current-sensing scheme are R_S, C_S, R_{CS}, R_{ISET} and C_{CS}, as shown in Figure 1.

R_{ISET} sets the actual value of the current limit based on the CS– pin current. It is important to note that the values selected for R_S and C_S are critical for accurate current measurement. Matching the time constant L/R_{DCR} (shown in Figure 2) with $R_S \times C_S$ ensures that the voltage measured across C_S is an accurate representation of the voltage measured across R_{DCR} with the inductor current flowing through it—nothing more, nothing less.

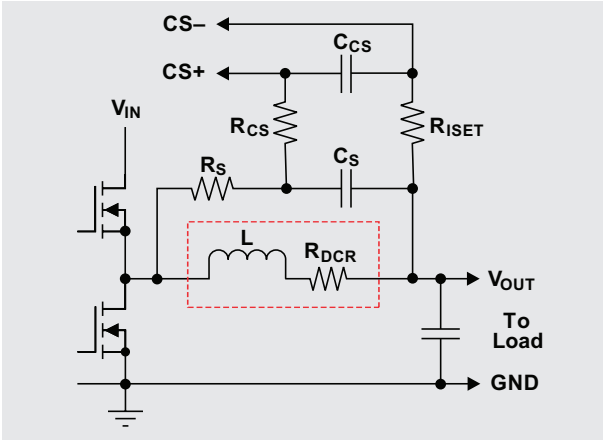
Looking at Figure 2, the goal for the design is for the RC time constant of R_S and C_S to be equal to the ratio of L/R_{DCR}, as expressed by Equation 1:

$$R_S \times C_S = L/R_{DCR} \quad (1)$$

When $R_S \times C_S$ is equal to L/R_{DCR}, the voltage developed across the sense capacitor, C_S, is a replica of the inductor DCR's voltage waveform. The recommended value for C_S is a capacitance greater than 0.1 µF to maintain low impedance on the sense network, thus reducing the susceptibility of noise pickup from the switch node.

With the power inductors providing the lowest possible DCR to minimize power losses, the typical DCRs should range from 0.4 mΩ to 4 mΩ. For a given load current of 25 A, the voltage presented across the CS+ and CS– pins

Figure 2. Details of inductor DCR sensing



can range between 10 mV and 100 mV. This small differential signal is superimposed on a large common-mode signal that is the DC output voltage, which makes the current-sense signal challenging to process.

To help reject the high-frequency common-mode noise, a series resistor (R_{CS}) can be added with the same resistance as R_{ISET} to the CS+ signal path as shown in Figure 2. A small filter capacitor (C_{CS}) added across CS+ and CS– will attenuate any noise corrupting the current-sense signal.

Now consider a 25-A application with a 1-µH, 3-mΩ inductor. With the right values for the low-pass filter (R_S, C_S) across the inductor, a 2-A peak-to-peak inductor current should produce 6 mV across C_S as shown in Figure 3.

Figure 4 shows the effect of mismatched time constants when compared to the matched time constants stated in Equation 1. The results in simulation show a large error in sensed voltage in the mismatched case.

Mistake No. 3: Excessive switch-node ringing

There are two main reasons why switch-node ringing is undesirable:

- The ringing waveform voltage can exceed the breakdown voltage of the power MOSFET.
- The ringing waveform produces radiated/conducted electromagnetic interference (EMI).

In a controller-based buck design, MOSFET selection is based on the input-voltage range. For the highest efficiency, it's best not to over-spec the voltage rating of the MOSFET. MOSFETs with higher voltage ratings are more expensive and have higher capacitances.

Designers widely use three methods to minimize switch-node ringing:

1. Careful layout of the PCB to minimize the parasitic loop inductance in the circuit.
2. A gate resistor/bootstrap resistor to slow down the turn-on of the control FET.
3. An RC snubber circuit to attenuate the ringing.

The importance of careful PCB layout cannot be over emphasized. In most cases, the root cause of ringing is a violation of the first method. If the switch-node ringing is caused by a bad layout, applying the second and third methods is like trying to fix a pipe that has a hole in it. In most designs, the second and third methods are

Figure 3. R_S = 3.3 kΩ, C_S = 0.1 µF (matches the current flow)

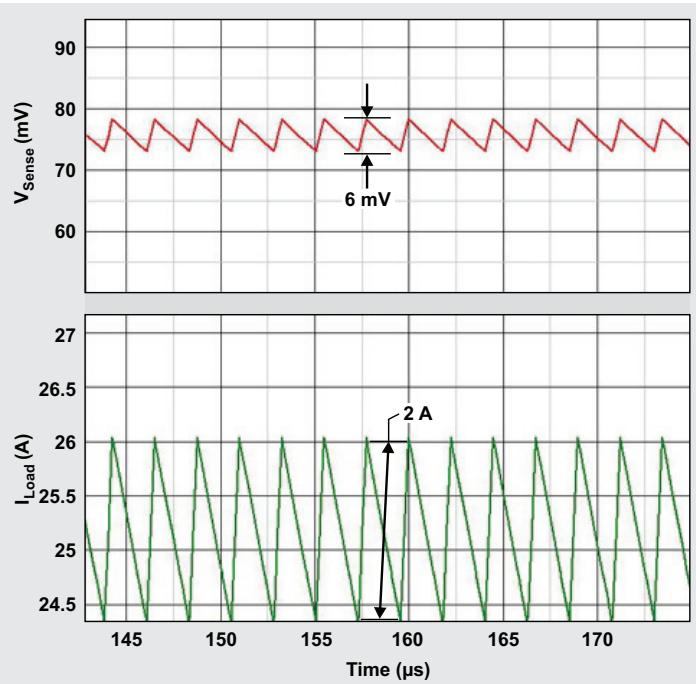
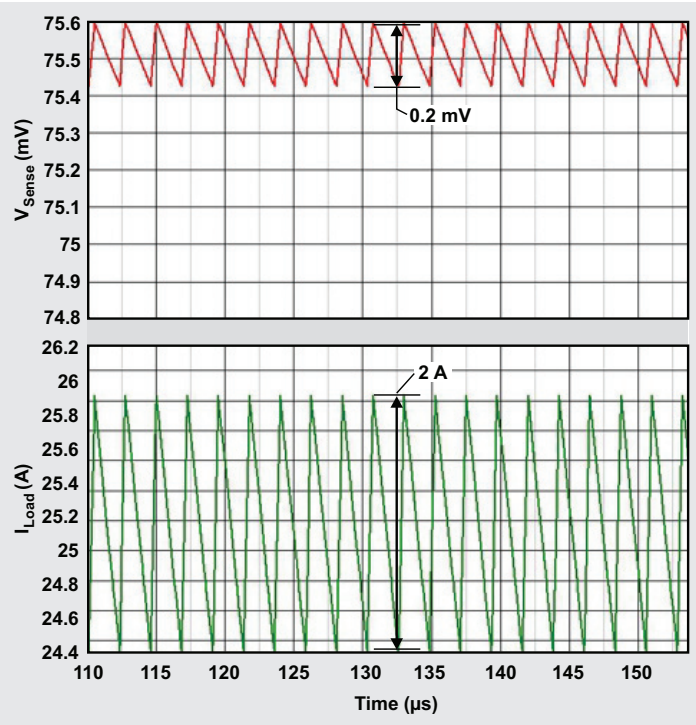


Figure 4. R_S = 100 kΩ, C_S = 0.1 µF (mismatches the current flow)



placeholders in PCB layouts to offer flexibility in taming the ringing. Figure 5 shows a PCB layout with optimized component placement.

A bootstrap resistor slows down the rising edge of the control FET, whereas the gate resistor slows down both the rising and falling edges. A good rule of thumb is to try a 4.7-Ω resistor in either location and determine the best results based on ringing improvement and efficiency. Resistor values above 10 Ω are not recommended.

A method to determine RC-snubber circuit values

The procedure for choosing the resistor and capacitor components starts with measuring the ringing frequency (f_P) of the original circuit undamped (Figure 6).

Equation 2 can be used to find R_{snub}.

$$R_{snub} = \frac{1}{4\pi \times f_P \times C_P} \quad (2)$$

where C_P = parasitic capacitance of the synchronous FET (C_{oss}) and C_{snub} = one-half to three times C_P

Another practical way to find C_{snub} is to experiment with the capacitor values in parallel with the synchronous FET. When the frequency is half the original value, the C_{snub} parallel capacitor is equal to three times the parasitic capacitance of the original circuit.

Equation 3 can be used to find the power dissipation in the snubber resistor.

$$P_{snub} = \frac{C_{snub} \times V_{snub}^2 \times f_{SW}}{2} \quad (3)$$

where V_{snub} is the maximum input voltage for a buck converter. Pay careful attention to the power dissipation of P_{snub} and select the case size of R_{snub} accordingly. For example, if V_{IN} = 15 V, C_{snub} = 1 nF, R_{snub} = 2.7 Ω and f_{SW} = 500 kHz, then P_{snub} = 0.052 W. Thus, a 0603 or 0805 case size for R_{snub} would be appropriate.

Figure 5. Optimized placement and PCB layout

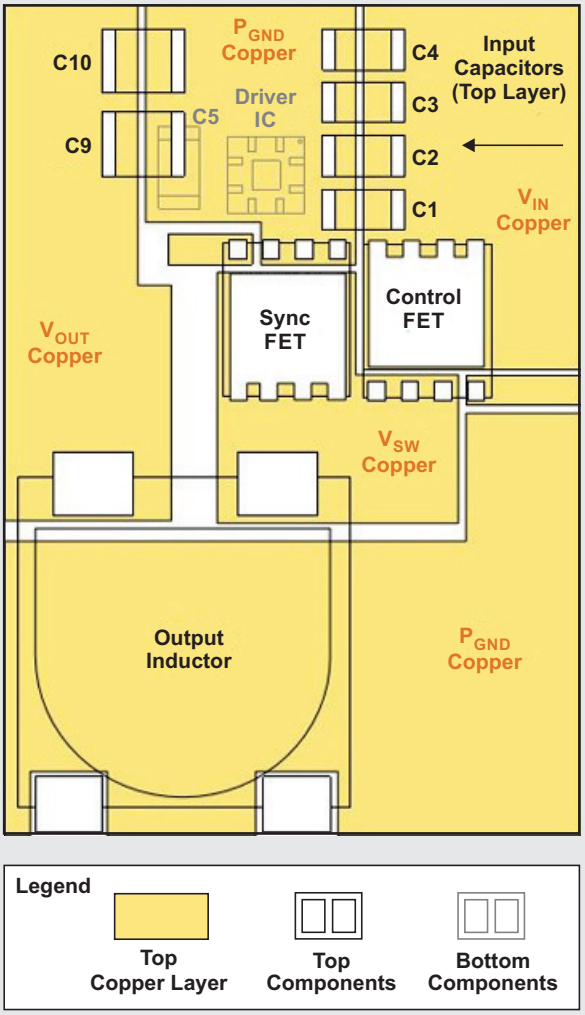
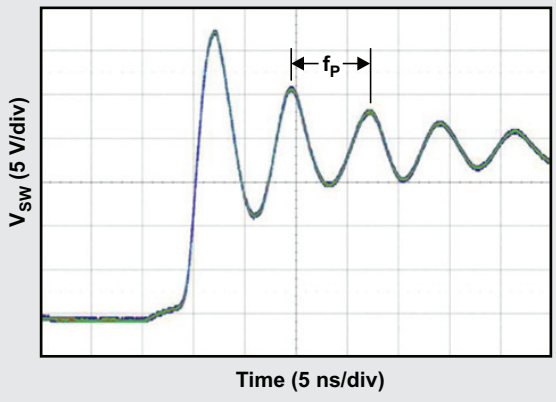


Figure 6. Determining f_P



Mistake No. 4: $C_{dv/dt}$-induced gate turn-on

The synchronous FET can be affected by the so-called "sync-FET false turn-on," which can be potentially dangerous for the MOSFET itself and the reliability of the entire converter. When the control FET turns on, a high dv/dt appears across the synchronous FET (Figure 7). Through the Miller capacitance of the FET, a capacitive current flows ($I_{DG} = C_{gd} \times dv/dt$), coupling to the gate pin of the synchronous FET (Figure 8). If the total resistance formed by the intrinsic, external and driver resistances is much lower than the equivalent MOSFET impedance between gate and source, the coupled capacitive current flows through the resistive path mentioned above.

The capacitive current causes spurious bouncing across the gate and source MOSFET pins. If the induced voltage is higher than the minimum threshold voltage, the synchronous FET can be partially turned on, creating a low-resistance path between input and ground. This causes undesired power dissipation in each switching cycle, which degrades converter efficiency, thermal management and reliability. In designs that have a wide conversion ratio and where the synchronous FET is much larger (a lower $R_{DS(on)}$) than the control FET, it is important to watch for $C_{dv/dt}$-induced gate turn-on. As a rule of thumb, it is better to avoid gate resistors for synchronous FETs.

Other common mistakes

Here are other common mistakes:

- **Incorrect pin conditions:** Use the data sheet to verify that each pin condition is satisfied. The common issues are related to unused functions and the corresponding state of the pins.
- **A crossover frequency that's too high:** Just like going over the speed limit invites trouble, selecting a crossover frequency higher than one-fifth the switching frequency is asking for trouble. Even though the phase margin may look good, the device's susceptibility to noise increases.
- **Incorrect compensation values leading to low phase and gain margins:** It's always good to verify the results on your board because the characteristics of the capacitors may be different on your board compared to generic reference designs.
- **Setting the compensation and then making a change downstream:** Changes might include replacing output capacitor types, inductor values, etc., and then forgetting to revisit compensation. Some designs are revamped later as part of cost reductions or component availability exercises. It's during these sort of changes where mistakes come into play.
- **Current-limit variation with temperature:** This seems to catch designers by surprise when they set current limits too aggressively close to their maximum current. Be sure to account for component variation and parametric variations of current-limit setting pins over temperature and make the worst-case calculations.

Figure 7. Illustration of $C_{dv/dt}$-induced current path

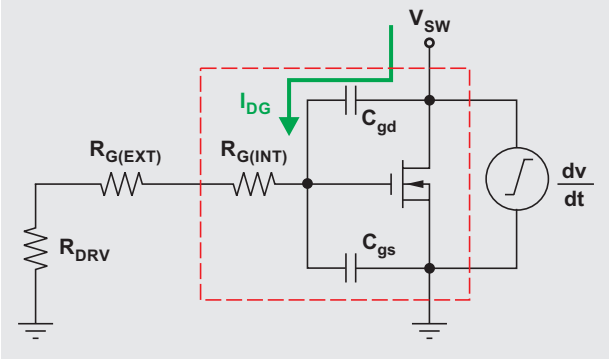
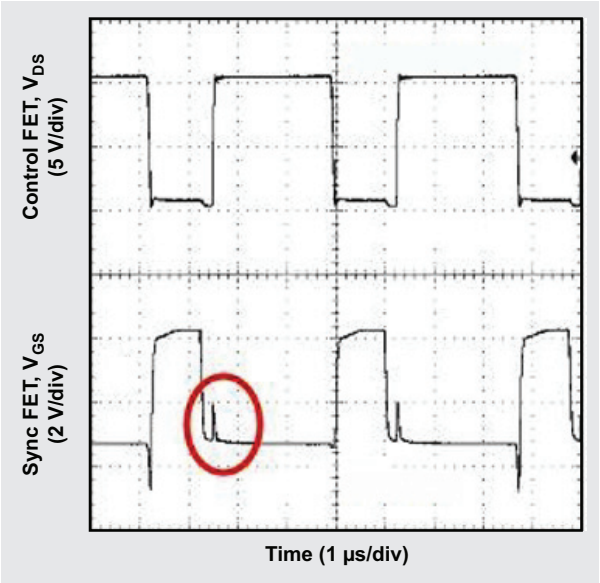


Figure 8. Waveforms showing effect of I_{DG}



Conclusion

Designing with controllers is relatively easy if datasheet guidelines are followed, but it is helpful to be aware of the common mistakes presented in this article. A designer with this awareness can adapt and modify their controller designs with greater confidence and get products to market quicker.

Related Web sites

Product information:
LM27403
LM3495
CSD86360Q5D

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