Understanding the thermal-resistance specification of DC/DC converters with integrated power MOSFETs

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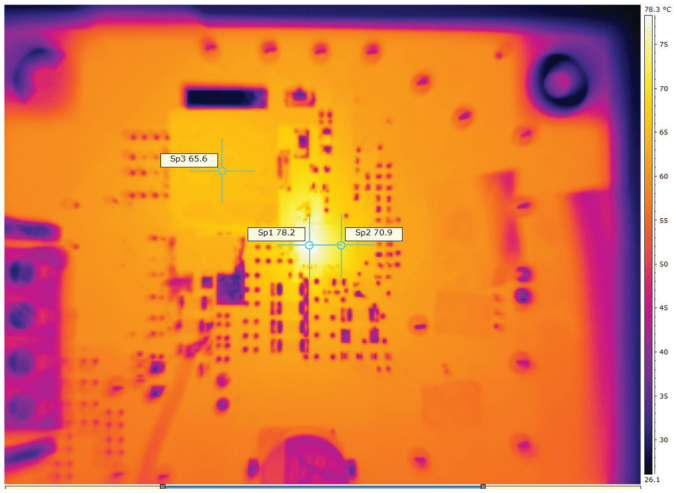
Introduction

Since operating temperature contributes to the performance and reliable life span of semiconductor devices, conducting thermal analysis on power devices is an important part of the power-management design process.

Understanding thermal information from a DC/DC converter data sheet is a critical component of thermal analysis. The data sheets for most modern power devices provide thermal-resistance tables and thermal images (Figure 1) to help designers with their thermal analysis. However, understanding the information in the data sheet is not always direct or easy.

This article presents assumptions that analog designers may make for thermal analysis. The analysis for each assumption is followed with insights to decipher the actual thermal information in the data sheet. The device used for analysis is a high-current DC/DC converter capable of delivering 20 A to 30 A of output current at a low output voltage from a 12-V input.

Figure 1. TPS543C20 40-A thermal image at 0.9-V output with 12-V input, at 25°C ambient



Typical power architecture for point-of-load consumer applications

The thermal information section of a data sheet typically appears before the electrical characterization section. Table 1 shows the thermal information table from the data sheet of the TPS543C20 in the 5- by 7-mm, quad-flat, no-lead (QFN) package.[1] For more information about the thermal metrics shown, please read the application report, "Semiconductor and IC Package Thermal Metrics."[2]

Table 1. TPS543C20 thermal information

Thermal metric	TPS543C20	Unit
$R_{\theta JA}$ Junction-to-ambient thermal resistance	28.9	°C/W
$R_{\theta JC(top)}$ Junction-to-case (top) thermal resistance	18.9	°C/W
$R_{\theta JB}$ Junction-to-board thermal resistance	4.1	°C/W
ψ_{JT} Junction-to-top characterization parameter	1.3	°C/W
ψ_{JB} Junction-to-board characterization parameter	4.1	°C/W
$R_{\theta JC(bot)}$ Junction-to-case (bottom) thermal resistance	1.0	°C/W

Analog designers may look at Table 1 and see the junction-to-ambient thermal resistance is 28.9° Celsius per watt (°C/W). For example, when the maximum ambient temperature inside the system is 65° and the maximum recommended operating temperature is 125°, the estimated allowable power dissipation of the DC/DC converter is 2.07 W (125 – 65/28.9) according to the $R_{\theta JA}$ specification rating.

For this simple analysis to be correct, assume that the system uses a Joint Electron Device Engineering Council (JEDEC)-standard, high-K board. Essentially, a high-K board is a 1.6-mm thick, four-layer board with 2-ounce copper on the top and bottom layers, 1-ounce copper for the internal planes, and a copper area of 74.2 mm by 74.2 mm. The package device pins are connected to the top layer and routed with 0.25-mm wide traces, 25 mm to the perimeter, and equally spaced no more than 2.54 mm apart. But questions remain as to what the rest of the thermal specification numbers in Table 1 mean and how they pertain to a high-K board.

Components of thermal resistance

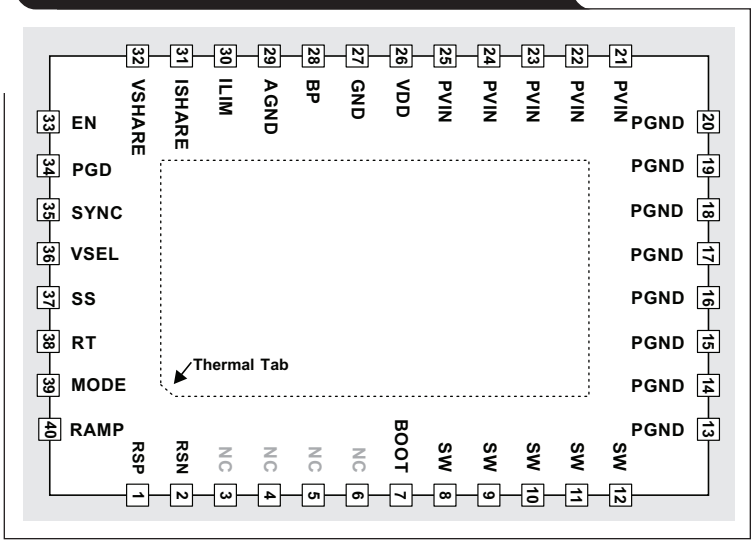
The junction-to-ambient thermal resistance, $R_{\theta JA}$, is the most commonly reported thermal metric and the most often misused. Note the difference between the first value in Table 1, junction-to-ambient thermal resistance, and the last value, junction-to-case (bottom) thermal resistance. Of the 28.9°C/W thermal resistance, only 1°C/W is inside the package. Therefore, only about 3% of the total thermal resistance is moving the heat from the power metal-oxide semiconductor field-effect transistors (MOSFETs) into the ground pad of the circuit board and to the surface of the

integrated circuit (IC). The remaining 97%, or 27.9°C/W, is moving the heat from the IC through the circuit board, thus spreading the heat through the ground plane and surface traces and into the ambient area.

The 27.9°C/W thermal resistance is made up of several parts. The first part—over which designers have very little control—is the thermal resistance from the circuit board into the surrounding air. Without forced airflow, each square millimeter of solder-masked FR4 has a thermal resistance to air of about 65,000°C/W, or about 12°C/W for the 74.2-by 74.2-mm JEDEC board. Although larger boards will offer improved performance, other heat sources in close proximity will begin to contribute to the total power dissipated by the circuit board local area.

Lateral heat flow through the circuit board's copper will reduce the heat dissipated beyond 35 mm from the IC. This second part of thermal resistance, which is the majority of the remaining 15.9°C/W, comes from this lateral heat flow, and is where designers can make the most thermal improvements.

Figure 2. TPS543C20 stacked-clip QFN pin configuration and functions



Reconsidering JEDEC board design

The internal ground plane of the high-K board is only a single layer of 1-ounce copper, which is the primary conduction path for heat drawn from the thermal pad under the DC/DC converter. A second 1-ounce copper ground plane can easily reduce the lateral thermal resistance by half, while additional ground layers will continue to reduce the lateral resistance.

The surface layers that connect to the converter's pins of the JEDEC board are not copper pours but 0.25-mm-wide traces, even when adjacent package pins are intended for connection to a common copper pour. The traces are fanned out from a 0.3-mm-wide space at the IC to 2.54 mm apart at the perimeter of the board. Compared to a copper pour, this fanned pattern has two to four times as much lateral thermal resistance as a solid copper pour.

In power devices such as TI's PowerStack™ clip-QFN package of the TPS543C20 in Figure 2, the PVIN, GND and SW pins are connected to the power MOSFETs through wide, thick copper clips. Copper pours at these pins can significantly improve the lateral heat flow from the FETs across the circuit board and eventually into the ambient air.

Using 2-ounce copper for the top layer with copper pours at PVIN, GND and SW, and at least two 1-ounce copper ground planes connected to the package thermal pad reduces the 15.9°C/W thermal spreading resistance by 50 to 70%, thus reducing the practical $R_{\theta JA}$ from the JEDEC reference value of 28.9°C/W to 20°C/W.

ψ_{JT} and top-side thermal measurements

It is interesting to note the low value of ψ_{JT} despite the high value of the actual thermal resistance to the top of the case, and how it's now possible to measure the die temperature effectively through the top of the package. ψ_{JT} is very low because almost no heat is actually flowing from the top of the case into the ambient area.

Remember that the thermal resistance of the circuit board is 65,000°C/W for 1 mm^2 of circuit-board area. The top side of the package has about the same thermal resistance rating, but it's size is much smaller. The 30-mm^2 package area has a thermal resistance of about 2,000°C/W, or about 1,000°C/W with forced air cooling, so very little heat will flow through the top of the package. This high top-side case-to-ambient thermal resistance enables the top-side package temperature to serve as a very good proxy for the die temperature.

Top-side cooling assumptions

A common question that arises is top-side cooling. While some benefit can be had through top-side cooling, the small thermal surface area of the converter severely limits its effectiveness.

With heat generated over an area of approximately 10 mm^2 on one side of the package, a 0.1-mm-thick layer of thermal grease introduces 5 to 10°C/W of thermal resistance. A 0.2-mm-thick "super-thermal" gap filler introduces approximately 20°C/W of thermal resistance, and conventional gap fillers add 4- to 10-times higher resistance. Compared to the 20°C/W thermal path through the circuit board, very little heat can be drawn through the package unless a thin layer of thermal grease conducts the heat directly to a heat sink.

Packaging difference assumptions

Another common question that arises is if the same techniques that reduce the $R_{\theta JA}$ of the PowerStack clip-QFN package are applicable to other packages to similarly reduce their thermal resistance. The answer is that these

techniques can be tried, but their effectiveness depends on how the JEDEC-standard board limits the junction-to-ambient thermal path of these other packages.

Not all packages can improve their circuit board's thermal spreading resistance as effectively in a practical design as much as the PowerStack clip-QFN package. Consider whether the JEDEC board moves most of the heat generated by the DC/DC converter through the top layer traces or through the ground plane. Also, consider whether the DC/DC converter package allows connection of the pins to the wide planes, or if the pins are limited to the narrow traces of the converter.

Conclusion

Many thermal metrics exist for semiconductor and IC packages, which range from $R_{\theta JA}$ to ψ_{JT}. Often, designers misapply these thermal metrics when trying to estimate the junction temperatures in their systems. Ultimately, thermal performance depends on the circuit-board layout and using standard JEDEC-referenced thermal numbers.

References

1. "TPS543C20 4-VIN to 16VIN, 40-A Stackable Synchronous Step-Down SWIFT™ Converter with Adaptive Internal Compensation." Texas Instruments data sheet (SLUSCD4A), September 2017.
2. Darvin Edwards and Hiep Nguyen, "Semiconductor and IC Package Thermal Metrics," Texas Instruments Application Report (SPRA953C), April 2016.

Related Web sites

Product information:
TPS543C20

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