Achieving a clean startup by using a DC/DC converter with a precise enable-pin threshold

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Introduction

In many applications, the various DC/DC converters in a given system need to start up at a specific supply voltage. For example, industrial applications that draw power either from a 4–20-mA current loop or from energy harvesting must have sufficient energy stored in the input capacitance before the DC/DC converter turns on. In the absence of sufficient energy, the in-rush current that the converter draws during startup may pull the input voltage down too low and cause the system or converter to reset. In a worst-case scenario, the system never starts at all.

Most DC/DC converters contain an enable (EN) pin input that is used to overcome this startup behavior. This article explains some common EN-pin threshold specifications found in device data sheets and describes several application circuits that provide a clean startup, with or without using a converter with a precise EN-pin threshold.

Enable pin specifications

Fundamentally, an EN pin is a digital input that turns a DC/DC converter on or off. When the EN pin's voltage is above a logic threshold, most often called $V_{\rm IH}$, the converter detects a logic high at the pin and turns on. When the EN pin's voltage is below a logic threshold, most often called $V_{\rm IL}$, the converter detects a logic low at the

pin and turns off. An EN pin has either a "loose" threshold voltage or a "precise" threshold voltage, each of which has different application considerations. Table 1 shows an example of a loose threshold voltage from the TPS62130A data sheet. Table 2 shows an example of a precise threshold voltage from the TPS62136 data sheet.

The typical EN-pin threshold-voltage values in Tables 1 and 2 show how much hysteresis is present on the EN-pin input. Hysteresis is important in order to avoid on/off oscillations that may occur with a very slow ramp rate on the EN signal.

Table 3, from the TPS62740 data sheet, shows another way to write a loose EN-pin threshold voltage. While the values shown are in opposite columns, compared to Table 1, the meaning is the same: the EN pin must be driven above 1.1 V to ensure that the converter reads a logic-high level and driven below 0.4 V to ensure that the converter reads a logic-low level. The integrated circuit (IC) might read any voltage between V_{IH} and V_{IL} as either a logic high or logic low. Since this area between the high and low levels is very large, this is a loose EN-pin threshold-voltage specification. Table 1 describes what voltage the application must apply, whereas Table 3 describes the actual voltage-threshold level inside the IC.

Table 1. The TPS62130A has a loose EN-pin threshold voltage

	PARAMETER	TEST CONDITIONS	MIN	ТҮР	MAX	UNIT	
CONTROL (EN, DEF, FSW, SS/TR, PG)							
V _H	High level input threshold voltage (EN, DEF, FSW)		0.9	0.65		V	
VL	Low level input threshold voltage (EN, DEF, FSW)			0.45	0.3	V	

Table 2. The TPS62136 has a precise EN-pin threshold voltage

	PARAMETER	TEST CONDITIONS	MIN	ТҮР	MAX	UNIT	
CONTROL (EN, SS/TR, PG, MODE, VSEL)							
V _{IH}	Input threshold voltage for EN pin; rising edge		0.77	0.8	0.83	V	
V _{IL}	Input threshold voltage for EN pin; falling edge		0.67	0.7	0.73	V	

Table 3. The TPS62740 has a loose EN-pin threshold voltage

	PARAMETER	TEST CONDITIONS	MIN	ТҮР	MAX	UNIT	
INPUTS EN, CTRL, VSEL 1-4							
V _{IH_TH}	High level input threshold	$2.2V \le V_{IN} \le 5.5V$			1.1	V	
$V_{\text{IL}_{\text{TH}}}$	Low level input threshold	$2.2V \le V_{IN} \le 5.5V$	0.4			V	

Using the EN pin to achieve a clean startup

Proper use of the EN pin solves many common startup behaviors that are problematic for different types of systems:

- Systems powered from current-limited sources may get stuck in their startup state.
- Systems with a slowly rising input voltage may be sensitive to an output-voltage rise time that's too slow.
- Other systems may not be tolerant of wide variations in startup timing, which arise from a loose-control EN pin combined with a resistor-capacitor (RC) delay circuit.

Converter startup analysis for three scenarios

1. Converter stuck in its startup

A common outcome for current-limited systems, such as 4-20-mA current loops and energy harvesting, is for the converter to get stuck in startup and then hiccup as it tries to bring the output voltage from 0 V into regulation. This occurs because the converter draws a relatively high in-rush current during startup, which is almost always greater than the output power of current-limited systems. This in-rush current causes the input voltage to drop suddenly, which trips the undervoltage lockout (UVLO) of the converter, causing it to turn off. With the in-rush current gone, the input voltage rises back up, and the converter restarts. Now, the converter draws in-rush current again and the system shuts back down.

Figure 1 shows an example of hiccup operation using the TPS62125 powered through a current-limited input supply and not using its EN pin. The output voltage never reaches its 3.3-V set point.

A simple solution to this challenge is to use a converter with a precise EN-pin threshold voltage. When using the TPS62125's EN pin, the input voltage rises up to the programmed $V_{\rm IH}$ level, which is well above the converter's UVLO level.^[1] This stores enough energy in the input capacitance to supply the in-rush current.

Figure 2 shows that although the input voltage still drops, the drop does not trip the UVLO circuit, which enables the DC/DC to keep operating and start up properly.

A precise EN-pin threshold voltage is also useful for simple maximum-power-point tracking (MPPT). In this

Figure 1. A current-limited system can get stuck in hiccup during startup



Figure 2. A current-limited system requires a precise EN-pin threshold voltage for proper startup



application, the input voltage is allowed to hiccup around the maximum power point (MPP) in order to operate an energy harvester, such as a solar panel, at its peak output power. Reference 2 details an example with the TPS62125.

2. Output voltage rising too slowly

For systems with a slowly rising input voltage, the output voltage may also rise too slowly and violate the ramp-time requirement of the load, such as a microcontroller (MCU). The output voltage rises too slowly when set above the converter's UVLO level and the input voltage slew rate is slower than the programmed soft-start time. In this case, a slow input-voltage ramp enables the converter properly, but instead of ramping up within the set soft-start time, the output voltage ramps up with the input voltage's rise time.

Figure 3 shows that the converter, a TPS62136 set to a 3.3-V output, enters 100% mode (circled in red) during startup and has a very long total startup time. Entering 100% mode during startup indicates that the converter is trying to create a faster output voltage ramp but cannot, because the input voltage is insufficient.

The output voltage ramp is faster when using the EN pin to enable the converter once the input voltage reaches a higher voltage. Figure 3 also shows the resulting different output voltage ramp times when given the same input voltage ramp.

3. Variations in startup timing

Multi-rail systems frequently require sequencing the startups of various DC/DC converters. Sequencing allows the input voltage or another system rail to be fully up at its nominal voltage before the startup of the next converter. Separating the startups like this reduces the total in-rush current that the system demands. Specific loads, such as processors and field-programmable gate arrays (FPGAs), typically require sequencing of their numerous supply voltages.

While connecting the power good (PG) output of the first converter to the EN input

of the next converter is the simplest method to achieve sequencing, it may not always be possible for a variety of reasons. The first converter may not have a PG output. Or the pull-up voltage of the PG signal may not be high enough for the second converter's EN pin. Finally, using the PG output of the previous converter is impossible for the first converter in the startup sequence. In all of these cases, using an RC delay circuit is frequently used to delay the startup of converters and provide very basic sequencing.

An RC delay slows the voltage applied to the EN pin, relative to the input voltage or another system rail. However, because of the tolerances of the resistor and



Figure 3. A precise EN-pin threshold voltage allows a proper

Figure 4. An RC delay circuit delays the startup of a converter relative to the input voltage, but is not precise



capacitor, as well as the EN-pin threshold voltage, this delay time is not precise and varies widely. Figure 4 shows the startup of the TPS62130A with an RC delay circuit, where the converter starts at its typical 0.65-V, EN-pin threshold voltage. The horizontal cursors show the 0.3-V and 0.9-V logic levels, $V_{\rm IL}$ and $V_{\rm IH}$. The vertical cursors at these points show the possible variation in startup delay time from the loose threshold voltage. The time between these cursors does not include any variation from the resistor and capacitor, which would affect the slope of the EN signal and create an even wider startup-delay time variation.

The TPS62136 is newer than the TPS62130A shown in Figure 4. The TPS62136 provides the same basic input voltage range and output current, but with improved performance, such as a smaller solution size, a higher output current, a more accurate output voltage and a precise EN-pin threshold. The precise EN-pin threshold voltage removes much of the variation inherent in RC delay circuits, greatly improving their startup timing accuracy.

Using a simple resistive voltage divider from the input voltage to the EN pin is not a robust solution for achieving startup delays for devices with a loose EN-pin threshold voltage. When properly setting the divider ratio to ensure that the device always starts—based on the input voltage's lowest tolerance and highest $V_{\rm IH}$ level—the divider gives very little delay when an EN-pin threshold voltage occurs near the $V_{\rm IL}$ level.

Using an SVS to achieve a clean startup

A supply voltage supervisor (SVS) is a discrete IC that monitors a voltage relative to a precise programmed threshold. SVSs monitor critical system voltages and assert a fault if the voltage exceeds certain limits; they also provide proper startups and shutdowns of some subsystems. In addition to the precise threshold voltage, some SVSs incorporate fixed or programmable startup delay times. A discrete SVS such as the TPS3890 is useful when an application requires a specific converter and a precise startup level, but this particular converter does not have a precise EN-pin threshold voltage. A discrete SVS is used in the same way as a precise EN-pin threshold in the three examples shown in this article.

Conclusion

Various applications, such as those powered from a current-limited source or sources with a slow ramp time, require special startup considerations. Often, the DC/DC converter must start up at a certain level to achieve proper system operation.

To determine the best way to alleviate a startup concern, it is important to understand the type of EN-pin threshold voltage specification—precise or loose—for a specific converter. A converter with a precise EN-pin threshold voltage, or a discrete SVS, overcomes many startup issues in industrial systems.

References

- 1. Chris Glaser, "Harnessing wasted energy in 4- to 20-mA current-loop systems," Texas Instruments Analog Applications Journal (SLYT488), 4Q 2012.
- 2. Chris Glaser, "Easy solar-panel maximum-power-point tracking for pulsed-load applications," Texas Instruments Analog Applications Journal (SLYT478), 3Q 2012.

Related Web sites

Product information: TPS62130A TPS62136 TPS62125 TPS62740 TPS3890

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