Control challenges in a totem-pole PFC

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Introduction

Power-conversion system efficiency is becoming ever more important due to economic reasons and environmental concerns. The efficiency levels defined in the 80 PLUS® standard require up to 96% for Titanium. It becomes a design challenge for power-supply companies with traditional topologies when such high efficiency is required.

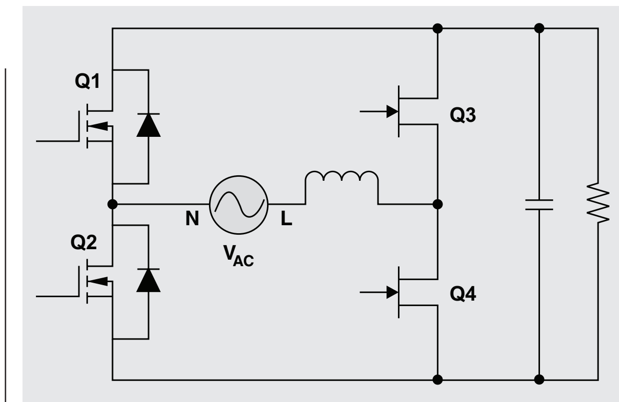
For a power supply with 75 W or greater, the design usually consists of power-factor correction (PFC) circuitry and a DC/DC converter. PFC forces the input current to follow the input voltage so that any electrical load appears like a resistor. Among the different PFC topologies, totem-pole PFC is attracting more attention because it can offer the highest efficiency.

A basic totem-pole PFC structure is shown in Figure 1. Note that Q3, Q4 and the inductor consist of a boost converter. Based on V_{AC} polarity, Q3 and Q4 alternately work as a PFC main switch or sync switch. During a positive V_{AC} cycle, Q4 is the main switch, while Q3 works as a sync FET. The driving signals for Q3 and Q4 are complementary: Q4 is controlled by the duty cycle (D) from the control loop, while Q3 is controlled by 1 – D.

During a negative V_{AC} cycle, the function of Q4 and Q3 is swapped where Q3 becomes the main switch, and Q4 works as a sync FET. The driving signals for Q3 and Q4 are still complementary, but Q3 is now controlled by D while Q4 is controlled by 1 – D. Because of the reverse-recovery issue, a regular MOSFET cannot be used in a continuous-conduction mode (CCM) totem-pole PFC, therefore Q3 and Q4 need to be gallium nitride (GaN) FETs, which have no reverse recovery. Q1 and Q2 diodes are paralleled with regular MOSFETs to further improve efficiency.

There are no commercial analog controllers available for a totem pole PFC at this time. A digital controller, because of its flexible nature and integrated digital power peripherals, is a good candidate for this topology. Even though the traditional control method cannot be directly applied to a totem-pole PFC, special control algorithms need to be developed. In fact, the control of a totem-pole PFC is much more complex when compared to a traditional PFC. Lacking a bridge rectifier, the bidirectional inductor current and the function swap between the main switch and the sync switch creates many challenges in a totem-pole PFC design.

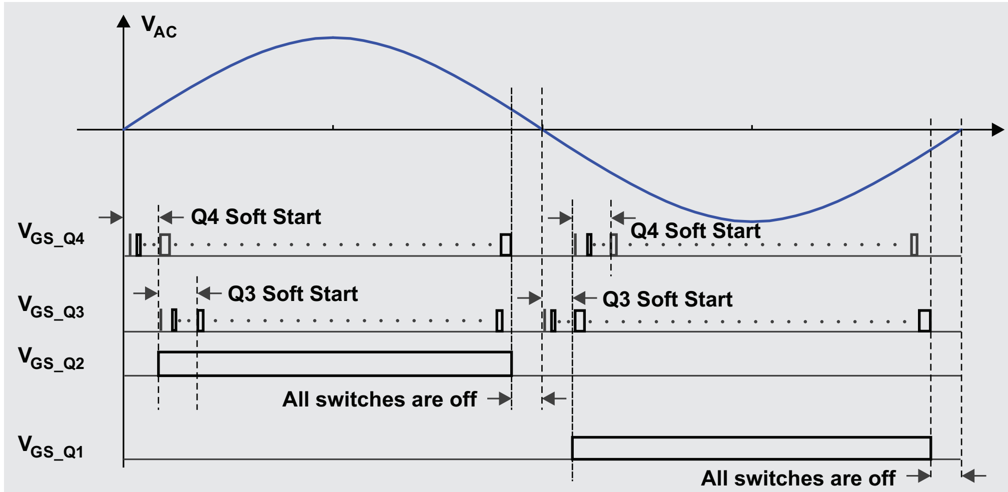
Figure 1. A totem-pole PFC structure



Current spike at AC zero-crossing

One challenge with a CCM totem-pole PFC is that the input current has big spikes at AC zero-crossing. The issue is inherent with totem-pole PFC topology and is very complicated. Circuit characteristics that can generate these spikes include the turn-on sequence of the switches, slow reverse recovery of Q1 and Q2 body diodes, large C_{OSS} of Q1 and Q2, sudden swaps of the PWM signal between Q3 and Q4, and so on. By turning the switches on with a special sequence and executing a soft-start mechanism on both the main and sync FETs (Figure 2),[1] current spikes can be reduced significantly. Thus, total harmonic distortion (THD) is significantly improved as a result.

Figure 2. PWM signal timing after AC zero-crossing



How to reliably detect AC zero-crossing

As mentioned earlier, the function of Q3 and Q4 depends on V_{AC} polarity. Q3 and Q4 alternate operation as the main switch and the sync switch right after AC zero-crossing. The duty ratio of one switch changes abruptly from almost 100% to zero, while the duty ratio of the other switch changes abruptly from zero to almost 100%.

An error in V_{AC} zero-crossing detection, typically caused by noise or a voltage spike, would be problematic. For example, during a positive V_{AC} cycle, if noise makes the controller react as if the AC changed to a negative cycle, the controller will apply almost 100% duty to Q3. Since Q2 is still on in this scenario, the output bus is shorted to ground, thus causing a huge current spike that may damage the hardware. A reliable way to detect the correct AC zero-crossing is as follows:

1. For safety reason, whenever the controller detects changes in AC polarity, it shuts down all switches.
2. If the controller detects a V_{AC} polarity change for a consecutive number of times (for example three), it is safe to assume that the V_{AC} polarity change is true. As a result, the controller will execute a special soft-start sequence as described in Reference 1.

These operation precautions can essentially eliminate an error in V_{AC} zero-crossing detection typically caused by noise or voltage spikes.

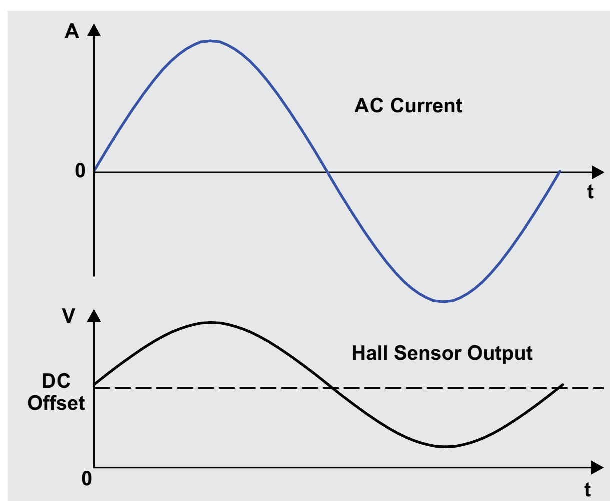
Turn sync switch off during soft start

Before a PFC start up, both the voltage loop and current loop are off and their outputs are zero. Once the PFC starts up, these control loops start a "build-up" process. The integrators in these loops start to accumulate until the required control effort (duty cycle) is met. Therefore, at the beginning of soft start, the duty cycle (D) is small, while 1 – D is big. If the sync switch turns on with 1 – D at this moment, the output voltage is discharged, which produces a reverse-current spike. To eliminate this issue, the sync switch should remain off until the PFC soft start is over and PFC enters steady state.

Current reference and control-loop polarity

The inductor current in a totem-pole PFC is bidirectional. The current sensor should be able to sense this bidirectional current and trigger the control loop accordingly. A Hall-effect sensor is a good candidate for this application. The Hall-effect sensor output is usually a sinusoidal waveform with a DC offset as shown in Figure 3. This is different from a traditional PFC where the current feedback signal is a rectified sine wave with no DC offset. As such, the traditional PFC current reference cannot be used in a totem-pole PFC. For proper current-loop control, the current reference in the totem-pole PFC is modulated to accommodate this special waveform.

Figure 3. Hall sensor output for sensing bidirectional AC current



The current reference in a totem-pole PFC can be derived by first calculating the sinusoidal current reference to be the same as in a traditional PFC. Then at the positive V_{AC} cycle, calculate the control loop current reference as shown in Equation 1.

$$\text{Current Reference} = \text{Sinusoidal Reference} + \text{DC Offset} \quad (1)$$

The control loop provides negative feedback and is the same as in a traditional PFC (Equation 2).

$$\text{Error} = \text{Current Reference} - \text{Feedback} \quad (2)$$

During a negative V_{AC} cycle, the control-loop current reference is defined by Equation 3.

$$\text{Current Reference} = \text{DC Offset} - \text{Sinusoidal Reference} \quad (3)$$

Moreover, because the feedback signal is inversely proportional to the real current signal in a negative V_{AC} cycle, the control-loop feedback polarity must change from negative to positive.

$$\text{Error} = \text{Feedback} - \text{Current Reference} \quad (4)$$

V_{AC}-drop issue

When V_{AC} drops, it takes time for the controller to detect this drop. Because the switches are still on before the controller detects an AC drop, the DC bus voltage is discharged through the sync switch, which can cause two problems. The first problem is that the power stored in the output capacitor is discharged and the hold-up time can no longer be guaranteed. The second problem is a big reverse current.

The worst-case scenario occurs when V_{AC} drops at its peak, where the sync switch has the widest duty. An extra circuit needs to be added to fast-detect AC drop, then either notify the controller or directly shuts down the switches. There is a simple and zero-cost solution to this problem. Note that the reverse-current spike caused by the AC drop is always in the opposite polarity of the V_{AC} waveform. This is a negative current spike at the positive V_{AC} cycle, and a positive current spike at the negative V_{AC} cycle. To solve the V_{AC} drop issue, the controller is configured to detect the positive current spike at negative AC cycle, and detect a negative spike at a positive cycle. Once such a spike is detected, the controller knows that the AC has dropped and shuts down all the switches, which prevents the output capacitor from discharging.

Now, if V_{AC} drops for a few cycles then comes back, it causes another issue. In a traditional PFC, when the controller detects that V_{AC} comes back, the controller can immediately turn on the PFC main switch. The instantaneous turn on can occur anywhere in the V_{AC} waveform. In a totem-pole PFC with a sync switch, timing of the turn on becomes important. Assuming that V_{AC} comes back at its peak, the D is small and 1 – D is big. Turning on the PFC sync switch at this point will cause a big reverse-current spike. A practical solution to compensate for when AC comes back is to:

1. Always turn on main switch first;
2. Always turn on PFC at AC zero-crossing and execute a special soft-start sequence as described in Reference 1.

Conclusion

With modern digital controllers and the advent of GaN FETs, the limitations for designing a CCM totem-pole PFC are minimized. However, controlling a CCM totem-pole PFC poses many challenges which do not exist in a traditional PFC. This article illustrated these challenges and provided practical solutions for each of them. These solutions were validated in a 1-kW totem-pole PFC controlled by the UCD3138. The test results showed that the solution achieves 99% efficiency with excellent THD and power factor (PF).[2]

References

1. B. Sun, “How to reduce current spikes at AC zero-crossing for totem-pole PFC,” Texas Instruments Analog Applications Journal (SLYT650), 4Q 2015.
2. Z. Ye, A. Agular, Y. Bolurian and B. Daugherty, “GaN FET-Based CCM Totem-Pole Bridgeless PFC,” TI Power Supply Design Seminar (SLUP327), 2014.

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