How unmatched impedance at the clock input of an RF ADC affects SNR and jitter

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Introduction

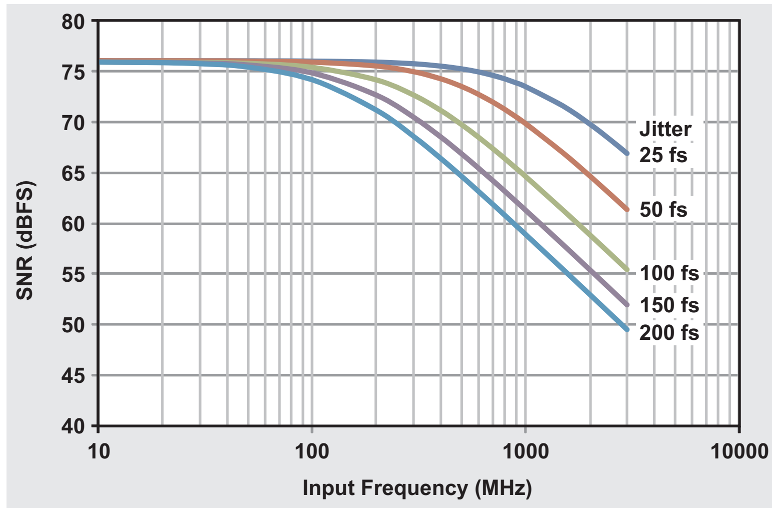
Modern high-speed data acquisition systems, such as phased-array radars or high-speed digitizers, continue to push higher both the bandwidth and input-frequency requirements without any sacrifice of dynamic range performance. System designers need to deliver the highest possible signal-to-noise ratio (SNR) in order to optimize system performance down to a tenth of a decibel.

However, it is well known that as input frequencies increase, the analog-to-digital converter (ADC) SNR becomes increasingly sensitive to the sampling-clock's timing uncertainty—or jitter. This applies to slower speed but high-precision ADCs with 16-bit resolution or more, and very high SNR. This situation also applies to high-speed 12- and 14-bit ADCs that have a wide bandwidth front-end to sample signals at multiple gigahertz. The SNR degradation follows a well known formula of:

$$SNR = 20\log(2\pi \times f_{IN} \times t_{Jitter}),$$

where t_{Jitter} is the combination of both external and internal aperture jitter. Figure 1 shows SNR dependency on the input frequency and the total amount of clock jitter for an ADC with 76-dB thermal noise

Figure 1. ADC SNR versus jitter

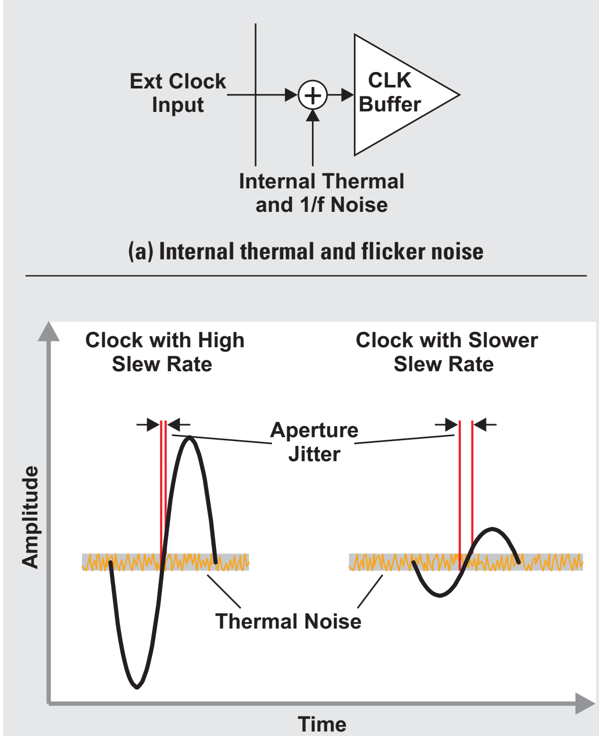


What is aperture jitter?

In simple terms, the ADC clock input has both thermal and flicker noise components that get added to the clock signal, as in Figure 2a. The smaller the clock slew rate, the more dominant the noise factors when latching the clock signal. Therefore, the faster the rising edge of the clock signal, the less frequency error is present during the sampling instant at the zero crossing (Figure 2b). When using a sine-wave clock signal, the slew rate and amplitude are directly related to each other.

Designing for optimum ADC-aperture jitter for modern RF-sampling converters operating at 2+ GSPS can consequently become challenging. The system designer has to ensure delivery of a large-amplitude clock signal to the ADC while addressing RF issues. Examples of these issues include excessive board attenuation (the higher the frequency the higher the attenuation), higher voltage standing-wave ratio (VSWR), and lack of impedance matching.

Figure 2. ADC clock-input noise sources



(a) Internal thermal and flicker noise

(b) Slew rate comparison

While there are a few ways to improve and optimize external jitter, such as using a low-jitter clock source or an external bandpass filter, the ADC aperture jitter depends primarily on the clock amplitude. See the example in Figure 3.

Impact of reduced clock amplitude

When examining the frequency spectrum of a sampled sine wave in a fast Fourier transform (FFT), the impact of the clock amplitude to the ADC aperture jitter becomes clearly visible as shown in Figure 4. For Figure 4, the ADC sampling rate was 2.949 GSPS with an input signal of 1.81 GHz at –2 dBFS, and clock amplitudes of 500 mV_{PP} and 1 V_{PP}. The full Nyquist-zone fast-Fourier transform (FFT) (Figure 4a) shows a uniform increase of the overall noise floor. When normalizing the FFT to the sine-wave frequency (Figure 4b), note that there is an increase in the 1/f noise component of the ADC aperture jitter. This needs to be taken into consideration when designing systems with certain noise power targets at specific offset frequencies, such as global system for mobile communication (GSM) or long-term evolution (LTE) base stations or radar receivers.

Is impedance matching required on the clock input?

Input impedance matching can be a simple but very effective way to significantly boost the clock amplitude and improve the ADC aperture jitter. An RF-sampling ADC typically has integrated termination resistors. Otherwise, in order to minimize reflection, the termination resistor should be placed as close to the end of the transmission line as possible. At higher clock frequencies, increased degradation can

Figure 3. Aperture dependency on clock amplitude from ADC32RF45 data sheet

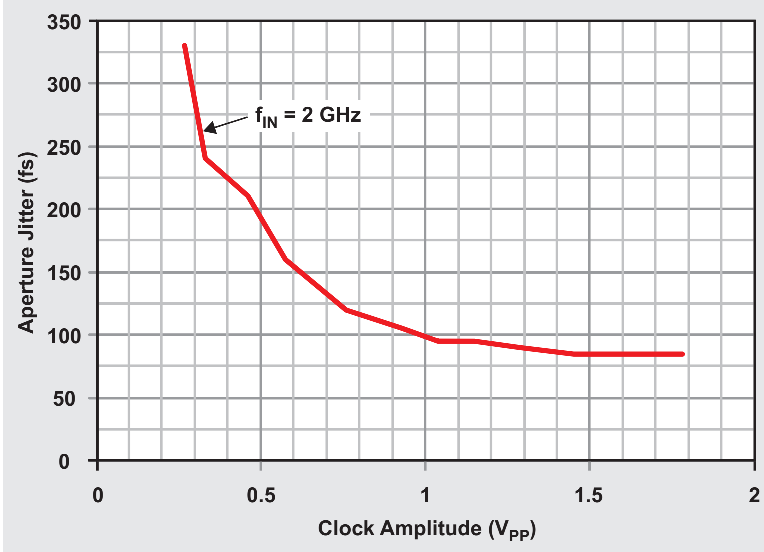
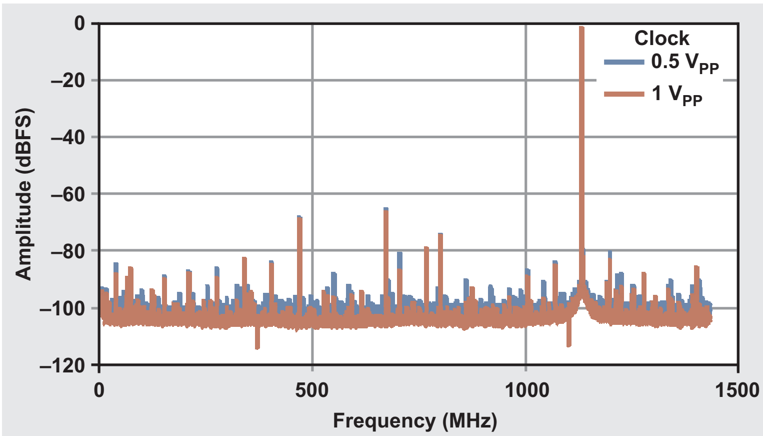
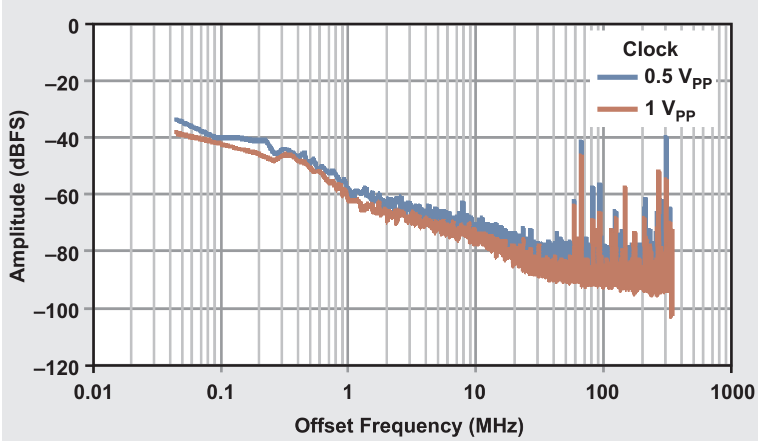


Figure 4. Fast-Fourier transform (FFT) of an ADC



(a) A full Nyquist FFT



(b) FFT normalized to the input frequency

Figure 5. Smith chart of the clock input impedance versus frequency of the ADC

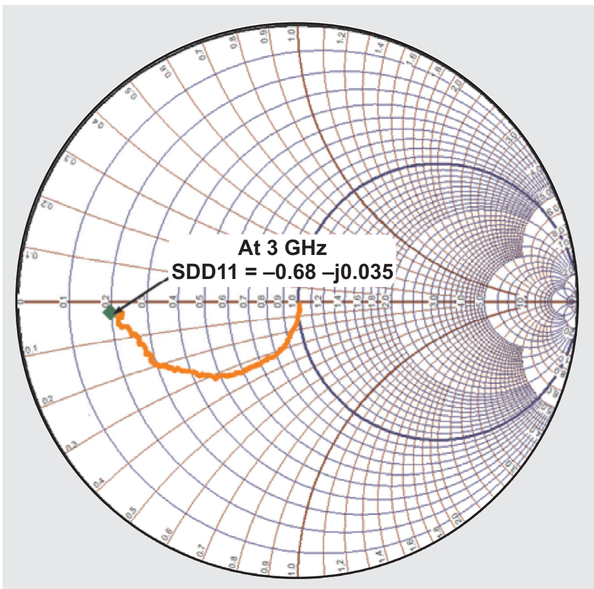
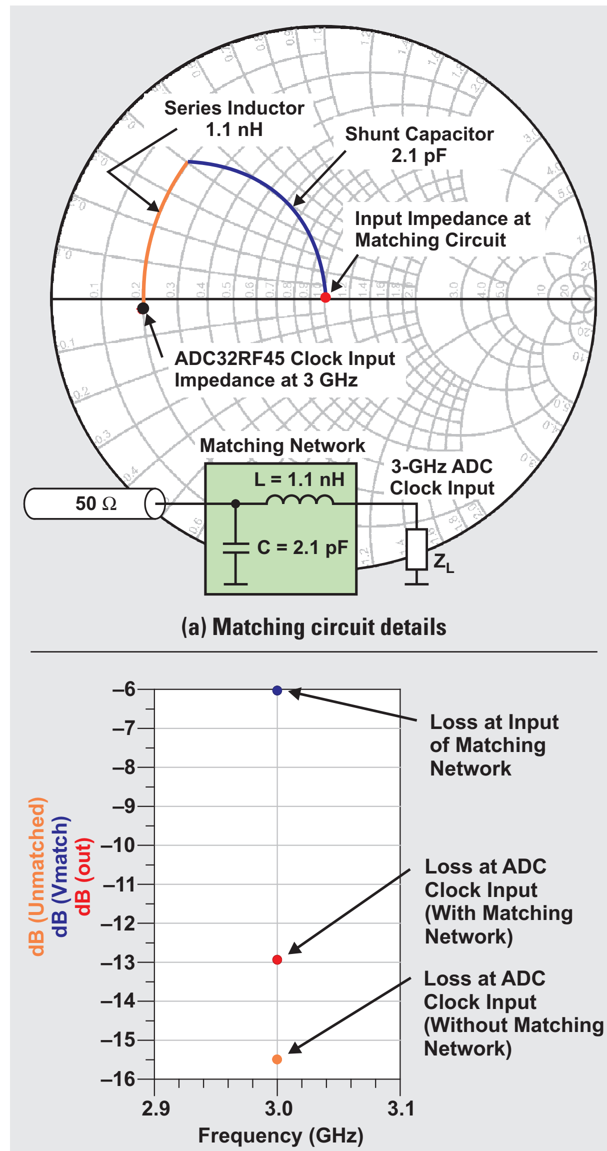


Figure 6. Clock-input loss simulation with and without matching network



(a) Matching circuit details

(b) Loss simulation comparison

be attributed to the board and internal layout in addition to increased routing parasitics of the termination impedance. This is reflected in the Smith chart of the ADC32RF45 clock input in Figure 5.

In this example, with a clock frequency of 3 GHz, the internal differential 100-Ω termination looks more like a complex impedance of about 20 Ω. This reduced load impedance significantly impacts the amplitude in two different aspects:

1. The reduced load impedance makes it much harder for the clock source to deliver sufficient clock amplitude to the clock-input buffer for optimum ADC aperture jitter.
2. The load impedance is significantly different from the source and transmission-line impedance. This mismatch causes unwanted reflections and noise on the ADC's clock input. Due to the impedance mismatch, the resulting voltage divider delivers significantly less amplitude compared to the power match. In a power match, the load and source impedances match, resulting in a 50/50 voltage divider to deliver maximum amplitude to the load.

Fortunately, a simple first-order matching network with two or three passive components can be designed to match the ADC clock-input impedance at the desired sampling rate to the impedance of the transmission line (typically 50 Ω, single-ended).

The external matching circuit for the ADC32RF45 at a frequency of 3 GHz for a power match could consist of a differential ≈1.05-pF shunt capacitor (2.1-pF single-ended), and ≈1.1-nH series inductors at the clock input of the ADC (Figure 6a). This transforms the complex load impedance of about 10 Ω back to 50 Ω (100-Ω differential) for a clock frequency of 3 GHz. There are free online tools available to assist with this exercise.

This power match now delivers maximum amplitude at the new load's input, which consists of a matching circuit plus load impedance. Additionally the matched load presents a larger load impedance to the clock generator, which enables it to provide a larger output amplitude. However, there is still a voltage divider present between the matching circuit and the load impedance. Hence, some amplitude loss will always be present as illustrated in Figure 6b. When compared to a similar setup without a matching circuit, the amplitude delivered to the clock input with a matching circuit improved by 2.5 dB. Note that the clock source also delivers a higher amplitude, driving a 100-Ω load instead of a 20-Ω load.

Conclusions

The amplitude of the sampling clock is a critical parameter since it is directly tied to the ADC aperture jitter. This is made clear when trying to maximize the receiver dynamic range and to achieve the advertised SNR performance of modern RF-sampling converters, such as the ADC32RF45. As the converter clock frequencies increase, the system designer has to counter additional attenuation from the PCB material as well as limited amplitude-drive capabilities from the clocking sources. A simple matching circuit at the clock input can avoid a heavy load for the clocking device while the matched impedances ensure that maximum amplitude is delivered to the load.

References

1. Tommy Neu, "Direct RF conversion: From vision to reality," Texas Instruments White Paper (SLYY068), May 2015.
2. Robert Keller, "Signal chain basics #45: Is high-speed ADC clock jitter being over-specified for communication systems?" Planet Analog, September 2, 2010.
3. Overview of RF sampling with high-speed ADCs.

Related Web sites

Product information:
ADC32RF45

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