JESD204B over optical fiber enables new architecture for phased-array radars

By Matt Guibord
System Engineer, High-Speed Data Converters

Electronically controlling the beam direction of a phased-array antenna has been in use since the mid-twentieth century. However, most antennas still rely on analog methods to steer the beam.[1] The next step for phased-array radar is to achieve full digital control of the beam, often called a "digital phased-array radar." A digital phased array requires every antenna element to have its own data converters. Analog phase-shifting is no longer performed between the antenna and data converters in this architecture. Instead, phase-shifting and beamforming are performed using purely digital functions.

Digital phase shifting and beamforming enables the formation of multiple beams and can allow multiple frequency bands to be used for multi-target tracking or simultaneous missions. Aside from flexibility, there are also performance reasons to move toward digital arrays. For one, the imperfect analog phase shifters and beamforming elements are replaced by precise digital phase-shifting and beamforming for improved sidelobe rejection. Additionally, clutter rejection is improved because of decorrelated analog-to-digital (ADC) and digital-to-analog (DAC) converter noise and distortion at every antenna element.[2]

The biggest roadblocks for building digital arrays are size, power, and processing ability. Each element, including data converters and other analog components, must be small enough to allow elements to sit half a wavelength from each other (Table 1). Such tight spacing raises thermal concerns, creating a requirement for low power consumption. Lastly, the required processing power for digital beamforming is significantly higher than analog beamforming, due in part to digital phase shifting and beamforming, but also due to the significantly higher amount of data from the ADCs.

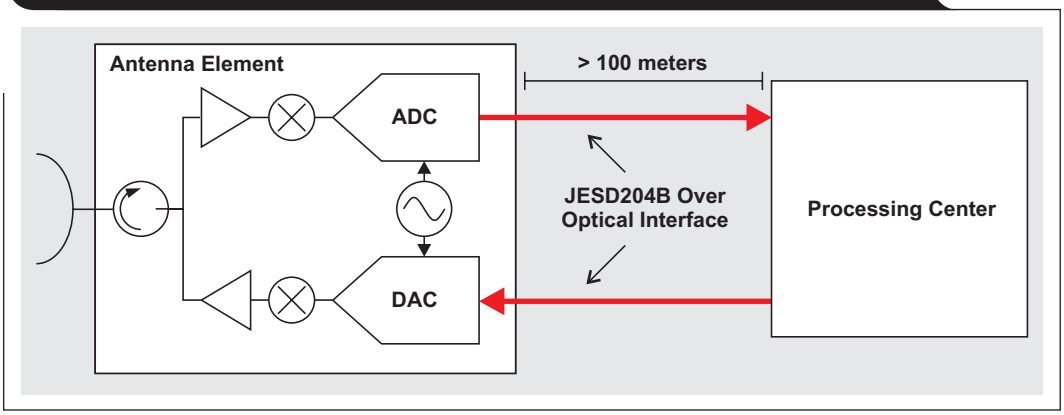
There are a number of potential architectures that could be used in digital phased-array radars. For instance, discrete data converters can be connected to FPGAs, all sitting at the antenna array. However, FPGAs are large, power hungry and noisy, especially with increased processing requirements. So it is undesirable to have one sitting at the array near sensitive analog components. Depending on usage, an FPGA can consume up to tens of watts of power, creating thermal issues and likely requiring bulky heat sinks or other advanced cooling methods. Instead, a preferred architecture moves the FPGA off the array and connects to the data converters directly through optical fiber. This architecture has recently become possible due to the adoption of the JESD204B interface in data converters (Figure 1).

JESD204B is a serialized data-converter interface that can operate at up to 12.5 Gbps over multiple current-mode logic (CML) lanes. The physical interface used is similar to that used by gigabit Ethernet protocols and, thus, lends itself well to use with optical transceivers. Using optical transceivers can extend the reach of the otherwise short-reach interface to greater than 100 meters. It is clear that placing an optical transceiver at the array to connect to the data converters and another at the FPGA can enable digital phased-array radar without the need for an FPGA at the antenna array.

Table 1. Antenna element spacing versus operating band

Radar Operating Band	Maximum Antenna-Element Spacing
L-band	150 mm
S-band	75 mm
C-band	37.5 mm
X-band	18.75 mm

Figure 1. Phased-array antenna element with optical JESD204B interface



A simplistic board placement shown in Figure 2 demonstrates the feasibility of this architecture in digital L-band, S-band, and potentially C-band radars. The RF paths shown are fairly narrow, however, using both the top and bottom of the board enables more room for placement and routing. This example uses commercially available components and is drawn to scale.

A 1-Gsps, 16-bit dual-channel ADC (ADS54J60) enables high performance for signal bandwidths of greater than 250 MHz. Likewise, a 2.5-Gsps, 16-bit dual-channel DAC (DAC38J82) enables similar transmit performance. For data rates of 1 Gsps, each data converter is capable of using two serializer/deserializer (SerDes) lanes per channel at 10 Gbps. The optical transceivers contain twelve channels allowing six ADC channels and six DAC channels to be used per set of transmitter and receiver. Total optical transceiver power at the antenna array is about 380 mW per antenna element, lower than an equivalent architecture with an FPGA directly interfaced to the data converters. Ideally, the optical transceiver size and power would be reduced even further.

The challenge with this architecture is not so much related to the SerDes interface itself as it is to the other signals required for JESD204B. Other than data, there are three main signals required when using the subclass 1 variant of JESD204B: device clock, SYSREF and SYNC.

Device clock is analogous to the data converter sampling clock and has the same low-jitter performance requirement. The skew between device clocks for multiple data converters ultimately determines the phase accuracy of the sampling instant, a key requirement for phased-array radar. However, it is possible that digital techniques can be used to compensate for device clock skew. The only additional concern added by the optical architecture is that both ends of the optical link must be frequency synchronized for the synchronous serialized link to function properly.

SYSREF is a low-frequency timing reference used for all JESD204B devices in order to obtain deterministic latency. For multi-device synchronization, SYSREF must be captured by the same device clock cycle at every data converter, or at least exactly an integer number of SYSREF periods later. This places a setup-and-hold timing requirement on SYSREF relative to the device clock. Additionally, the FPGA must also receive SYSREF at a deterministic time relative to the data converters in order to achieve deterministic latency. Thus, the phase of SYSREF at each end of the optical link must be well controlled.

SYNC does not have any specified timing requirements for subclass 0 or subclass 1 implementations of JESD204B. For most purposes, it is a binary DC signal that is used only during link initialization to align the character clocks within the SerDes transmitter and receiver. The receiver must toggle SYNC low on start up to tell the transmitter to start the code group synchronization process. Since this is a DC signal, an optical implementation requires encoding before transmission. Due to the large number of data converters that could be used in the system, and therefore large number of SYNC signals, a likely implementation

Figure 2. Example board placement using JESD204B over optical (to scale)

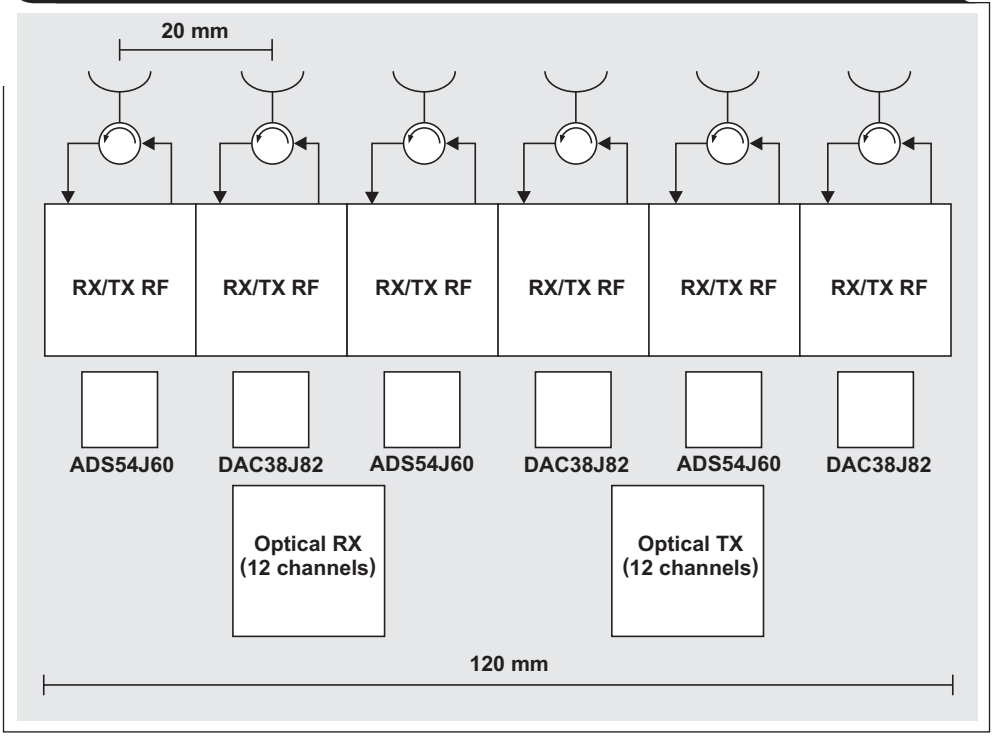
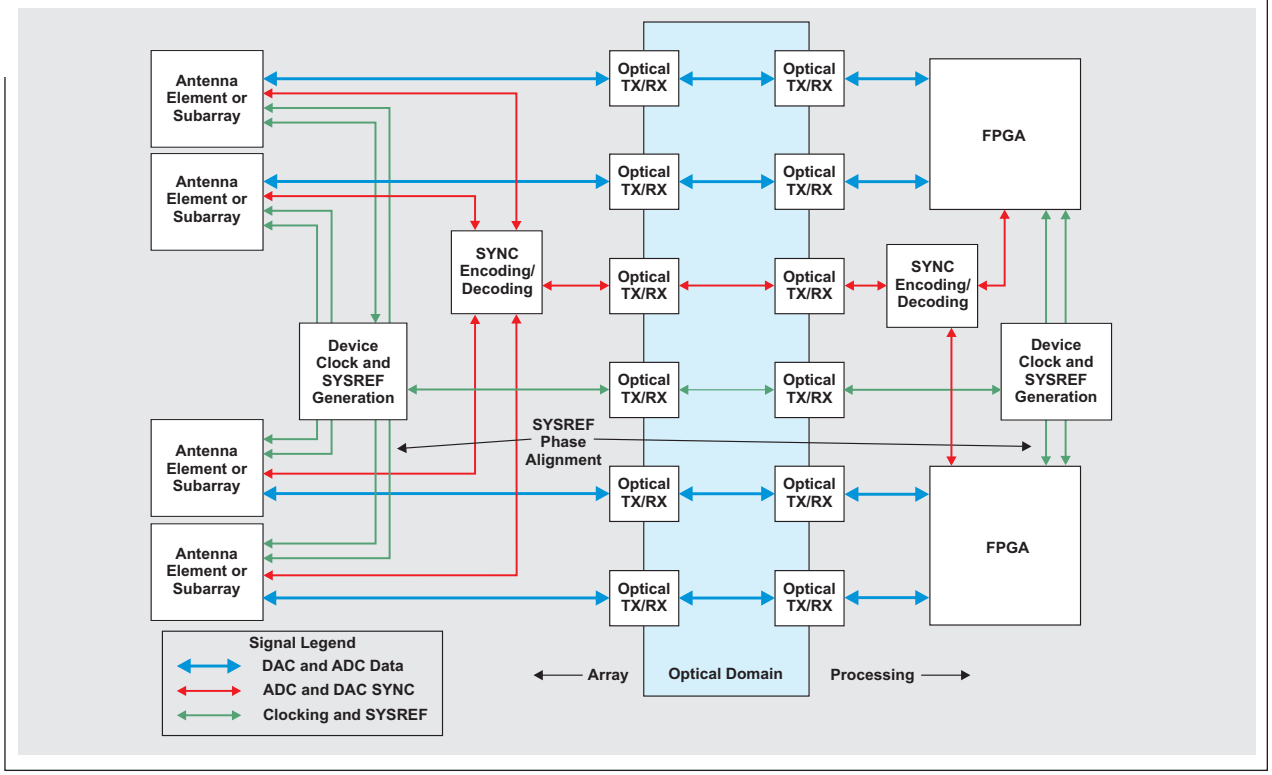


Figure 3. High-level phased-array radar system diagram using optical fiber in the JESD204B link



uses SYNC signal aggregation. A designer can do this by ANDing signals together to limit the total number of SYNC signals transmitted over the optical link. Note that SYNC can have timing requirements for subclass 1 implementations when numerically-controlled oscillators (NCOs) are used as part of digital up or down converters within the data converters.[3]

Figure 3 shows a high-level system block diagram of phased-array radar using an optical implementation of JESD204B. It is assumed that both the device clocks and SYSREF signals are generated at a single location at the array and distributed through traditional means to each antenna element to maintain high performance and phase alignment. The SYNC signals for each element can be aggregated at the subarray level (N SYNC signals in each direction for N subarrays in the system). An alternative is to aggregate each element at the system level before being encoded for transmission across optical to limit the number of signals.

Note that the clocks, including SYSREF and SYNC signals, can be sent over a copper interface such as coax cables, rather than over an optical link. The feasibility is dependent on the distance between the antenna elements and the FPGAs. A copper implementation of those signals is likely simpler, eliminating the encoding problem for SYNC and simplifying phase alignment of SYSREF.

Conclusion

There is little doubt that phased-array radars will continue to move toward the concept of digital phased-array radars, however, the optimal architecture is still debatable. The architecture discussed here, making use of JESD204B over optical, may enable entirely digital arrays for L-band, S-band, and C-band radars. This architecture reduces the total power and thermal requirements at each antenna element by eliminating the requirement for an FPGA to be near the data converters. Further reductions in optical transceiver size and power would make this architecture even more compelling.

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