Faster, cooler charging with dual chargers

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As the functionality and related power demands of the rechargeable battery-powered electronics such as smartphones and cameras grew, so did their batteries' capacities in order to extend run time. With higher-power wall adaptors and USB 3.x providing higher currents at 5 V, 9 V and 12 V, increasing the charger's input current limit to accept the additional power gives more charging current for faster charging. This also results in more losses that the charger dissipates as heat. Historically, these losses have been distributed through the PCB ground plane by careful placement of the external FETs with the charge-controller IC's. Consumer demand for smaller portable electronics has forced IC manufacturers to develop battery-charger ICs with integrated FETs (I-FETs) and with smaller packaging. Including thermal considerations early in the design is critical to ensure that these high-current, I-FET chargers provide the designed charge current without overheating the PCB.

Thermal management in portable devices requires careful PCB layout. For example, removing the heat from an IC in a QFN package with an exposed bottom thermal pad requires that the thermal pad be connected to a copper ground plane that is not thermally saturated, preferably exposed (as opposed to internal). Too many ICs in close proximity that are trying to use the same heat-sinking ground plane can saturate the plane with heat, causing the ICs to overheat and go into lower-power thermal-regulation mode, or even shutdown.

Additionally, when the ground plane of the printed-circuit board (PCB) is thermally saturated, the device's outside case temperature rises to unacceptable levels. To prevent this, each IC and a section of its adjacent ground plane should be allocated a portion of a thermal budget. The thermal budget sets a hard limit to the amount of heat that a single, small-footprint, I-FET charger, outputting several amperes of current, can dissipate without raising the device's case temperature.

For a buck charger with integrated FETs, the IC's efficiency is

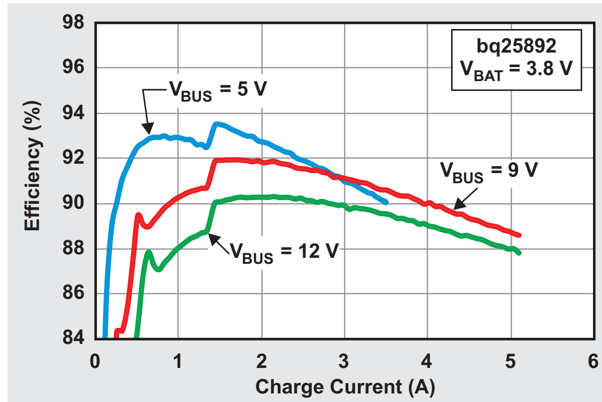
$$\eta = \frac{P_{OUT}}{P_{IN}} = \frac{V_{BAT} \times I_{CHRG}}{V_{BUS} \times I_{BUS}}$$

and loss through heat is

$$P_L = P_{IN} - P_{OUT} = P_{OUT} \times \left(\frac{1}{\eta} - 1\right)$$

At higher currents, this loss is dominated by the I^2R losses across the internal FETs. Figure 1 shows the efficiency of a battery charger, such as the bq25890, at different charging currents and input voltages.

Figure 1. Example of I-FET charger efficiency

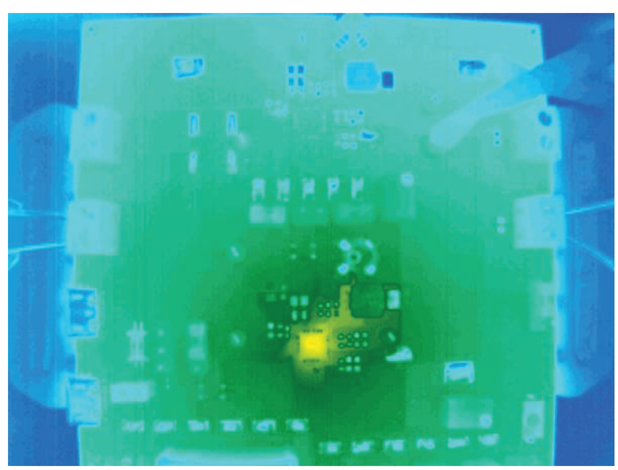


With a 9-V input adapter, a battery charger with 91% efficiency was set to provide a 3-A charging current to a 3.8-V charged battery with loses of

$$P_L = 3.8\ V \times 3\ A \times (1 / 0.91 - 1),$$

which equals 1.13 W in heat. The charger IC was soldered onto a four-layer, 31-mil thick, FR-4 board with 2-oz copper. The package's thermal pad was properly soldered down to the top-layer copper ground pour and through vias-to-ground pours on each of the internal and bottom layers. All of this copper acted as a heat sink. The image in Figure 2 shows a thermal image for a 4- by 4-mm QFN package where the temperature rise was 16.1°C at the IC's top-side case with a 25°C ambient air temperature. In this

Figure 2. Thermal image of single-charger operation (V_{IN} = 9 V, V_{BAT} = 3.8 V, I_{CHRG} = 3 A)



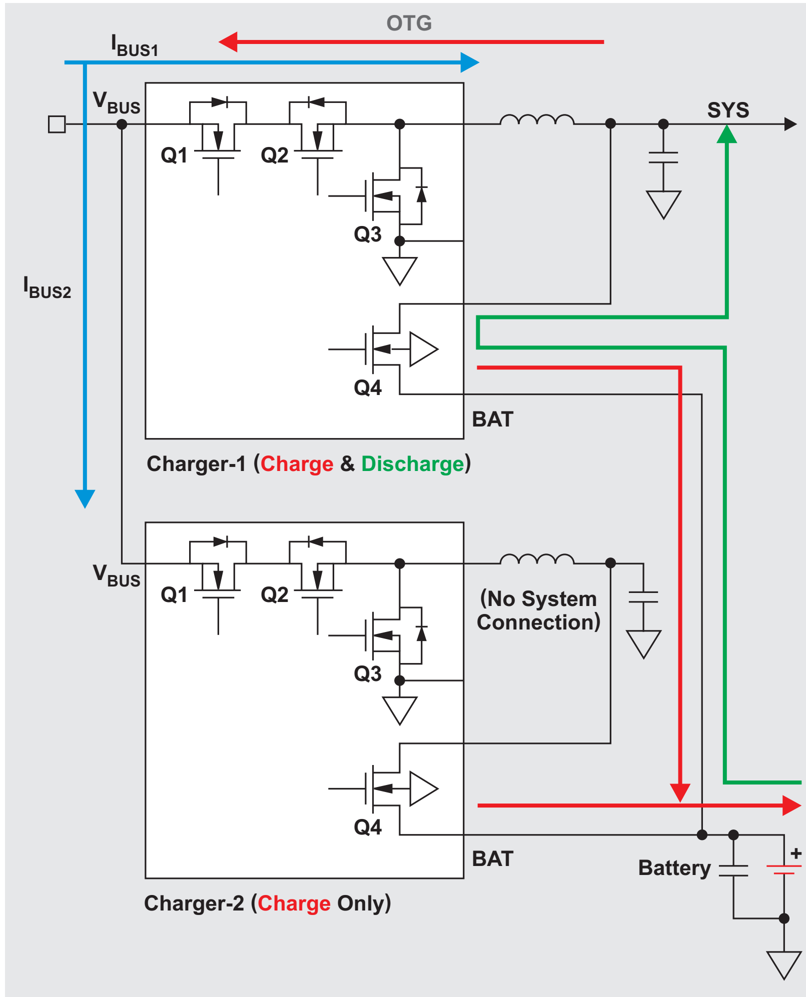
image, cool is shown as blue/green, warm as yellow, and hotter would show as red to white.

The PCB tested for Figure 2 contained no other power dissipating ICs, so the copper ground area approximates an infinite heat sink and was not saturated. This state is evidenced by the blue and green colors surrounding the yellow hot spot of the IC.

Increasing the charging current of this same charger by 50% to 4.5 A resulted in a temperature rise of 37°C compared to 25°C ambient. This temperature rise may be within the thermal budget of some devices, but not others.

Using the same concept of thermal distribution across the PCB as a charge controller with external FETs, two I-FET charger ICs in parallel, referred to as a dual-charger configuration, can be used. In general, there is no stability issue when connecting the battery-output pins of multiple chargers in parallel. This is because, while in constant-current (CC) mode, the charger's battery pin (BAT) has the characteristics of a high-impedance current source. While in constant-voltage (CV) mode, but well before termination, the battery pin characteristics are like a low-impedance voltage regulator. Dual-charger ICs in a parallel configuration are shown in Figure 3.

Figure 3: Dual-charger ICs in a parallel configuration



Charger-1 is configured for charging, however, if the internal battery FET (Q4) that provides a power path has low enough $R_{DS(on)}$, this IC also provides battery discharge through Q4. Charger-2 is configured only for charging. If required, charger-1 exclusively provides a USB On-The-Go (OTG) 5-V power rail at V_{BUS} after charger-2 has been configured for high-impedance mode. Even with the same termination voltage and current settings, and high regulation accuracy, one charger always attempts to terminate before the other due to the mismatch in each charger's internal reference voltages and currents. If both chargers are set to the same termination current, both chargers will have difficulty terminating the charge. Therefore, the termination current of one charger (typically charger-2) should be set higher than the other (typically charger-1) to allow for a smooth termination.

When the total required input current is high (for example, I_{CHARGE} > 5 A with a 5-V adapter), the parallel configuration is recommended for best thermal distribution. With both input pins connected, neither charger can use its control loop for automatic input-current-limit optimization (ICO) to extract maximum adapter power without causing loop instability at their mutual V_{BUS} node. Therefore, each charger's current-limit feature should be set to half the adapter's maximum output current. Inductor current ratings may also be reduced by half as well.

To prevent the V_{INDPM} loop from causing instability and to give charger-1 priority in powering the system, set the V_{INDPM} for charger-2 higher than that of charger-1. If the chargers have an integrated analog-to-digital converter (ADC) to provide real-time measurements of the charge current and the input, system and battery voltages, the host software must continuously monitor this information, as well as the loop status bits. The host software must then refresh each charger's current limit and charge current settings in order to maximize adapter power while balancing power and thermal loading between the two chargers.

When the total required input current is lower (for example, $I_{CHARGE} < 5$ A or an adapter change from 9 V to 12 V) and charger-1's reverse-blocking and current-limiting FET (Q1) has low enough $R_{DS(on)}$, the cascade configuration shown in Figure 4 may be a better option.

In the cascade configuration, charger-1 controls the total input current for both chargers. Host software development is greatly simplified because the V_{INDPM} and ICO features for charger-1 can be fully utilized to maximize adapter power extraction. In the event of a large system load transient while in the CV mode, the buck converter for charger-1 could see a higher input current. Therefore, the inductor for charger-1 needs to be sized to handle the adapter's full input current. If members of the same charger family with different I^{2}C addresses are available, say the bq25890 for charger-1 and bq25892 for charger-2, development is even easier because no additional hardware is required to switch between the I^{2}C communication lines of each charger.

Using the same PCB and test setup from Figure 2, the cascade chargers (Figure 4) were set to provide 2.25-A charge current to a 3.8-V battery and were 92% efficient. The heat loss for each charger was only

$P_L = 3.8\text{ V} \times 2.25\text{ A } (1/0.92 - 1) = 0.74\text{ W}.$

The top-side case temperature of both chargers rose above 25°C ambient by only 17°C, as measured by the thermal camera image in Figure 5. This is only 1°C above the single-charger case from Figure 2 for a 50% increase in charge current.

Figure 4: Dual-charger ICs in a cascade configuration

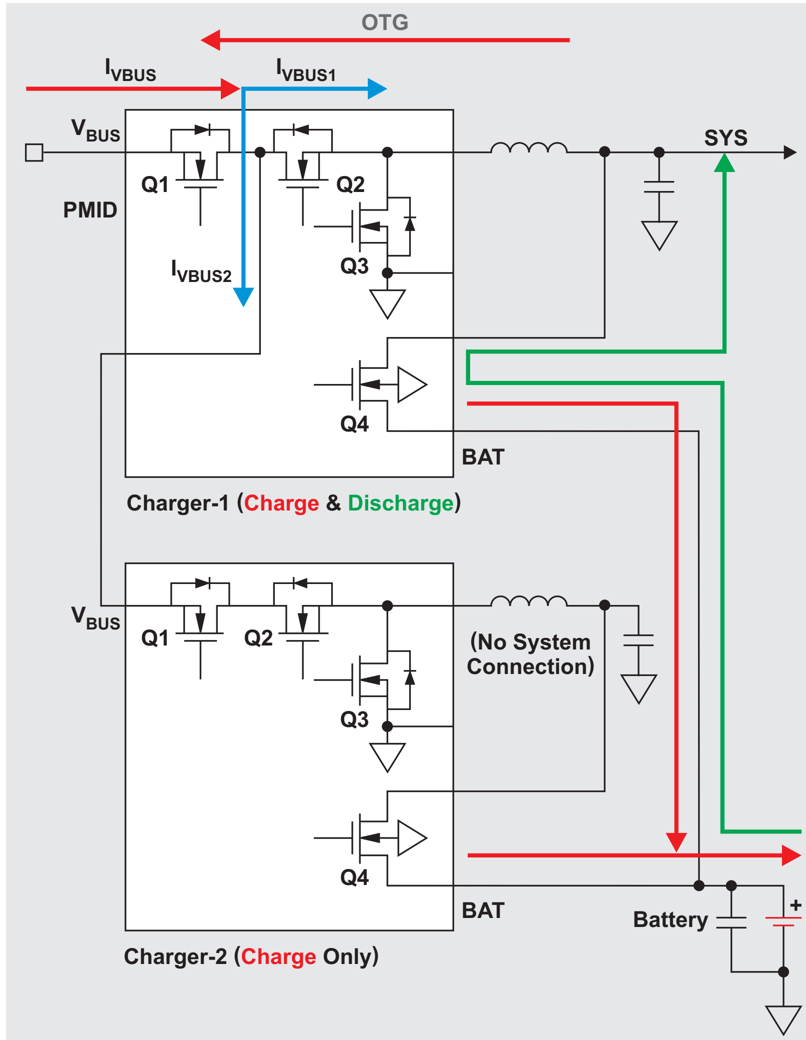


Figure 5. Thermal image of dual-charger operation (V_{IN} = 9 V, V_{BAT} = 3.8 V, I_{CHRG} = 4.5 A)

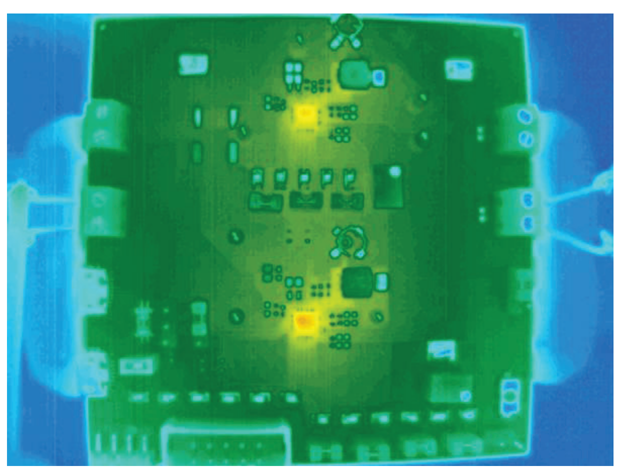
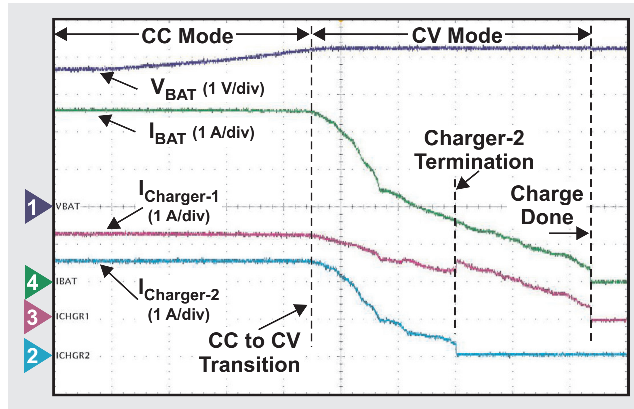


Figure 6 shows the typical charger-termination profile as the charger transitions from constant-current to constant-voltage regulation. Following the previous recommendation, for a clean termination, charger-2 terminates charging before charger-1.

Figure 6. Dual-charger charge-termination profile



Conclusion

Most battery-charger ICs have a thermal regulation loop that reduces their charge current in order to protect the IC from damage due to overheating. As such, PCB thermal management is critical to maximize the charge current (which reduces charge time) into today's high-capacity batteries in addition to maintaining practical outside case temperatures. Thermal management includes assigning thermal budgets to all heat-producing ICs, careful IC placement, and heat-sink grounding on the PCB to distribute heat without thermally saturating the copper pours and planes of PCB ground. Using I-FET dual chargers, either in a parallel or cascade configuration as the application allows, gives better heat distribution for lower IC and case temperatures along with faster, cooler charging and longer device run times.

Reference

1. "Dual Battery Charger IC Reference Design (connected in Cascode Configuration)," TI Designs, TIDA-00590

Related Web sites

Product information:
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