How to reduce current spikes at AC zero-crossing for totem-pole PFC

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Introduction

Power factor correction (PFC) is widely used in AC/DC power supplies with an input power of 75 watts or greater. PFC forces the input current to follow the input voltage so that any electrical load appears like a resistor. Amongst all the different PFC topologies, the totem-pole PFC[1, 2] has recently received more attention because it uses the least number of components, has the smallest conduction loss, and has the highest efficiency. Typically, a totem-pole PFC cannot operate in continuous-conduction mode (CCM) because of the slow reverse recovery of the MOSFET's body diodes. However, with the advent of the gallium-nitride (GaN) FET, its diode-free structure makes the CCM totem-pole PFC possible. Figure 1 is a totem-pole PFC structure.

In Figure 1, Q3 and Q4 are GaN FETs. Depending on V_{AC} polarity, they alternatively operate as a PFC active switch or a sync switch. To further improve efficiency, D1 and D2 are replaced with regular MOSFETs because the conduction loss for MOSFETs is lower than for diodes. The revised structure is shown in Figure 2 where Q1 and Q2 are regular MOSFETs and are driven at AC frequency.

The current flow paths for a totem-pole PFC are shown in Figures 3 and 4. During the positive AC cycle, Q4 is the active switch, while Q3 works as a sync FET. The driving signals for Q4 and Q3 are complementary: Q4 is controlled by D (duty cycle from control loop) and Q3 is controlled by 1 – D. When Q4 turns on, the current goes through the AC line, inductor, Q4, Q2, and then back to AC neutral. When Q4 turns off, Q3 turns on, the current goes through the AC line, inductor, Q3, load, Q2, and then back to AC neutral. Q2 stays on for the whole positive AC half-cycle and Q1 remains off.

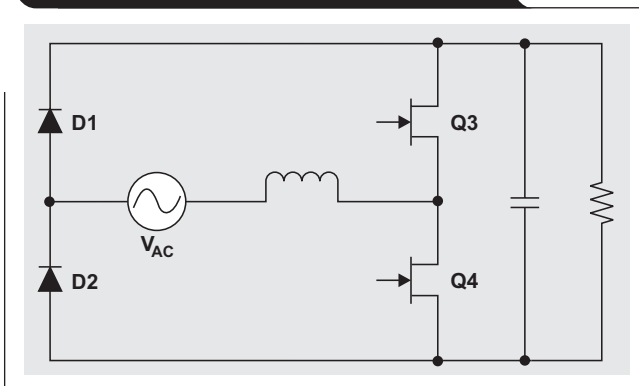**Figure 1. Totem-pole PFC with GaN FETs and line-rectification diodes**

Figure 2. Totem-pole PFC with GaN FETs and line-rectification MOSFETs
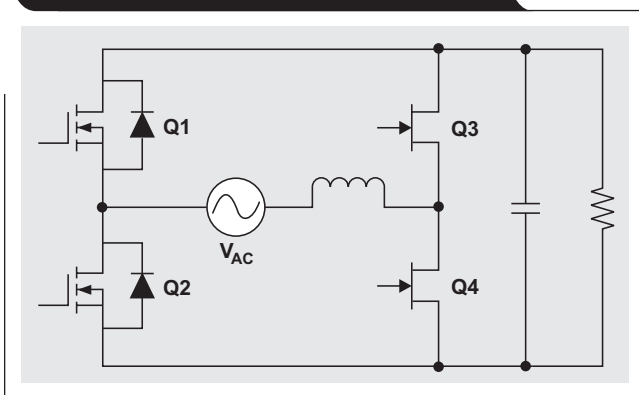

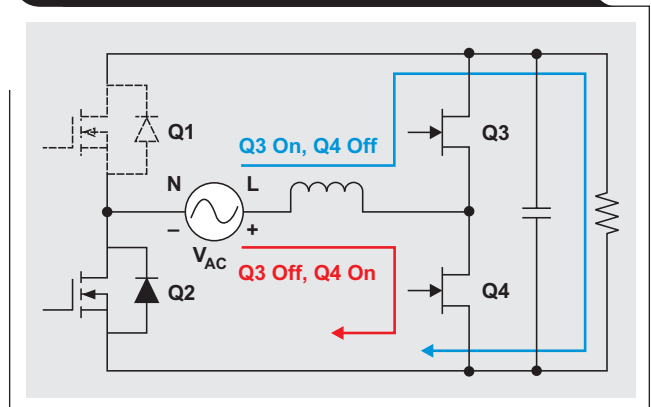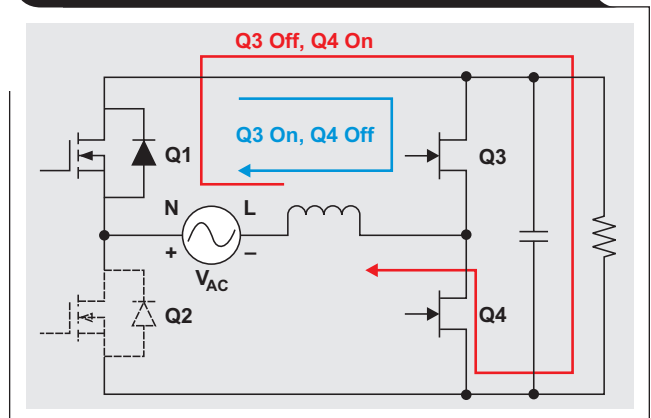**Figure 3. Current paths for positive AC cycle**

Figure 4. Current paths for negative AC cycle

During the negative AC cycle, the function of Q4 and Q3 swaps: Q3 becomes the active switch and Q4 works as a sync FET. The driving signal for Q4 and Q3 are still complementary, but Q3 is now controlled by D and Q4 is controlled by 1 – D. When Q3 turns on, the current goes through AC neutral, Q1, Q3, inductor, and then back to AC line. When Q3 turns off, Q4 turns on, the current goes through AC neutral, Q1, load, Q4, inductor, and then back to AC line. Q1 stays on for the whole negative AC half-cycle and Q2 remains off.

One of the challenges in totem-pole PFCs is that the input current has big spikes at the V_{AC} zero-crossing. The issue is inherent with totem-pole PFCs and very complicated. In fact, the spikes contain both positive and negative spikes, and they occur for different reasons. There are several scenarios that can cause current spikes.
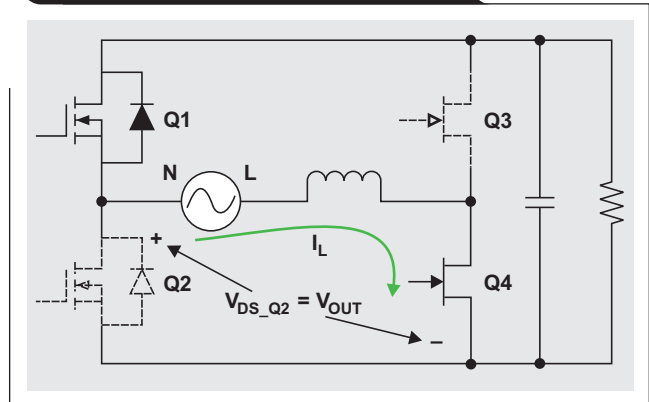
Scenario 1

As shown in Figure 5, when the operation mode changes from negative cycle to positive cycle at the AC zero-crossing, the duty ratio of switch Q3 changes abruptly from almost 100% to zero. The duty ratio of switch Q4 changes abruptly from zero to almost 100%. Because of the slow reverse recovery of the Q1 body diode and the large C_{OSS} of Q2, the V_{DS} voltage of Q2 still equals V_{OUT} (400 V). Since this high voltage is applied to the inductor when Q4 turns on, a positive current spike is generated. This scenario is analyzed in Reference 3 and a Q4 soft-start method is proposed to solve this issue.

Scenario 2

However, even with soft turn on of Q4, there are still excessive current spikes. This is because V_{AC} is very low right after zero-crossing and is therefore insufficient for the inductor current to build up. On the other hand, when Q3 turns on with 1 – D, even though its duty is not high, the voltage applied to the inductor is high (400-V V_{OUT}). The resulting high reverse current through the inductor causes a negative current spike.

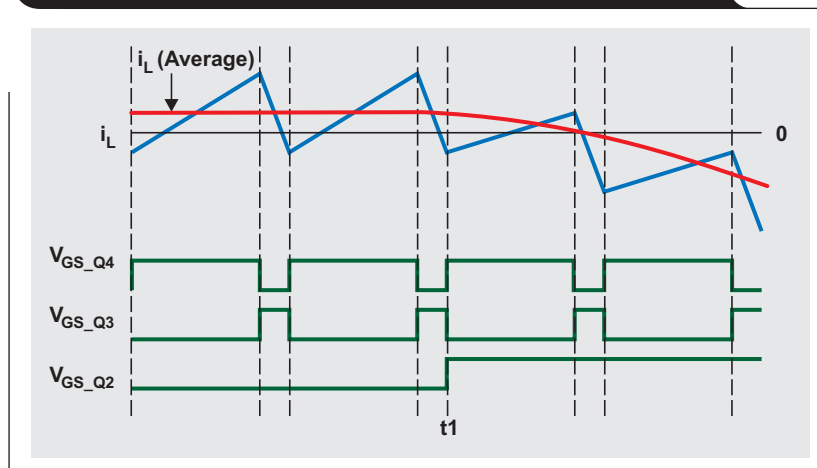**Figure 5. Current spike caused by sudden turn on of Q4**

Scenario 3

Timing for Q2 turn on is also critical. A short-through can occur if Q2 turns on before Q4 soft start and if the body diode of Q1 does not recover quickly enough.

Scenario 4

If Q2 turns on too late, a negative current spike can be generated (Figure 6). The high V_{BUS} voltage generates a reverse inductor current when Q3 is on while Q2 is off. This reverse current first turns off the Q2 body diode, then starts to charge C_{OSS} of Q2 and the V_{DS} of Q2 builds up to a high voltage. Then, when Q4 turns on, the high voltage ($V_{DS} + V_{IN}$) that is applied to the inductor results in high rising current in the inductor. Therefore, the inductor's rising and falling currents are both large magnitude, which achieves a balance that maintains the average current at a small positive value. Now, if Q2 suddenly turns on at t1, V_{DS} of Q2 will be clamped to zero. When Q4 turns on, only V_{IN} is applied to the inductor. Since V_{IN} is very small, which is insufficient for the inductor to build up current high enough, the inductor's rising current becomes very small. Because the falling current still has a large magnitude, the balance is broken and results in a large negative current spike.

Figure 6. Current spike caused by turning on Q2 too late

Reducing current spikes at AC zero-crossing

A new control method is provided in this article to solve the current-spiking issue. In this method, Q1, Q2, Q3, and Q4 are turned on with a special sequence and each executes a soft-start mechanism. The driving signals for this new method are shown in Figure 7:

In this solution, when V_{AC} changes from a negative to positive cycle, after AC zero-crossing, Q4 first turns on with a very small pulse width. The pulse width then gradually increases to D (the duty cycle generated by control loop). By doing a soft-start on Q4, Q1 completely reverse recovers. Now the voltage, V_{DS}, of Q2 gradually reduces to ground, thus the positive spike caused by scenario 1 is eliminated.
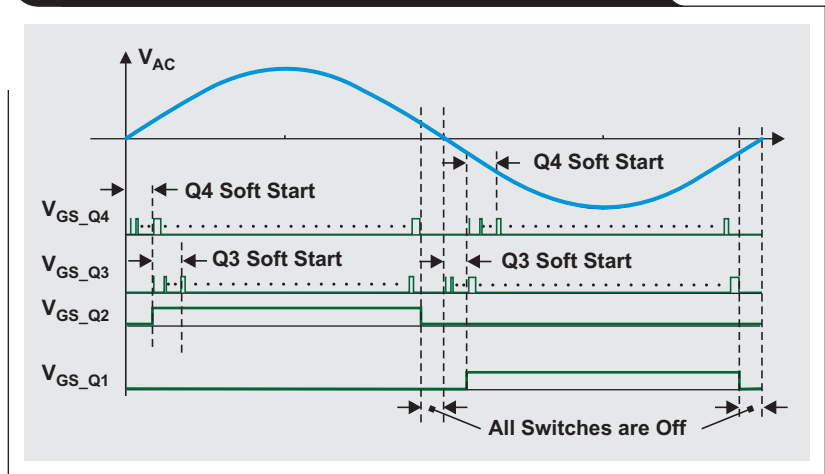
Once the Q4 soft-start is complete, the sync FET, Q3, starts a soft turn-on with a tiny pulse width and gradually increases until the pulse width reaches 1 – D. This eliminates the negative current spike caused by scenario 2.

At the same time when the Q4 soft-start is complete and the Q3 soft-start begins, the low frequency switch, Q2, is turned on. Since the body diode of Q1 is already recovered, there is no short-through issue as mentioned in scenario 3.

Also, since Q3 starts with a very small pulse width, it is insufficient for an inductor to build a negative current high enough, and thus eliminates the current spike caused in scenario 4.

Finally, the zero-crossing detection could be mistriggered by noise. For safety purposes, all the switches are turned off at the end of a positive cycle. This leaves a small dead zone to prevent the input AC from short circuiting. Note that the control loop should freeze during

Figure 7. Gate signals timing for proposed method

this dead zone. Otherwise, when the PFC turns back on, the integrator build-up in the loop generates a large PWM pulse, which can cause a large current spike.

The same operation principle applies to the AC transition from a positive to a negative cycle.

Experiment results

The method proposed earlier was verified on a 1-kW totem-pole PFC that was controlled with a UCD3138 digital controller from Texas Instruments. Figure 8 is the current waveform with a traditional control method and Figure 9 shows the current waveform with the proposed method. Both were tested with the same conditions. Notice how the current spikes are significantly reduced with the proposed method and the current waveform becomes much smoother at AC zero-crossing. As a result, the total harmonic distortion (THD) is reduced from 8.1% to 3.7%.

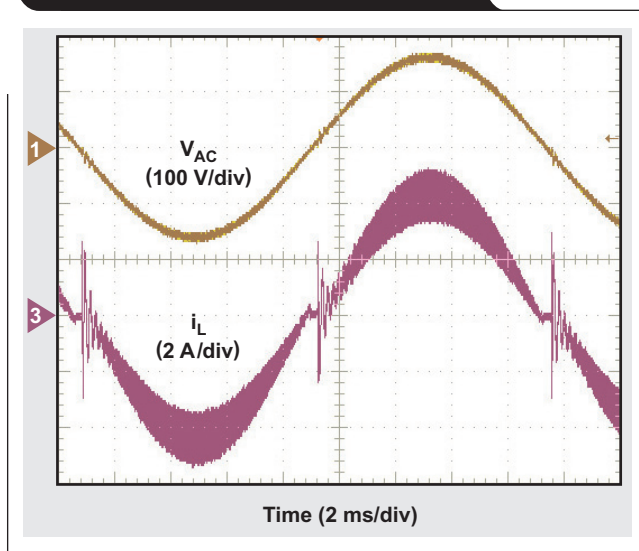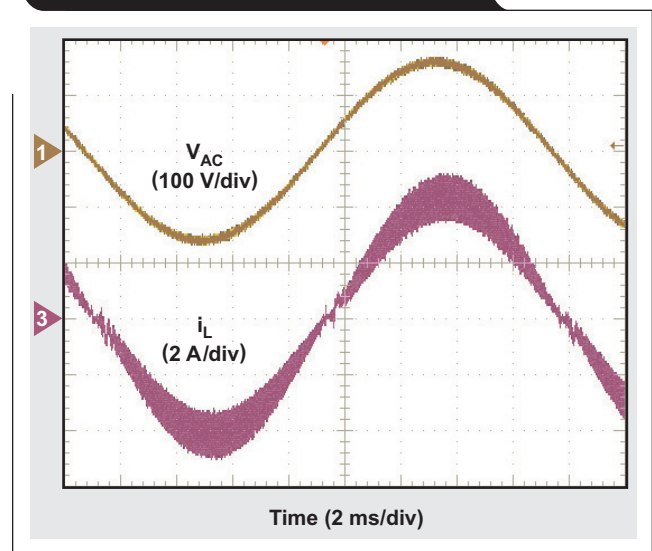Figure 8. Current waveform using a traditional control method

Figure 9. Current waveform with the proposed control method

Conclusion

While totem-pole PFC is attracting more attention, some design challenges prevent it from being widely adopted. One inherent issue in a totem-pole PFC is the current spikes at AC zero-crossing. The causes for current spikes are complicated: turn-on sequence, slow reverse-recovery of MOSFET's body diode, large C_{OSS} of MOSFET, sudden turn on of the active FET with almost 100% duty cycle, sudden turn on of the sync FET, and so on. All these scenarios contribute to spikes. By turning the switches on with a special sequence, and executing a soft-start mechanism on both the main and sync FETs, current spikes can be significantly reduced and THD is significantly improved.

References

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2. L. Huber, Y. Jang and M. Jovanovic, "Performance Evaluation of Bridgeless PFC Boost Rectifiers", IEEE Transaction on Power Electronics, Vol. 23, No. 3, May 2008.

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