Understanding frequency variation in the DCS-Control™ topology

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Introduction

A common requirement in automotive, communications equipment and industrial markets is to avoid interfering with specific frequency ranges, such as the AM radio band, to minimize disturbances for sensitive electronics, such as sensors. One example for reducing interference from power supplies is setting their switching frequency above the sensitive frequencies to keep switching noise at a higher frequency.

If the frequency is set below sensitive frequencies, then higher-frequency harmonics would be in band and possibly cause interference. Most modern power supplies do not use an actual oscillator to set their switching frequency, as in traditional voltage- or current-mode control. Instead, either the on-time or off-time is controlled, which then provides a relatively constant operating frequency.

DCS-Control™ topology is an example of a topology that is on-time based, which efficiently provides the low-noise and fast-transient response needed in many applications. While the switching frequency of this topology does vary, this variation is understood, controlled, and usually sufficient for frequency-sensitive applications such as automotive, communications equipment, test and measurement, and factory automation.

Application example

Figure 1 shows the basic block diagram of the DCS-Control topology used in a typical automotive infotainment device.[1, 2]

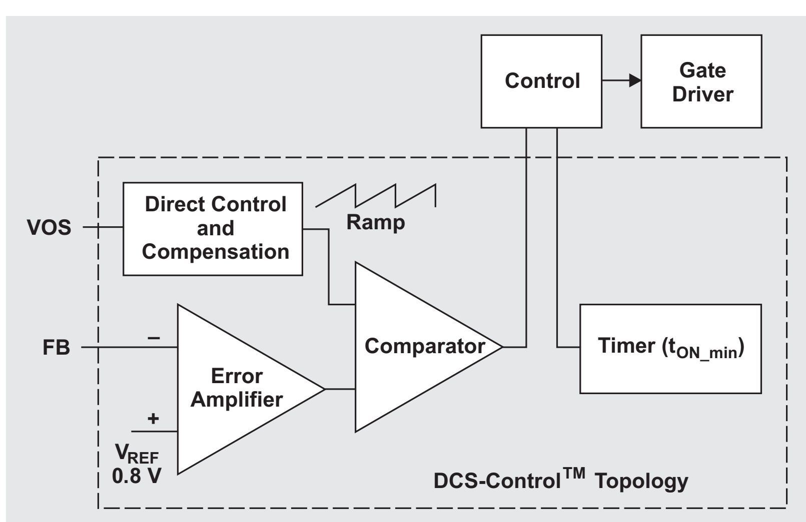
As explained in Reference 1, the timer (t_{ON_MIN}) is responsible for providing a controlled switching frequency by adjusting the on-time based on V_{IN} and V_{OUT} through Equation 1.

$$t_{ON} = \frac{V_{OUT}}{V_{IN}} \quad 400 \text{ ns} \tag{1}$$

The 400-ns value sets the ideal switching frequency to 2.5 MHz when the DCS-Control device is operating with the on-time set by the timer. However, due to circuit losses, propagation delays, and in some specific application conditions, operation does not always follow the on-time set by the timer. As a result, the frequency varies. The reasons for this variation are grouped together based on the duty cycle, ideally V_{OUT}/V_{IN}, at which the device operates.

Measured data explains the principles behind the DCS-Control topology's frequency variation. To better explain the concepts, the TPS62130 (catalog version) was chosen and it offers two switching frequencies: 2.5 MHz and 1.25 MHz. The 2.5-MHz data exactly matches the TPS62130A-Q1 data because both converters offer the 2.5-MHz setting. All data was taken on the evaluation module with a 2.2-µH inductor and two 22-µF output capacitors (to overcome the DC bias effect).[3]

Figure 1. Block diagram of the DCS-Control™ topology in the TPS62130A-Q1 converter



Moderate duty cycles

In the typical application of converting the 12-V car battery to 5 V for universal serial bus (USB) ports, the required duty cycle is not extremely high or low. Frequency variation in this case is very low because the on- and off-times are not at their extremes. Figure 2 shows the measured switching frequency, on-time, and off-time with a 5-V output voltage, two frequency settings, and two different load currents. A moderate duty cycle refers to those input voltages above 9 V for the 2.5-MHz setting and above 7 V for the 1.25-MHz setting.

Figure 2b shows the reason behind the low levels of frequency variation. The on-time matches very well to the ideal on-time set by the timer and to Equation 1 for both loads and frequency settings. The reasons for the small frequency variation with moderate duty cycles are: overcoming losses and propagation delays.

In Figure 2a, the frequency increases with heavier loads due to losses. Higher loads require slightly higher duty cycles to overcome resistive losses in the circuit. Since the on-times are the same for both the 1-A load and 3-A load, the off-time is decreased to achieve the higher duty cycle (Figure 2c). The same on-time and a shorter off-time results in a shorter period and higher frequency.

Also, the frequency decreases slightly with increasing input voltage. Because the on-time decreases with increasing input voltage, fixed propagation delays in the device have a more significant effect on the achieved on-time for smaller on-time values. The timer sets the on-time to achieve a certain frequency, but its output signal goes through the control and gate driver (shown in Figure 1) before reaching the power transistors. This path takes some finite amount of time. For example, if a 200-ns on-time is desired and the propagation delay is 20 ns, the actual on-time is 220 ns, which is 10% higher than desired. But, if the input voltage increases and the desired on-time reduces to 100 ns, the same 20-ns delay produces a 20% increase in the actual on-time. This effect is further pronounced for low duty cycles.

High duty cycles

While a car battery nominally operates at ~12 V, transients from high-current loads, such as starting the engine, can reduce the battery voltage. To the power supply this appears as a line transient, which means more advanced regulation is required in some applications. As long as the input voltage does not decrease below the level of the output voltage, the DCS-Control topology maintains output regulation during such line and load transients.

Figure 2. TPS62130 with a 5-V output

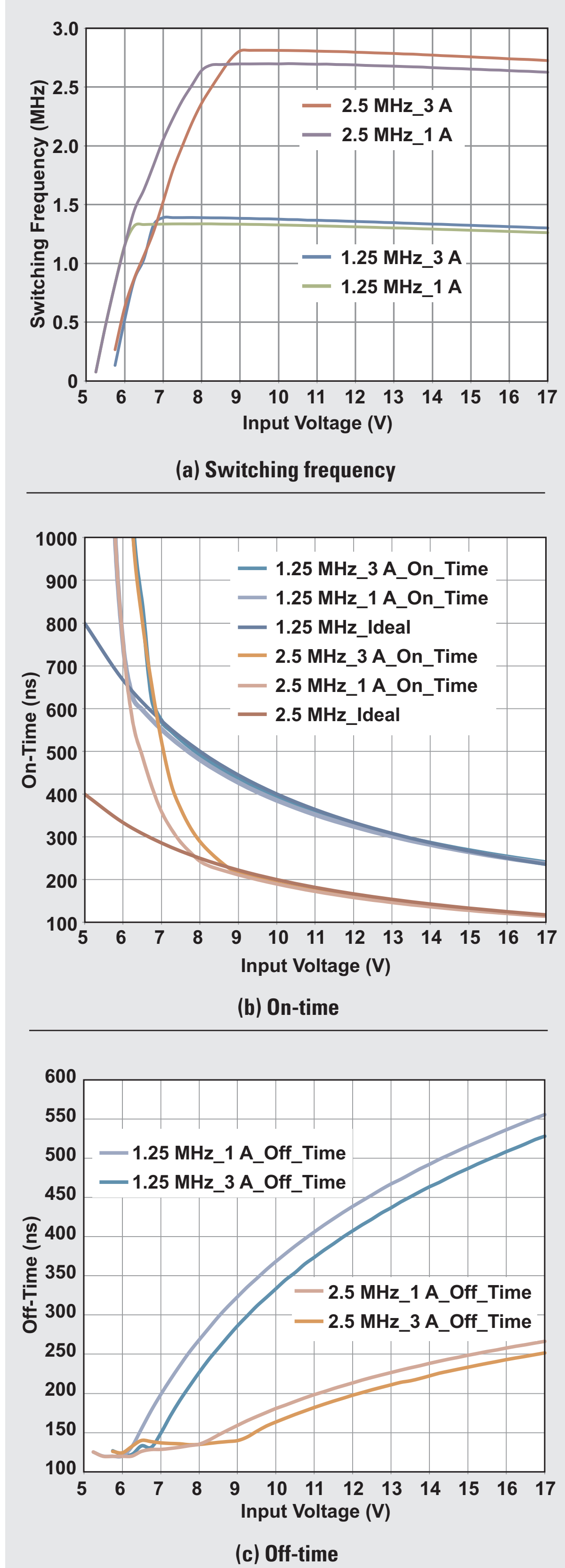


Figure 3 shows measured data for a 3.3-V output. When the input voltage of the converter drops, the duty cycle increases. At high duty cycles, the switching frequency decreases due to losses and a minimum off-time. High duty cycles refers to the left-most portion of Figures 2a and 3a where the switching frequency decreases from its nominal value towards zero.

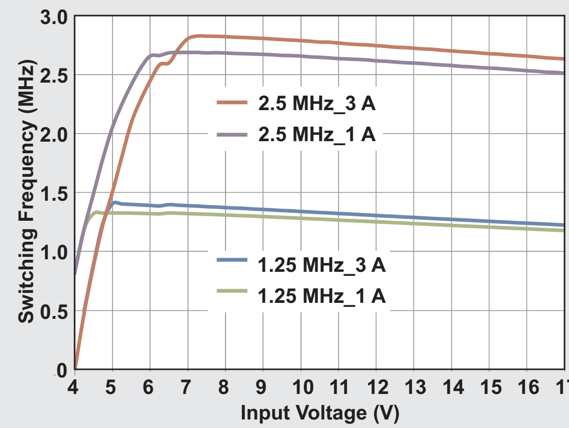
High duty cycles demonstrate a minimum off-time in the topology. Since high duty cycles occur at a lower input voltage and higher output voltage, the energy stored in the inductor during the on-time is lower. This outcome is because there is much less voltage across the inductor. To maximize efficiency, a minimum off-time is included to ensure that sufficient energy is delivered to the output. This is especially helpful in power-save mode, in which a certain amount of energy is delivered so the output stays higher for a longer time. This results in a gap between switching pulses and higher efficiency. From Figure 3c, once the minimum off-time is reached (around a 6-V input voltage for the 2.5-MHz setting), the on-time begins to rise from ideal in order to achieve the required increase in duty cycle that corresponds to the lower input voltage. Figure 2c and Figure 3c show the 120-ns approximate value of the minimum off-time.

Furthermore, the minimum off-time is quickly reached at high duty cycles because the input voltage value is lower as well. At input voltages below 6 V, the resistance of the high-side MOSFET ($R_{DS(on)}$) inside the DCS-Control device increases, thus creating higher losses and a greater required extension of the duty cycle. For example, 3-A loads show longer on-times than 1-A loads at lower input voltages.

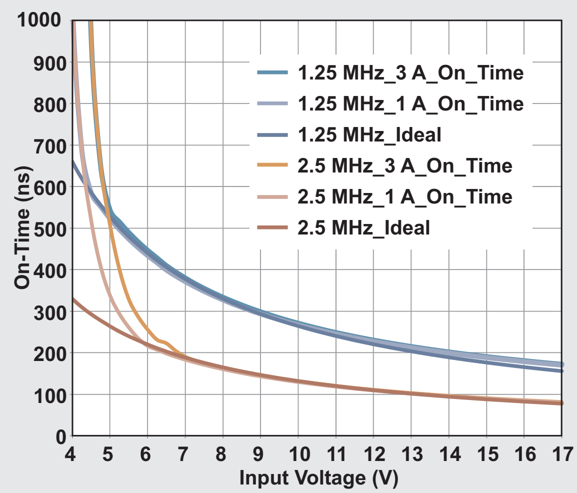
Low duty cycles

Low duty cycles occur with lower output voltages, such as 1 V and 1.8 V. The relatively high 12-V input voltage requires duty cycles of sometimes less than 10%. With respect to the desired 400-ns period, this requires on-times near and even below 40 ns. Such small on-times are challenging for any converter to achieve, or are actually impossible due to absolute minimum on-times. The TPS62130 data sheet notes a typical 80-ns absolute minimum on-time that occurs in these cases. This is the primary source of frequency variation at low duty cycles. Fixed propagation delays added to small on-times are another source of variation, as explained before. Figure 4 shows measured data for a 1.8-V output voltage.

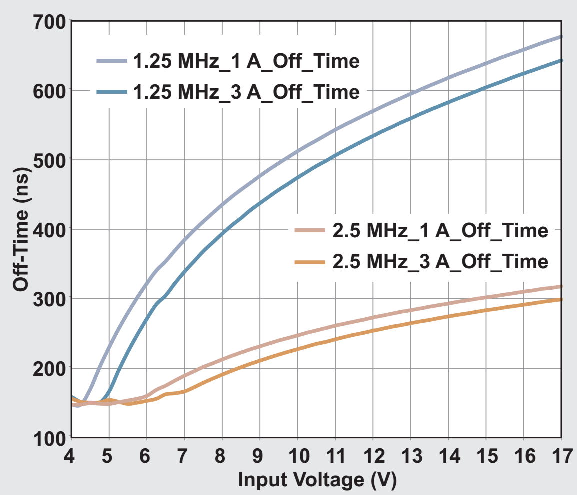
Figure 3. TPS62130 with a 3.3-V output



(a) Switching frequency



(b) On-time



(c) Off-time

The 2.5-MHz curves in Figure 4b clearly show a minimum on-time in the 80-ns range. This sets an upper boundary on the achievable switching frequency. The 1.25-MHz curves show good frequency variation similar to Figures 2a and 3a. Due to smaller on-times with this 1.8-V output, fixed propagation delays cause a sharper downward frequency shift versus higher output voltages, which result in a lower frequency.

Additionally, the bumpiness seen in the 2.5-MHz curves (Figure 4a) shows a third impact to the on-time: the comparator. During a transient, the comparator extends the on-time past the output of the timer to deliver more energy to the output to make the output voltage recover faster. This is a key aspect of a hysteretic converter and explains the fast transient response of the DCS-Control topology.

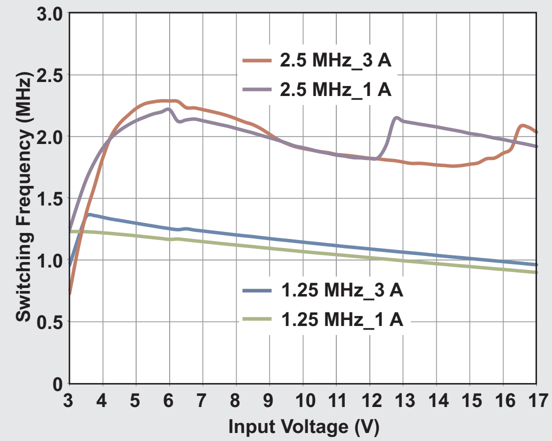
While the 80-ns minimum on-time and the output of the timer do not change much over the input voltage range, the output signal does change due to the changing ripple on the inductor current. There is increased ripple with higher input voltages. Having more ripple across the equivalent series resistance (ESR) and equivalent series inductance (ESL) in the output capacitors creates more signal for the comparator on which to react, making the system faster. Between 12 and 13 V, there is enough signal and the comparator no longer controls the on-time. The minimum on-timer controls it. Thus, higher frequency is achieved above this input voltage.

One solution to the lower frequency is a two-stage conversion of the 12 V to the load. A two-stage conversion (via 5 V, for example) to very-low output voltages achieves a higher frequency in both stages because of the more moderate on-times of each stage.

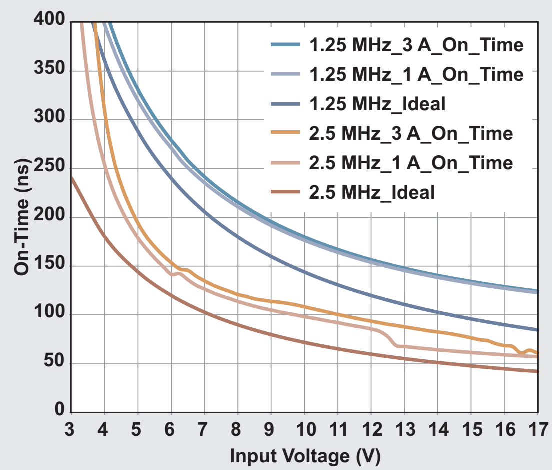
Finally, the lower switching frequency that occurs with lower output voltages will increase the inductor current ripple, but this ripple is already lowered because of the low output voltage (Equation 2). Lower output voltages have less current ripple to begin with. When following the datasheet recommendations for inductance and switching frequency, this lower switching frequency does not limit the output current below the 3-A device rating.

$$\Delta I_{L(max)} = V_{OUT} \times \left(\frac{1 - \frac{V_{OUT}}{V_{IN(max)}}}{L_{(min)} \times f_{SW}} \right) \quad (2)$$

Figure 4. TPS62130 with a 1.8-V output



(a) Switching frequency



(b) On-time

Conclusion

The switching frequency of the DCS-Control topology and other non-oscillator-based control topologies vary with changes in the application conditions. Depending on the duty cycle, the on-time and the frequency are affected by losses, the minimum off-time, the absolute minimum on-time, propagation delays, or the comparator. This behavior is understood and expected, and output voltage regulation is maintained. The lower operating frequency provides higher efficiency with no reduction in output current capability. High-frequency operation is maintained for the common applications of USB ports and system rails with higher voltages.

References

1. Chris Glaser, "High-efficiency, low-ripple DCS-Control offers seamless pulse-width modulation (PWM)/power-save transitions," *TI Analog Applications Journal*, 3Q 2013 (SLYT531)
2. Datasheet, "TPS6213xA-Q1 3V to 17-V 3A Step-Down Converter with DCS-Control™," Texas Instruments, May 2014
3. TPS62130EVM-505, "Evaluation Module for TPS62130 a 3-A, synchronous, step-down converter in a 3x3-mm, 16-pin QFN," Texas Instruments

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