TPS650860 Power Management Integrated Circuit

Fully programmable PMIC for various FPGA, processor and system applications

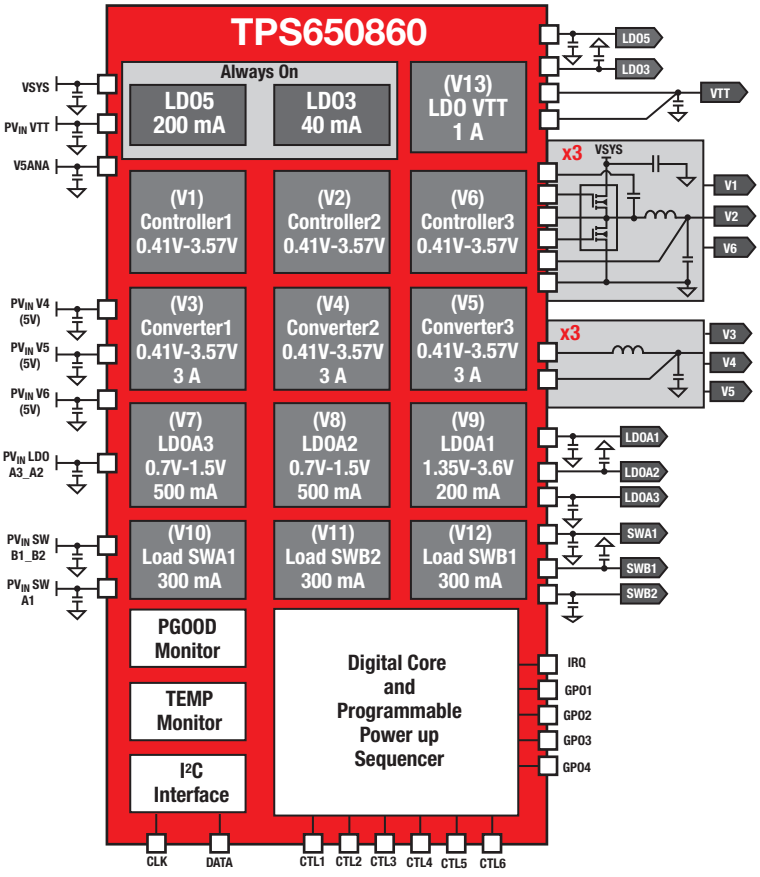
TEXAS INSTRUMENTS

Reduce board space

TI's TPS650860 is a fully versatile and feature rich Power Management Integrated Circuit (PMIC). With assembled sets (three of each) of programmable and power efficient controllers, converters, LDOs, and load switches; this device is ideal for many different processor, FPGA, and system applications. The same design can be easily modified and utilized for next generation applications which might require different output voltages, output currents, or different power up or power down sequences. By incorporating all the essential logic to support any simple or complex power up or power down sequences, it will drastically reduce design complexity, design time, and board space. The TPS650860 also integrates much enhanced monitoring and supervisory logic for output voltages, over current, die temperature, under-voltage lockout (UVLO), and critical temperature, which simplifies board design, reduces board space, and improves system reliability.

Fully controllable

The TPS650860 uses I2C interface (with programmable device address) which supports standard mode (100 KHz), fast mode (400 KHz), and fast mode plus (1 MHz) for communication with the host. Either digital input pins (CTL1 to CTL6) or I2C interface can be used to enable/disable the voltage rails to enter or exit low power state (phase) or to enable/disable (shut down) the TPS650860. When CTL pins are used to enable the voltage regulators, any of the CTL pins can be used to enable or disable one or multiple voltage regulators in any sequence with programmable delay between them. One or two of the CTL pins can also be used to change one, multiple, or all of the output voltages automatically for the controllers, converters, or LDOs. This feature can be used to enter or exit lower power state (phase) automatically with just toggling one or two CTL pins. Due to these rich capabilities, the same design can be leveraged in multiple platforms with minimum efforts.



Key Features

- Completely programmable power up and power down sequences
- Full DVS and decay support
- Programmable power good and power fault detection for all rails
- Up to four GPOs, controlled through I2C
- Temperature monitoring (hot and critical)

Digital control

The TPS650860's IRQ and GPOs (GPO1 to GPO4) pins can be configured to provide status of the device and output rails. Outputs of all the rails are being monitored to be within their nominal output voltages. TPS650860 can be configured to automatically shut down or inform the system/host through IRQ or one of the GPO ports in case of Power Good error or device temperature. There are also status registers which can be accessed through I2C interface that can provide the live and history of Power Good signals. Three of the four GPO pins can be configured as either open drain or push poll; one is open drain only. The state of GPO pins can either be controlled by I2C, by device temperature status, by Power Good status of one, multiple, or all voltage regulators, or be used as level shifter for one of the CTL input pins.

The PMIC also has a full range of capabilities to help debug and identify the system issues related to all the rails which it provides. I2C interface provides dynamic and static (failure history) status of all the rails. I2C interface can also be used to enable and disable individual or multiple rails in order to detect and debug system issues.

Save power with dynamic voltage scaling

PMICs and controllers support a wide range of input voltage for their VSYS. Since Controllers use external FETs, they can support a wide range of output current based on their external FET size. All the controllers and converts in TPS650860 have 7 bits of VID composition and support full dynamic voltage scaling (DVS) with programmable slew rate and decay mode, which can be used to save power during normal operation or power saving phase (standby phase). The DVS steps can be set from 10-mV to 25-mV steps which are used for each of the converters or controllers independent of each other. The capability of adjusting output voltage will increase the battery life and reduce the system thermal. If one of the system's nominal operating voltages is 2.5V and can be reduced to 2.4V during normal operation, through DVS capability of this device, it will result in 4% power saving on this voltage rail. Also by using the DVS and decay feature of these rails, their output voltage can be lowered during lower power state (standby phase) of the system to save power. By using the decay feature of these rails instead of DVS it will help to save even more power by not forcing to discharge the energy stored on the output capacitors of the rails when their output voltages are lowered.

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