Analog Applications Journal

Third Quarter, 2015

Contents

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Introduction

The *Analog Applications Journal* (AAJ) is a digest of technical analog articles published quarterly by Texas Instruments. Written with design engineers, engineering managers, system designers and technicians in mind, these "how-to" articles offer a basic understanding of how TI analog products can be used to solve various design issues and requirements. Readers will find tutorial information as well as practical engineering designs and detailed mathematical solutions as they relate to the following applications:

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- Industrial
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AAJ articles include many helpful hints and rules of thumb to guide readers who are new to engineering, or engineers who are just new to analog, as well as the advanced analog engineer. Where applicable, readers will also find software routines and program structures and learn about design tools. These forward-looking articles provide valuable insights into current and future product solutions. However, this long-running digest also gives readers archival access to many articles about legacy technologies and solutions that are the basis for today's products. This means the AAJ can be a relevant research tool for a very wide range of analog products, applications and design tools.

Ten tips for successfully designing with automotive EMC/EMI requirements

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Introduction

The automotive industry and individual automobile manufacturers must meet a variety of electromagnetic compatibility (EMC) requirements. For example, two requirements are to ensure that electronic systems do not emit excessive electromagnetic interference (EMI) or noise, and to be immune to the noise emitted by other systems. This article explores some of these requirements and offers some tips and techniques that can be used to ensure that equipment designs are compliant with these requirements.

Overview of the requirements for EMC

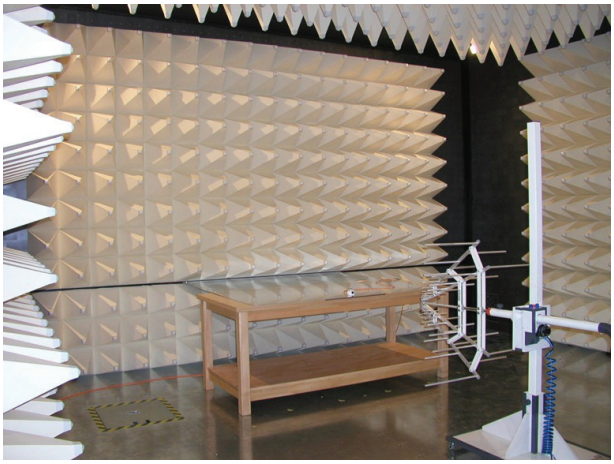
CISPR 25 is a standard that presents several test methods with suggested limits to evaluate the level of radiated emissions from a component to be installed in a vehicle.[1, 2] In addition to the guidance that CISPR 25 provides to manufacturers, most manufacturers have their own set of standards to augment the CISPR 25 guidelines. The primary purpose of CISPR 25 testing is to ensure that the component to be installed in the automobile will not interfere with other systems within the vehicle,

CISPR 25 requires that the electromagnetic noise level in the room where the test is performed must be at least 6 dB lower than the lowest levels being measured. Since CISPR 25 has places where it looks for levels as low as 18 dB (µV/m), an ambient level of less than 12 dB (µV/m) is needed. As reference, this is approximately the field strength for a typical AM radio station, 1 km from the antenna.[3]

In today's environment, the only way to meet this requirement is to perform testing in a special chamber that is designed and built to shield the testing environment from outside fields. Additionally, since normal budgets require that the chamber be of finite size, it is important to protect the testing environment from reflections of signals generated within the room. Therefore, test-chamber walls must be lined with a material that will not reflect electromagnetic (EM) waves (Figure 1). Test chambers are expensive and typically rented by the hour. To save costs, it is a good idea to evaluate EMC/EMI issues during the design phase to achieve first-time success in the chamber.

Another testing standard is the ISO 11452-4 Bulk Current Injection (BCI) suite of tests that are used to verify if a component is adversely affected by narrow-band electromagnetic fields. Testing is done by inducing disturbance signals directly into the wiring harnesses with a current probe.

Figure 1. Typical testing chamber with special conical tiles to stop reflections



10 tips for successful EMC testing

1. Keep loops small

When a magnetic field is present, a loop of conductive material acts as an antenna and converts the magnetic field into a current flowing around the loop. The strength of the current is proportional to the area of the enclosed loop. Therefore, as much as possible, keep loops from existing, and keep any required enclosed areas as small as possible. An example of a loop that might exist is when there is a differential data signal. A loop can form between the transmitter and the receiver with the differential lines.

Another common loop is when two subsystems share a circuit, perhaps a display and an engine control unit (ECU) that drives the display. There is a common ground (GND) connection in the chassis of the vehicle—a connection to this GND at the display end and at the ECU end of the system. When the video signal is connected to the display with its own ground wire, it can create one huge loop within the ground plane. In some cases, a loop like this is unavoidable. However, by introducing an inductor or a ferrite bead in the connection to ground, a DC loop can still exist, but from an RF emissions standpoint, the loop is broken.

Also, a loop is formed by every differential driver/receiver pair when a signal is sent over the twisted-pair cable. Generally, this loop has a small area for the cable portion of the link because the twisted-pair is tightly coupled. However, once the signal gets to the board, close coupling should be maintained to avoid opening up the loop area.

2. Bypass capacitors are essential

CMOS circuits are very popular, in part, because of their high speed and very-low power dissipation. An ideal CMOS circuit only dissipates power when it is changing states and when the node capacitances need to be charged or discharged. From a power-supply standpoint, a CMOS circuit that requires 10 mA on average may be drawing many times that during clock transitions, then little or no current between cycles. Therefore, emission-limiting techniques are focused on peak voltage and current values rather than average.

Current surging from the power supply to the power pin on a chip during clock transition is a prime source for emissions. By placing a bypass capacitor close to each power pin, the current required to supply the chip during the clock edge comes directly from the capacitor. Then the charge on the cap builds up with a lower, steadier current between cycles. Larger capacitors are good for supplying large surges of current, but tend to react poorly to very high-speed demands. Very small capacitors can react quickly to demand, but their total charge capacity is limited and can quickly become exhausted. The best solution for most circuits is to use a mix of different-sized capacitors in parallel, perhaps 1-µF and 0.01-µF capacitors in parallel. Place smaller size capacitors very close to the chip's power pins, while larger-sized capacitors can be placed further away.

3. Good impedance matching minimizes EMI

When a high-speed signal is sent through a transmission line and it encounters a change in the characteristic impedance on that line, part of the signal is reflected back to the source of the signal and part continues along in the original direction. Invariably, the reflection leads to emissions. For low EMI, good high-speed design practice is a necessity. There are a plethora of good sources for transmission-line design information.[4, 5] Here are some suggested precautions when designing transmission lines:

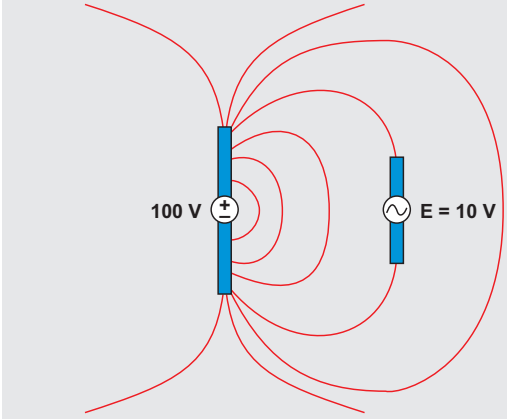
- Remember that the signal exists between the ground plane and the signal trace. Emissions can be caused by an interruption in either the signal trace or the ground plane, so pay attention to ground plane cutouts or discontinuities beneath the signal trace.
- Try to avoid sharp angles on the signal trace. Nicely curved corners are much better than right-angle turns.
- Often times, an FPD-Link signal will have components tapped off of it; such as power over coaxial cable, power connections, AC-coupling caps, and many others. To minimize the reflections at the components, try to use small components such as 0402 size and set the width of the trace to be the same as the width of the 0402 component pad. Also, be sure to set the characteristic impedance of the trace by controlling the dielectric thickness in the stackup.

4. Shielding

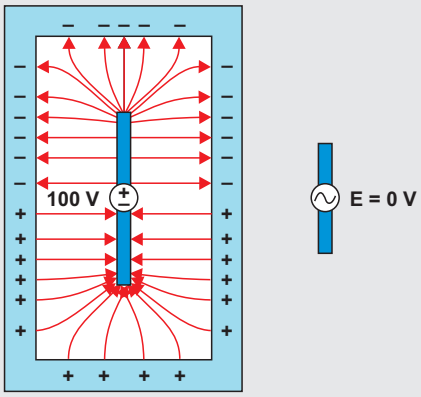
Don't shortcut good shielding techniques. When designing to minimize emissions, put a shield around the offending portion of the circuit. It may still emit energy, but good shielding can capture the emissions and send them to ground before they escape from the system. Figure 2 illustrates how shielding can control EMI.

Shielding can take a variety of forms. It might be as simple as enclosing a system in a conductive case, or it could involve fashioning small custom metal enclosures that are soldered over emission sources.

Figure 2. Example of shielding



(a) Typical EMI problem



(b) EMI controlled with shielding

5. Short ground connections

Every bit of current that flows into a chip flows back out again. Several tips in this article discuss having short connections to the chip—bypass capacitors close to the IC, keeping loops small, etc. However, often forgotten is the path that the ground current has to take to get back to its source. In an ideal situation, a layer of the board is dedicated to ground and the path to GND is not much longer than a via. However, some board layouts have cutouts in ground planes that can force ground currents to take a long path from the chip back to the power source. While the GND current is taking this path, it is acting as an antenna to transmit or receive noise.

6. No faster than needed

There is a tendency to worry about timing margins and to use the fastest logic possible to provide the best timing margins. Unfortunately, very fast logic has sharp edges with very high-frequency content that tends to produce EMI. One way to reduce the amount of system EMI is to use the slowest logic possible that will still meet timing requirements. Many FPGAs allow programming the drive strength at lower levels, which is one way to slow the edge rates. In some cases, series resistors on logic lines can be used to decrease the slew rates of signals in the system.

7. Supply line inductors

Tip #2 discussed bypass capacitors as a way to decrease the impact of current surges. Inductors on the supply lines are another side of the same coin. By placing an inductor or ferrite bead on a power-supply line, it forces the circuits connected to that supply to draw their dynamic power requirements from the bypass capacitors, rather than all the way back from the power source.

8. Caps at inputs to switching supplies

One recurring theme when looking to solve EMI issues is to reduce dv/dt and/or di/dt wherever possible. In this context, DC/DC converters may seem completely harmless until it is realized that they don't convert directly from DC to DC. Rather, they go from DC to AC to DC. Hence, the AC in the middle has the potential to cause EMI problems.

One area where automotive designers are concerned about creating interference is in the AM radio band. Most every automobile is equipped with an AM radio, which has a very sensitive, high-gain amplifier tunable from 500 kHz to 1.5 MHz. If a component is emitting a signal within this band, it will probably be audible on the AM radio. Many switching power supplies use switching frequencies within this same band, which leads to issues in automotive applications. As a result, most automotive-switching supplies use switching frequencies that are above this band—often at 2 MHz or higher. If there is insufficient filtering either at the input or the output of a switching power supply, some of this switching noise may find its way into other subsystems that may be sensitive to the root or subharmonic frequencies.

9. Watch for resonances

For various sources of interference, inductors and capacitors have been prescribed to tame the dv/dt and di/dt evils that can lead to EMI. However, inductors and/or capacitors can have undesirable characteristics related to self resonance. This problem can often be rectified by adding a resistor in parallel to the inductor to absorb the energy of the oscillation before it becomes big enough to cause issues. Another potential issue is when there is a series inductor, either a discrete component or a parasitic inductance from a power line, that leads to a component with a bypass capacitor. The resulting L-C circuit has the potential to oscillate at the resonant frequency. Once again, this can be tamed with a resistor, often placed in parallel with the inductor.

10. Spread-spectrum clocking reduces peak emissions

With components such as FPD-Link serializers and deserializers (SerDes), there is often a data bus and clock that have the option of spread-spectrum clocking. In spread-spectrum clocking, the clock signal is modulated. The result is that energy generated by the edges of the clock and data signals is spread across a wider frequency band than it would otherwise occupy. Since EMI specifications are set to limit peak emissions at any frequency within a band, spreading noise across a wider band can help to minimize the noise peaks .

A good example of a deserializer is the DS90UB914A-Q1, which is often used in conjunction with the DS90UB913A-Q1 serializer. These devices are used to provide a video link between a camera in an advanced driver assistance system (ADAS) and the processor. The deserializer recovers the clock that the image sensor in the camera provided to the serializer and outputs this clock along with the data for use by the processor. Ten or 12 high-speed data lines that transition concurrently with a high-speed clock are a prime source of EMI. To mitigate this EMI, the DS90UB914A has an option to use a spread-spectrum clock with the output data, rather than the lower-jitter clock that the image sensor provides. The spread-spectrum clock is controlled through registers in the deserializer.

Conclusion

As automobiles rely more on electronics for critical vehicle operation in addition to entertainment and comfort functions, there is a growing need to operate without error in the presence of interference and to not provide interference to other systems within the vehicle. By following the tips and techniques outlined in this article, and through selection of appropriate components, engineers are able to design robust systems that enable automotive systems to operate reliability without EMI problems.

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5. Howard W Johnson and Martin Graham, "High Speed Signal Propagation: Advanced Black Magic," Prentice Hall Professional, 2003

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Transient-testing platforms and automation techniques for LDOs and buck regulators

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Introduction

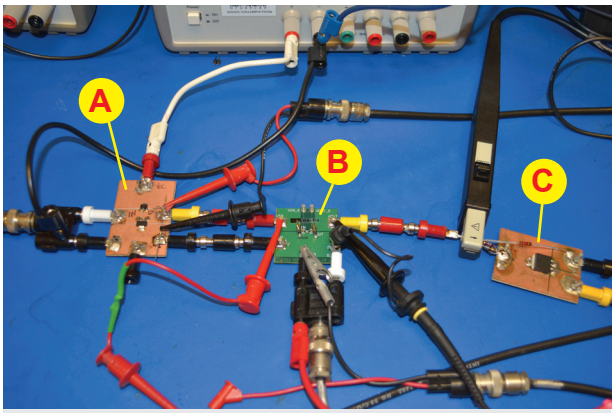
With mobile processors in wireless devices operating in the gigahertz range, there is increasing consumer demand for higher performance, longer battery life, smaller size, and lower cost. Therefore, the design of power management circuits is becoming an increasingly complex issue. Low dropout regulators (LDOs) and switching regulators are indispensable components in portable systems with standalone regulators and power management units (PMUs). As high-speed and portable communications devices employ regulators that require faster response time, it is necessary to rigorously validate regulator performance and merits in order to ensure reliable power management products. Key performance parameters include line transient, load transient, startup, load and line regulation, and several others. To have a complete analysis of these parameters, it is necessary to have state-of-the-art tools for the hardware test platform and mature methodology. These tools allow accurate and high sample rates for parameter characterization in addition to supporting automation techniques that speeds up testing and ensures repeatable results.

Implementing high-edge-rate and reusable test apparatus

For an accurate assessment of the key parameters of a regulator, it is necessary to generate steps in line voltage and load current that are fast with respect to the regulator's control-loop response time. Lab equipment and many commercial instruments that use operational amplifiers (op amps), passive components, and large driver chains can limit the rise and fall times of the stimulus signals with large excursions. To obtain high-speed edge rates for load transients (>> 1 A/µs) and line transients (>> 0.1 V/µs, with input caps), practically no off-the-shelf products are available.

It is possible for a slow-transient stimulus to make a poor regulator look good. In response, incremental research and development (R&D) led to simpler designs that are low in parasitic L and C, which can be readily built and duplicated for use in design and application labs. Setting up a respectable test jig is half the solution. To achieve optimal response, the device under test (DUT) must be properly wired or socketed onto the printed circuit board (PCB). Also important is proper selection of optimal ground and supply conduits, bypassing, charge reservoirs, and external support components. After all, it is the merits of the DUT that should be ascertained, not the parasitic or the unwanted effects from improper components and physical layout.

Figure 1. Antiquated setup for transient testing



A. Emitter followers and pulse generator create V_{IN} step voltage during line transient tests.

B. Device under test (DUT) is an LDO evaluation board (EVB).

C. PCB for NMOS transient load switch. A constant load is applied during line transient tests.

Preamble on test hardware challenges and limitations

In a load-transient test, the regulator's input is powered by a constant voltage source and the output is rapidly switched to a greater resistive load or current sink. A line-transient test is similar in that a line-voltage step is rapidly injected at the regulator input while its output is supported with a constant load. Figure 1 shows a typical test setup for transient testing. The setup is relatively modularized for ease of assembly and the long cable lengths were adequate for legacy technology. However, this setup is not satisfactory for today's requirement because of parasitics, ground loops, and higher voltages and currents.

Test-jig parasitics and automation

A transient-testing program for semi-automated testing was initiated in January of 2013 for PMUs and regulators. A universal regulator test bed was conceived and constructed to verify its merits. Figures 2 and 3 show an LDO regulator test jig that can accommodate an evaluation board (EVB) via machined socket pins for semi-automated testing. The schematic is shown in Figure 4.

Figure 2. Transient test jig with LDO EVB (blue PCB)

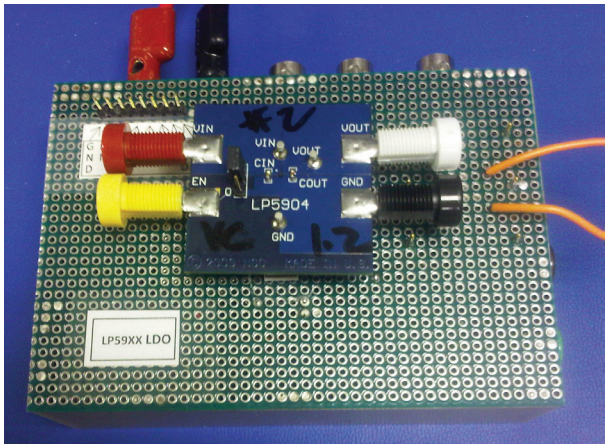
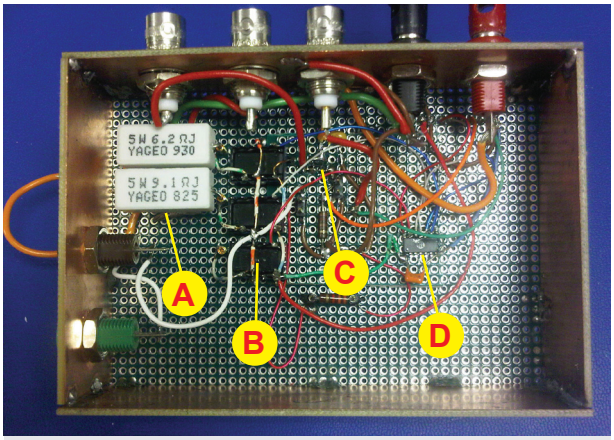
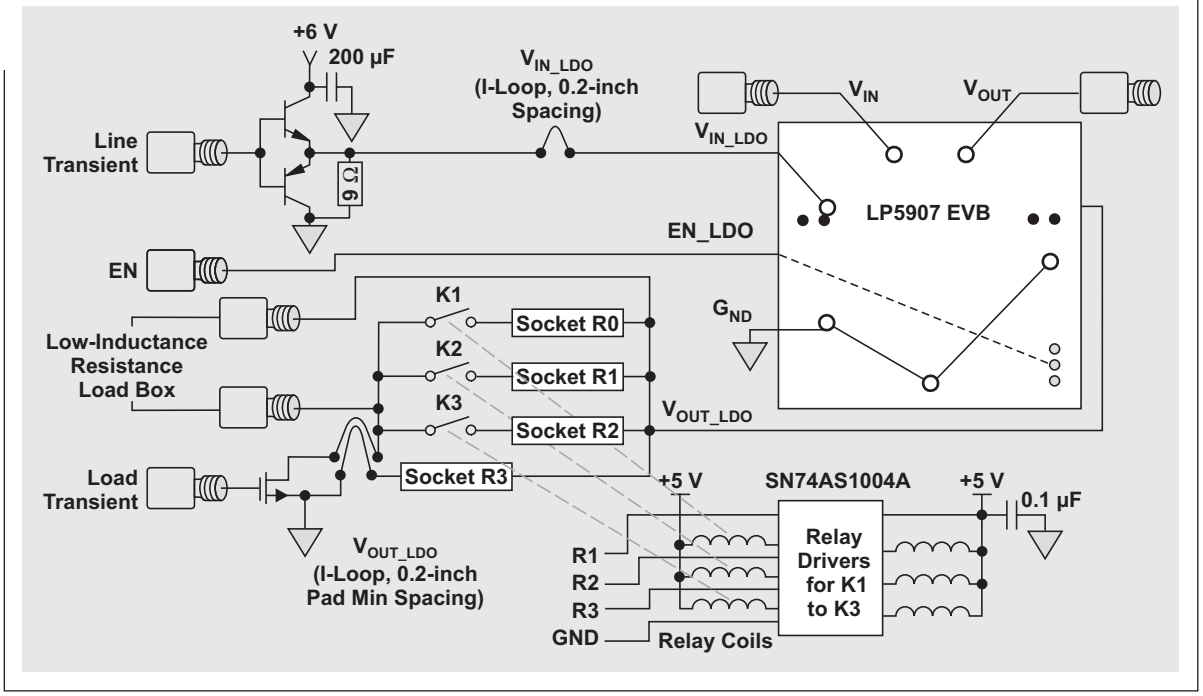


Figure 3. Back side of LDO test jig



A. NFET load step switch (under resistors).
B. Relays to select load.
C. NPN follower.
D. 48-mA relay drivers.

Figure 4. Schematic for the LDO test jig



Figures 5 through 7 show a similar transient test jig and schematic for a buck regulator.

Figure 5. Transient test jig and buck-regulator EVB (green PCB)

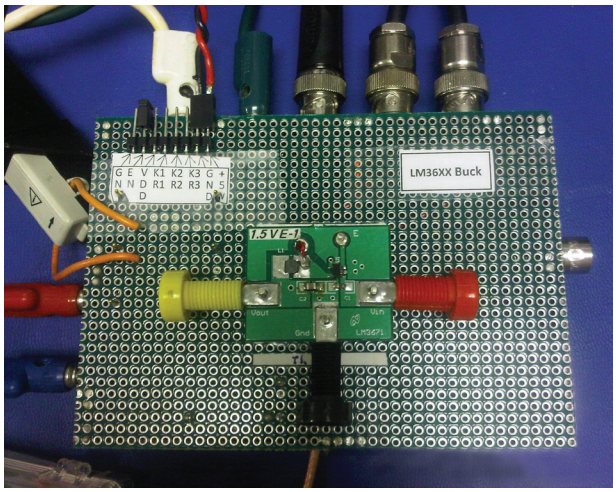
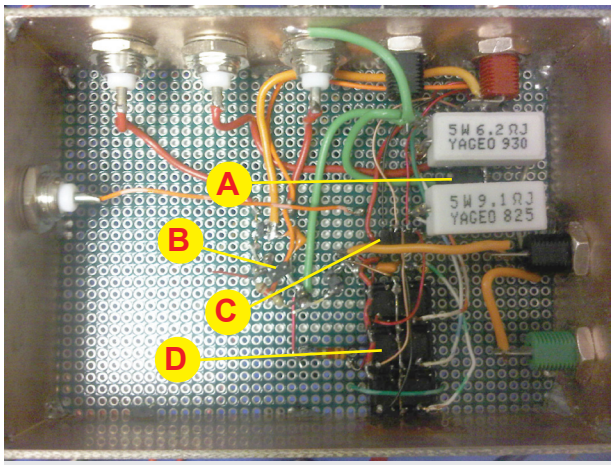
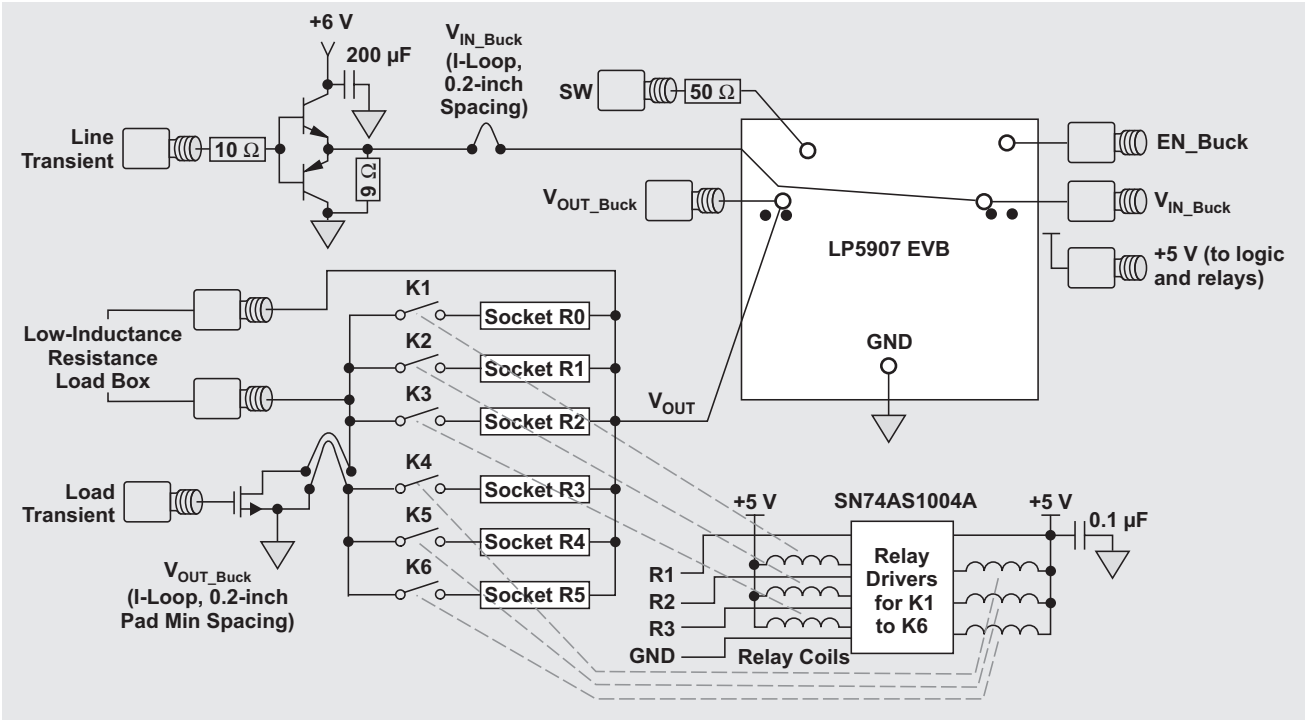


Figure 6. Back side of buck-regulator test jig



A. NFET load step switch (under resistors).
B. NPN follower for line step.
C. 48-mA relay drivers.
D. Relays to select load.

Figure 7. Schematic for the buck regulator test jig

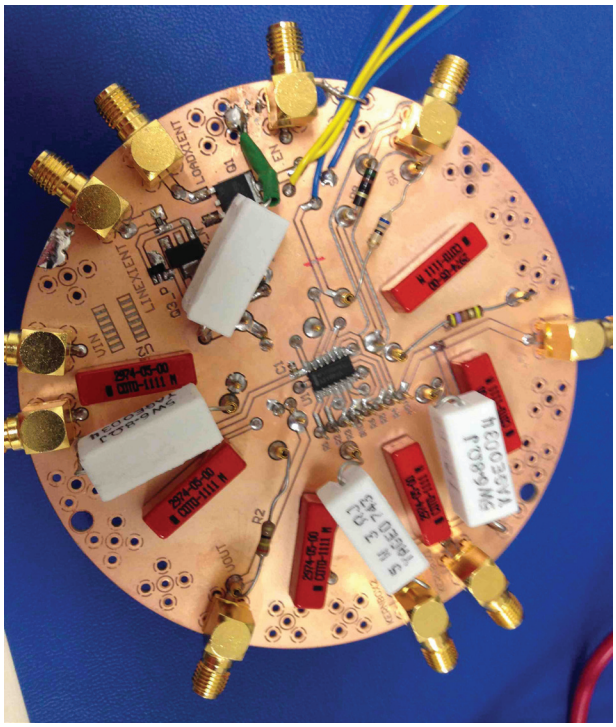


Further enhancements

The test jigs were successful in achieving the design goals in that they significantly reduced parasitics and current loops, thus enabling faster edge-rate stimulus for validating targeted products. In June of 2013, a follow-up enhanced design for a higher-performance, integrated transient test jig. This jig is capable of accommodating today's high-bandwidth and fast-edge-rate products and future generations.

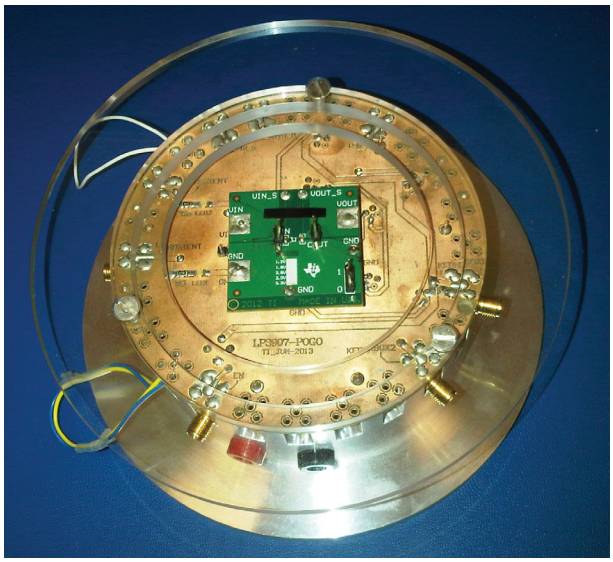
As shown in Figure 8, the enhanced jig was designed with a circular PCB configuration and can either adapt an EVB of a DUT for maximum flexibility. An alternate DUT layout is to solder it on the PCB for optimal performance. Radio frequency (RF) plumbing was used on the board and PCB traces were matched and impedance controlled. The jig also provides a rechargeable battery pack that provides clean and quiet power to the DUT for low-noise applications.

Figure 8. Enhanced test jig with resistive loads on board



For more extreme test requirements, the jig was redesigned to interface with temperature-cycling, air-stream systems that can be sealed air tight with no leakage, which will avoid icing at extreme temperatures. The result is the castle-shaped metal housing structure shown in Figure 9 that supports a personality card PCB for the EVB. An alternative could be a circular PCB with a direct on-board DUT mount. Also, a high-temperature transparent plastic adapter was included to interface to a temp-cycling housing.

Figure 9. Temperature-cycling test jig with personality PCB for PMUs

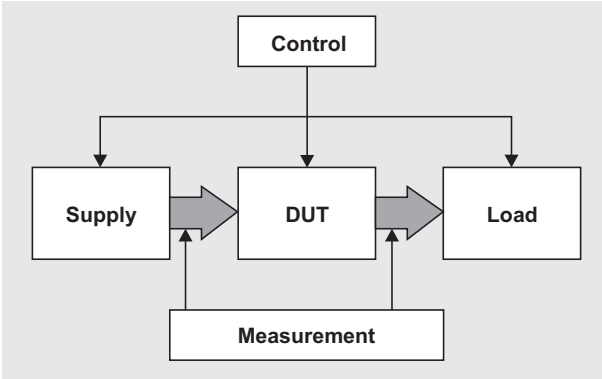


Architecture and automated test flow

A block diagram of the test environment for the automated test platform is shown in Figure 10.

The supply block provides all the voltage inputs and the line-transient input to the DUT. The load block provides multiple resistive loads that are controlled with relays. The control block is responsible for interfacing with the DUT and also for changing the supply and load settings. The measurement block is responsible for measuring the input and output voltages and currents.

Figure 10. Generic test environment



LDO test jig

Based on the jig schematic in Figure 4, the line-transient input is connected to a function generator to provide the line transient input to the LDO. Since the function generator cannot source a lot of current, an emitter follower is used to increase the current being sourced to the input. A 9-Ω resistor is connected at the output of the emitter follower circuit to provide fast discharge of the input capacitor during the fall time of the input line transient.

For tests that do not require a line transient, a constant DC voltage is provided through the line transient input, which is connected to the input of the LDO. The enable (EN) input is available to provide a pulse for the startup test using a function generator. In other test cases, the enable pin is supplied with a constant DC voltage for regular enable operation. The load-transient input is also controlled by a function generator that switches the NMOSFET continuously for a load-transient test. There is a base load (1-mA load for the LDO), which is always connected to the output of the LDO. However, it can be disconnected, if required. Three other resistive loads are controlled by using three relays. In turn, these relays are controlled via a computer through a USB relay controller.

Buck test jig

The system architecture of the buck-regulator test jig shown in Figure 7 is virtually the same as for the LDO jig. The only major change is the addition of three new relays. These were added because of the complicated nature of the load-transient tests for a buck IC. Unlike a LDO, load transients consist of different base current for load-transient testing. For example, for a LDO, the load transients required are 1 mA to 20 mA, 1 mA to 100 mA and 1 mA to 250 mA. However, for a buck, the various load-transient tests require 1 mA to 50 mA, 50 mA to 400 mA, 200 mA to 400 mA, and 0.6 A to 1 A. Hence, there are additional relays. The PCB design has some other changes. The buck is a switching regulator, thus, there is an additional switching pin to probe. This pin is isolated from other parts of the board by creating 20-mm segregation on both sides of this trace and pin. The tests for the buck test platform are exactly the same as for the LDO platform.

PCB design and issues

There are two major concerns on the layout of the redesigned automation test platform for high-performance validation. The first concern is maintaining high edge rates and signal integrity of the stimuli. The test setup is designed to produce fast line and load transients for the DUT. However, impedance mismatches and cross-talk between traces can significantly affect these high-speed lines. The second concern is voltage drops in power lines caused by attenuation from long traces. Hence, proper PCB design following good RF techniques is required. Also, it is necessary to measure a signal as close to its origin as possible to mitigate voltage drop or parasitic effects.

Lab equipment deployed

For line/load-transient and startup testing, the test platform includes a programmable power supply, three function generators, one oscilloscope, and a test jig. The power supply is used to provide power to the test circuitry required to carry out line- and load-transient testing. The power supply is also used to power the enable pin of the DUT and the relay driver chip, which allows the user to select different loads for a particular test. The function generators are used for generating pulse waveforms (using the arbitrary function waveform) for the line-transient step, load-transient step, and to pulse the enable pin.

The oscilloscope measures the input and output voltages and currents. The test platform is also used to observe the enable pin for the startup test. Designed as a plug-and-play test platform where the DUT needs to be installed on the test jig, this architecture methodology allows the reuse of the platform for different DUTs. The test setup relies on instruments that are controlled by a laptop running LabVIEW® software and connected via a general purpose interface bus (GPIB). All instruments, except for the oscilloscope, are daisy chained using GPIB cables that are connected to the laptop using a USB to GPIB cable. The oscilloscope is directly connected to the laptop with a USB cable. BNC to SMA cables are used to measure or probe all the signals.

LabVIEW tool (LVT) for test automation

Visual basic routines for virtual instruments (VIs) are written to automate the transient tests. These tests consist of three blocks. The first block of the LVT test selects the loads for the test. The second block includes the feedback correction loop that continuously measures the rise and fall times of the input-transient stimulus and corrects for the output of the function generator until the correct rise and fall times are measured by the oscilloscope. The third block of the LVT test captures a screenshot of the output and input voltage once the feedback is completed. It also obtains the measured rise and fall times and the maximum and minimum output voltages. The LVT obtains the minimum, maximum and mean of all the parameters directly from the scope. It also calculates the average of the maximum and minimum value measured. The LVT then populates a matrix of measurements and graphs that are displayed on the front panel. These measurements are also written to a text file in the Text Files folder. The screen shots are saved to a pen drive inserted into the oscilloscope. The name of these files are decided based on the kind of load and edge-rate setting. However, the names can be changed in the block diagram of the LVT.

Conclusion

The platform for automating high-speed transient testing is very multi-disciplinary because it requires capabilities beyond typical validation and test R&D. Included are a wide range of disciplines such as basic knowledge of startup-and-transient behavior characteristics for linear and switching regulators, best practices plus novel techniques for test and measurement, board-level system design, and software development.

With the prototyping test jigs for both LDO and buck ICs, the proposed test procedures can be validated and automated for line-transient, load-transient and startup tests. Stimulus edge rates can be achieved in the nanosecond range with proper drive, interfacing, and termination. High-speed waveform-capture sampling can be done with high-performance test equipment and probes. Serial-interface control of device modes, operation, and test equipment can be programmed on the fly to automate testing. Furthermore, closed-loop control and monitoring facilitates programming the timed events and electrical parametric stimuli in addition to accurately logging response time delays.

Acknowledgments

The author thanks Sheng Jin, Applications Manager MLP at Texas Instruments and Aditya Jain, our dedicated intern. Thanks also to Hoang Duong, Robin Gupta, and Hak-Leong Ng.

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Debugging power-supply startup issues

By Robert Taylor, *Applications Manager, Power Design Services, Analog Marketing*
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Introduction

You just received your assembled power supply printed circuit board (PCB) from the manufacturer. You plug it in and guess what? It doesn't work. Whether you are a novice engineer or an industry veteran, you know that sinking feeling. Regardless of how many days and hours you spend running the calculations, perfecting your design, and meticulously placing and routing your PCB, your 3.3-V output shows nothing but zeros on your multimeter or, worse yet, it goes up in a puff of smoke.

Gone are the days where power supplies use simple pulse-width modulators (PWMs) with limited bells and whistles. Integrated circuits (ICs) have dozens of pins and features like soft start, current limiting, pre-bias startup, and boot capacitors. But what do some of these features mean, and which ones are preventing your power supply from working?

This article provides a logical debug process for a malfunctioning design. The troubleshooting process starts with the simple "gotchas" and then tackles more difficult areas that even the experienced designer may find helpful.

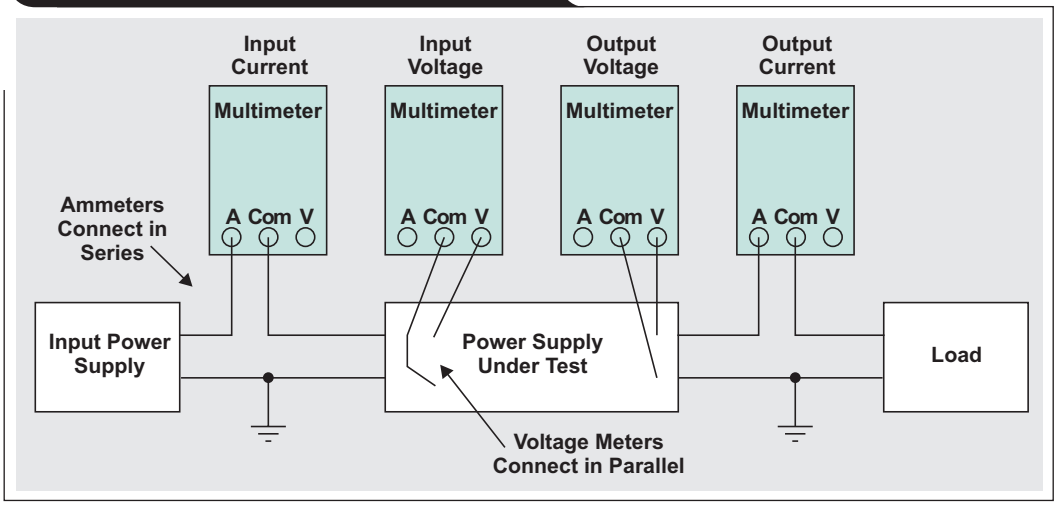
Check here first

The most obvious mistakes can be very time consuming when debugging a power-supply issue. Before powering up a supply for the first time, it is a good idea to do a visual inspection of the board. The designer needs to check that the correct parts are installed, check for missing parts, inspect all solder joints and verify that parts are soldered in the proper orientation. Double check to ensure that surface-mount resistors and capacitors were not swapped in assembly and that square ICs are not rotated 90 or 180 degrees. If you did not do a visual inspection and the board failed at turn on, this is good time to find and replace damaged parts, and to check the rest of the board.

Once the visual inspection and part replacement is complete, the next thing to check is that input cables are properly connected. Figure 1 shows a typical single-input, single-output, power-supply test setup.

After input connections are verified, the easiest way to get started on the debugging process is with a multimeter or oscilloscope. A multimeter can be used to ensure the input voltage is being passed to the PCB and arriving at the proper places on the board. If an ammeter is used to measure the input current, the meter could be connected incorrectly or have a blown fuse that would prevent the input voltage from getting to the board. When the power to the board is verified, measure the voltage across the capacitors located next to the IC. Some converters have AVIN and PVIN pins for the analog circuitry and power stage, respectively. Confirm that each of these nodes is receiving its designated voltage. Once you verify that the IC is receiving voltage, the next items to check are the on-board linear regulators or reference voltages. Check the datasheet to ensure the voltages on these pins are correct. Before spending too much time on the debugging process, this would be a good time to check another board. If other boards are working properly, that helps to

Figure 1. Typical power supply test setup



narrow the problem from a design issue to an assembly or PCB issue.

Power supply ICs usually have input-enable or undervoltage lockout (UVLO) circuits. An oscilloscope is useful for checking these voltage levels. Probe the input-voltage and enable pins to observe if each crosses the startup thresholds specified by the IC datasheet. Some converters need a 5-V or 3.3-V bias before the input is applied and enable is toggled. Verify that the bias is present in the correct timing sequence.

Detailed debug procedures

After verifying that the IC is receiving the right voltages on the input and enable pins, the next step is to detect if the IC tries to start. Although your multimeter reads 0.0 V on the output, the device may have started switching before shutting down. Place scope probes on the switch node, input voltage, output voltage, and enable pin. Set the oscilloscope to a normal trigger on the switch node and zoom the x-axis to ~1-ms/div. Apply power to the board and observe if the oscilloscope triggers. If the trigger catches and waveforms appear, the IC has made an attempt to charge the output. The supply could be shutting down from a short circuit. Remove power from the input and measure the impedance from the output to ground (GND). If it is a short or abnormally low impedance, the cause needs to be determined.

Lifting the inductor can help isolate the output node from the IC. If the short is on the output, it could be shorted output capacitors. If the short is on the IC side of the inductor, it could be a number of issues. The first step to isolate the short is to begin removing parts on the shorted node. If this is not successful, a power supply and thermal camera can be used to find the location of the short. Current limit the power supply to a few amperes and apply power across the shorted terminals. Be careful not to exceed the voltage ratings of any components on this node. Then use the thermal camera to observe where the board is heating up. Inspect with a microscope to pinpoint the problem.

If the power supply makes no attempt to switch, verify that the semiconductors are installed properly and are not damaged. Check the MOSFET impedances. The gate-to-source and drain-to-source impedances should both be high. Then use the diode measuring tool on a multimeter to measure the body diode of all MOSFETs. The source-to-drain body-diode voltages of the MOSFETs should be in the 0.3- to 1-V range. If these terminals are shorted, the device is blown and must be replaced. Check the forward voltage of any other diodes in the circuit for proper orientation.

Soft-start circuits can be used to control the ramp of the power-supply output. This is typically a current source feeding a capacitor. If the capacitor is shorted or intentionally held low, this will prevent the device from switching.

In some cases the power supply boots up and attempts to regulate. It is important to know the protection features inside the power controller. These can include overvoltage protection (OVP), undervoltage protection (UVP), overcurrent protection (OCP), undervoltage lockout (UVLO), and overtemperature protection (OTP).

If the power supply switches and the output voltage ramps and overshoots, the controller could latch off due to OVP. Check the top feedback resistor to verify that it is installed properly. UVP can occur if the output voltage does not ramp in time. This can happen in an overcurrent situation during startup, or if the supply voltage is lower than the output voltage set point during startup. If the power supply is reaching an overcurrent condition, it may not trip UVP. However, it could have another method of protection. These protections include voltage foldback, hiccup mode, or latching the device off.

Another issue could be that the output capacitance is too large and the converter cannot charge the output before the soft-start time runs out. In this case, a larger soft-start capacitor could help to solve the problem. Most ICs have overtemperature protection to prevent the device from thermal runaway. Use a thermal camera to diagnose this failure as the temperatures can rise well above 100°C. ICs may attempt to restart once cooled, providing a failure signature.

Table 1. Troubleshooting list for power-supply startup issues

Step	Issue	Symptom	Solution
Prior to hooking up any cables, visual inspection			• Check BOM and SCH vs. board • Ensure jumpers and 0-Ohm resistors are installed • Ensure that DNP parts are not present • Inspect all solder joints
Hooking up the cables			• Ensure all cables are wired correctly • Ensure ammeters are wired in series! • Ensure cables are big enough to handle the current
Applying power	Smoke		• Not good, fix bad parts, use current limit when starting. Check multiple boards
	No startup	No voltage to the IC	• Check input cables • Check multimeter fuses • Check on board fuses • Check the path from the source to the IC
		Check EN, VREG, VREF	• Check the enable voltage, UVLO, soft-start voltage, internal regulators, and internal references. Change ICs that are not correct
		No switching	• Check the MOSFETs for shorts • Check the body diodes of the MOSFETs • Check other diodes for proper orientation
		Brief switching	• Check the output for shorts • Lift the inductor to help isolate • Use thermal camera to help identify issues
	Startup immediate Shut down		• Check for OCP, OVP, UVP • Lift the inductor and add a current loop • Check feedback paths to ensure connectivity • Isolate any external loads on the board • Check to ensure soft start is completing, a larger cap may be required

Table 1 shows a top-level check list for troubleshooting common startup problems. This list applies to the typical switching supply, however, some supply topologies may require more extensive troubleshooting.

Conclusion

Power supplies are complex circuits, so care must be taken with design, layout, fabrication and assembly. The debug process when things are not perfect is an art in itself. Following the tips and process described here could help the designer find a remedy in an efficient and timely manner. Texas Instruments has an archive of over 1,000 built and tested power supply designs.[1] All of these designs have schematics, test reports and Gerbers available.

References

1. TI reference-design library for power management devices.

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Ceramic or electrolytic output capacitors in DC/DC converters—Why not both?

By Michael Score
Senior Member Technical Staff, Field Applications Engineering

Introduction

Switching power supplies are used in almost every end-equipment that needs a long battery life, low heat generation, or to meet ENERGY STAR® guidelines. When designing a switching power supply, it is difficult to decide which output capacitor type to use.

Electrolytic capacitors have high equivalent series resistance (ESR), making power loss high and transient response too poor for use with tough load-response requirements. However, electrolytic capacitors have stable capacitance with high bias voltage and are inexpensive.

Ceramic capacitors have very low ESR, but capacitance is reduced greatly with high bias voltage and can be expensive for large values. The effective capacitance of a ceramic capacitor can be less than half the rated capacitance in many buck converters.

Today's buck regulators typically use just one type of output capacitor because it becomes too difficult to design with different capacitances and ESRs. This forces many designers to use more expensive capacitor types like polymer or tantalum that provide lower ESR than electrolytic, but not as low as ceramic. Now a stable design with mixed output capacitors can be prepared in minutes by using new design tools. To illustrate this concept, this article describes the design of a DC/DC supply with mixed output capacitors.

Causes of output variation under load

The first step is to understand what the output capacitor does in the system. Figure 1 shows idealized waveforms with contributions of output-capacitor characteristics and where they occur in a load-transient event.

The spikes at the load transients are primarily caused by equivalent series inductance (ESL) or impedance of the output cap at very high frequencies. Fixed inductor-current slopes cause the bulk of the transient-event disturbance in the inductor current to overshoot and undershoot.[1] Recovery from the load-step transient also causes overshoot and undershoot. Minimizing these lower frequency errors relies on energy stored in the output capacitor and the voltage-loop response time. So, it is important to have a wide loop bandwidth, low ESR, and enough output capacitance for adequate storage.

There are two primary factors for maintaining low-noise output under load: 1) how much overshoot and undershoot the regulator will have; and 2) how much ripple voltage occurs at the switching frequency. Peak overshoot/undershoot is approximately the load-step current times the impedance of output capacitors at the loop crossover frequency (Equation 1). The equation emphasizes the importance of having low output-capacitor impedance at the loop crossover frequency (f_C) to get low overshoot or undershoot. The loop crossover frequency is usually targeted to be one-tenth the switching frequency. A higher loop crossover frequency minimizes overshoot/undershoot.

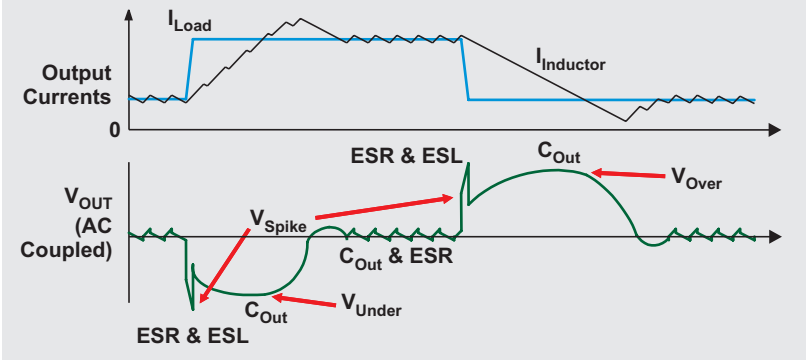
$$V_{OVER/UNDER\ SHOOT} \approx \Delta I_{OUT} \times Z_{OUT}(f_C) \quad (1)$$

An approximation for output ripple voltage is the output capacitor's impedance at the switching frequency times the peak-to-peak inductor current.[2]

$$V_{RIPPLE} \approx I_{L(P-P)} \times Z_{OUT}(f_{SW}) \quad (2)$$

Equation 2 shows that the output ripple voltage can be reduced by reducing the peak-to-peak inductor current, which is controlled by increasing the inductance value.

Figure 1. An idealized load-transient plot



However, there are drawbacks. A more effective way to minimize ripple is to reduce the output capacitor's impedance at the switching frequency. The impedance used for ripple voltage is at a much higher frequency because the switching frequency is around ten times the loop crossover frequency.

To minimize ripple and overshoot voltage under load transients, the regulator requires a wide loop-crossover frequency. There should also be sufficient capacitance for energy storage and the impedance of the output capacitors should be low over frequency.

Output capacitors minimize output impedance

Ideally, the output capacitor would be very large for energy storage and have very low impedance at the loop crossover and switching frequencies. Polymer and tantalum capacitors come in large values with low ESR, but they are expensive and the ESR is still not as low as a ceramic capacitor. Electrolytic capacitors are very good for obtaining large capacitance values at a low cost, however, they have a larger ESR and ESL. This makes them unsuitable for output load-step performance.

Ceramic capacitors have very low ESR and ESL that makes them great for transient performance, but they have limitations on capacitor size. Ceramic capacitor values of 22 µF and less are relatively inexpensive. The effective capacitance of ceramic capacitors decreases with bias voltage, which makes it more difficult to provide enough energy storage for large load steps. TDK SEAT software was used for the plot in Figure 2 to show the effect of V_{BIAS} on effective capacitance. The two 22-µF-rated ceramic capacitors decrease to 19 µF and 16 µF with 12 V of bias voltage. Note that two 22-µF, 25-V, X7R capacitors from the same vendor have very different V_{BIAS} curves, so be sure to check the actual V_{BIAS} curve.

With the same software, Figure 3 shows the impedance of 22-µF and 47-nF ceramic capacitors versus frequency. The 22-µF capacitor has low impedance at 100 kHz and above, but it does not provide enough energy storage. The electrolytic capacitor can be paralleled with the 22-µF ceramic, allowing low impedance at frequencies less than 100 kHz. The electrolytic capacitor is desirable at low frequencies because it has large capacitance and adding a small ceramic capacitor in parallel will reduce electromagnetic interference (EMI) that results from switching noise.

A 47-nF ceramic was chosen because it has a lower impedance than the 22-µF capacitor at 20 MHz and above. The 47 nF of additional capacitance is too small to affect stability. The black curve shows the impedance of the parallel combination of the 22-µF and 47-nF capacitors. Figure 3 shows the 22-µF ceramic as the dominant curve for the impedance through most of the frequency band. However, the electrolytic dominates at low frequencies and the 47-nF ceramic dominates at very high frequencies.

Figure 2. Effective capacitance of different 22-µF, 25-V, X7R ceramic capacitors

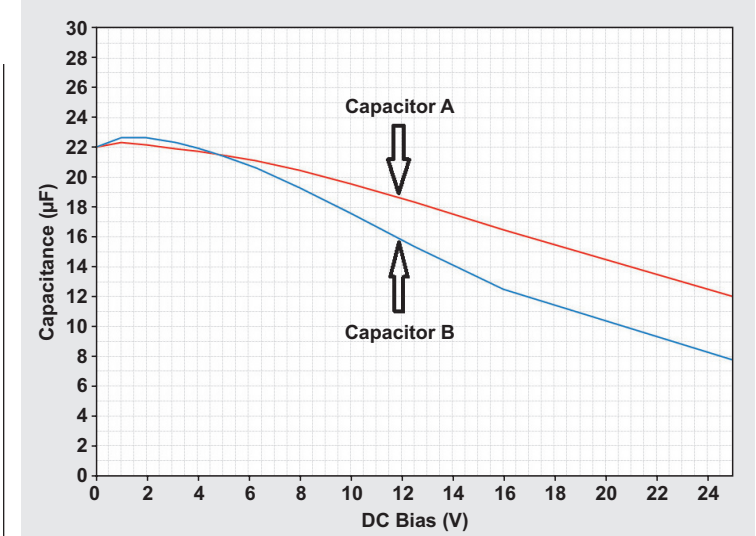
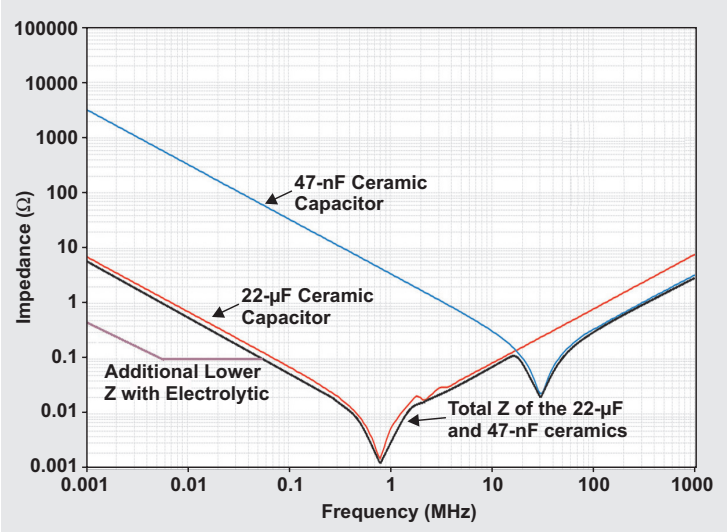


Figure 3. Impedance of ceramic and electrolytic capacitors



A design with mixed output capacitors provides the lowest output impedance across the widest frequency range. However, compensation of the feedback loop for a buck regulator becomes very difficult to calculate. It is important to consider the pole/zero locations because of the combination of lower ESR and capacitance from the ceramics, and higher ESR and capacitance from the electrolytics. The inductor and each capacitor provide different pole/zero locations. TI's WEBENCH® software takes each path into account separately, which makes the design easier and more robust than calculating by hand.

Mixed-capacitor design example

A mixed-capacitor design was chosen with a buck regulator having an input voltage of 24 V (±20%) and a 12-V output voltage at 6 A. The focus is on obtaining a good transient response with a low-cost solution.

You can enter the requirements either in the WEBENCH panel or directly into the panel on the product page of the chosen regulator. For this example, the LM25117 buck controller was chosen and the input conditions were entered on the product page. After the design is started, an advanced-option section will appear on the left side as shown in Figure 4. This design needs good transient performance, so the "user preferred frequency" box was checked and "500 kHz" was entered in the box below to allow a wide loop-crossover frequency. Under the "Output Cap Options," "Mixed" was selected and then "Update" was clicked to start a new design that allows 500 kHz and mixed output capacitors. These selections are circled in red in Figure 4.

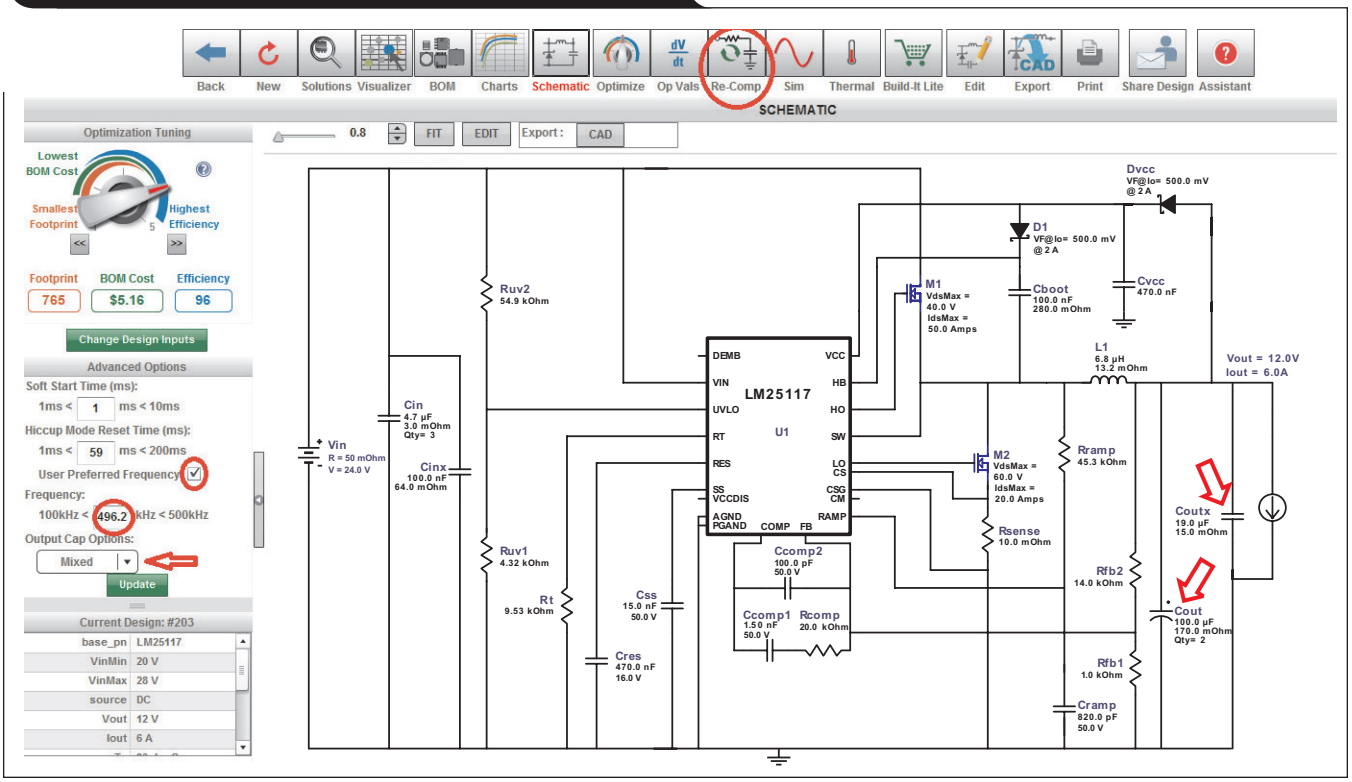
After clicking the schematic to enlarge the view, the components on the schematic can be changed by double-clicking on the component. In this case, the inductor (L1) was double-clicked to choose a slightly lower cost option. Each output capacitor (red arrows in Figure 4) was changed for the desired mix of electrolytic and ceramic capacitors. C_{OUT} was changed to two 100-µF electrolytic capacitors from the tool's database and C_{OUTX} to a ceramic capacitor. The database has several suitable ceramic capacitors. However, the tool did not have the 22-µF ceramic capacitor shown in Figures 2 and 3. The C_{OUTX} capacitor was double-clicked and then "Create Custom Part" (bottom of window) was selected. A 19-µF ceramic was substituted for the 22-µF typical value to adjust for reduced capacitance at the 12-V bias voltage and 15 mΩ was entered for ESR, which adds a little resistance for traces.

After changing the output capacitors, the "Re-Comp" button (Figure 4, circled in red) was clicked to see the bode plot and change the compensation.

On the following page, the blue curves in Figure 5 show the total loop magnitude and phase, while the orange curves show the power stage response. The tool marks the pole and zero locations of the power stage with the mixed output-capacitor design and the power-stage gain curve.

Stability of the selected design is sufficient, but the goal was to get a wider crossover frequency. The WEBENCH Compensation Designer allows auto compensation with the option to select a cross-over frequency, gain margin, and phase-margin ranges. In this example, however,

Figure 4. Schematic with mixed output capacitors



manual compensation was selected for control of the compensation poles and zeroes instead. The "Edit Poles/Zeroes" option allowed the compensation poles and zeroes to be moved and component values automatically changed to meet the pole/zero locations. "Zero1" was decreased from 5.3 kHz to 2.8 kHz to increase the crossover frequency and remove some of the dip in phase at 1 kHz. Pole1 was acceptable to stay near its original frequency of 80 kHz.

Moving the compensation zero to 2.8 kHz increased the crossover frequency from 21 kHz to 56 kHz. Phase margin was reduced to 65 degrees and the gain margin to 15 dB, which is still a very stable design. The stability results are circled in Figure 6. Selecting the "Apply Changes to Design" button updates the schematic.

Figure 5. An initial bode plot with mixed output capacitors showing poles and zeros on the power stage magnitude curve

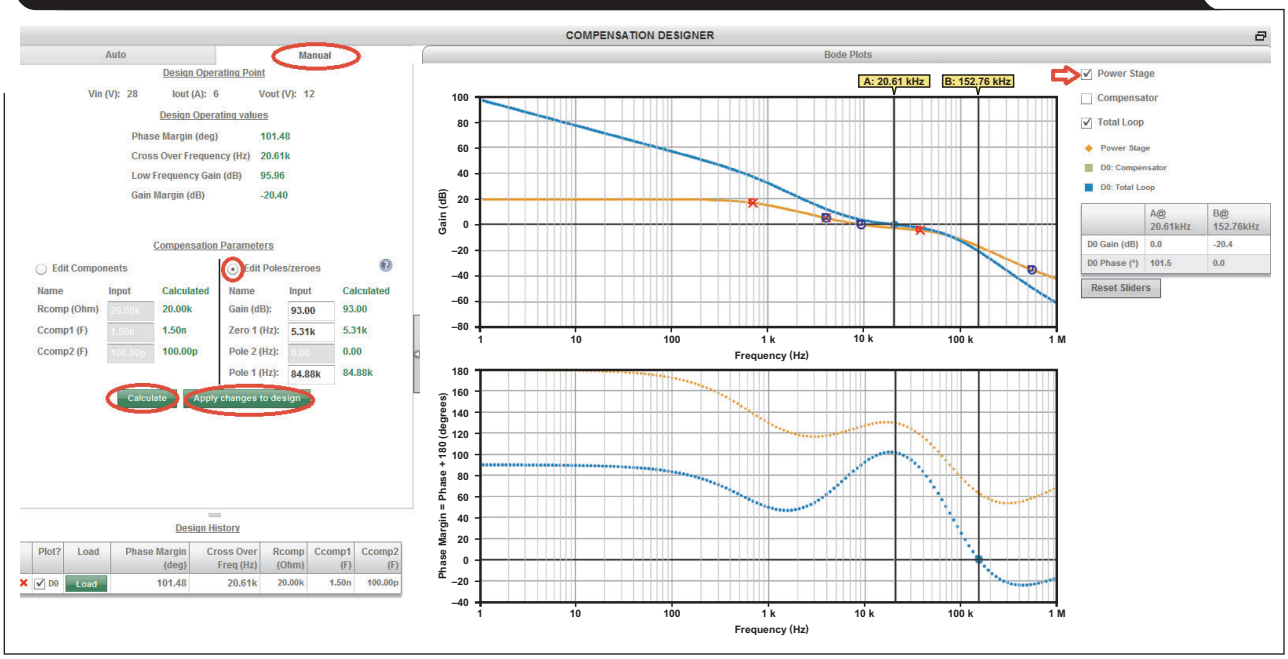


Figure 6. Bode plot with mixed output capacitors after manual compensation shows increased bandwidth and good phase margin

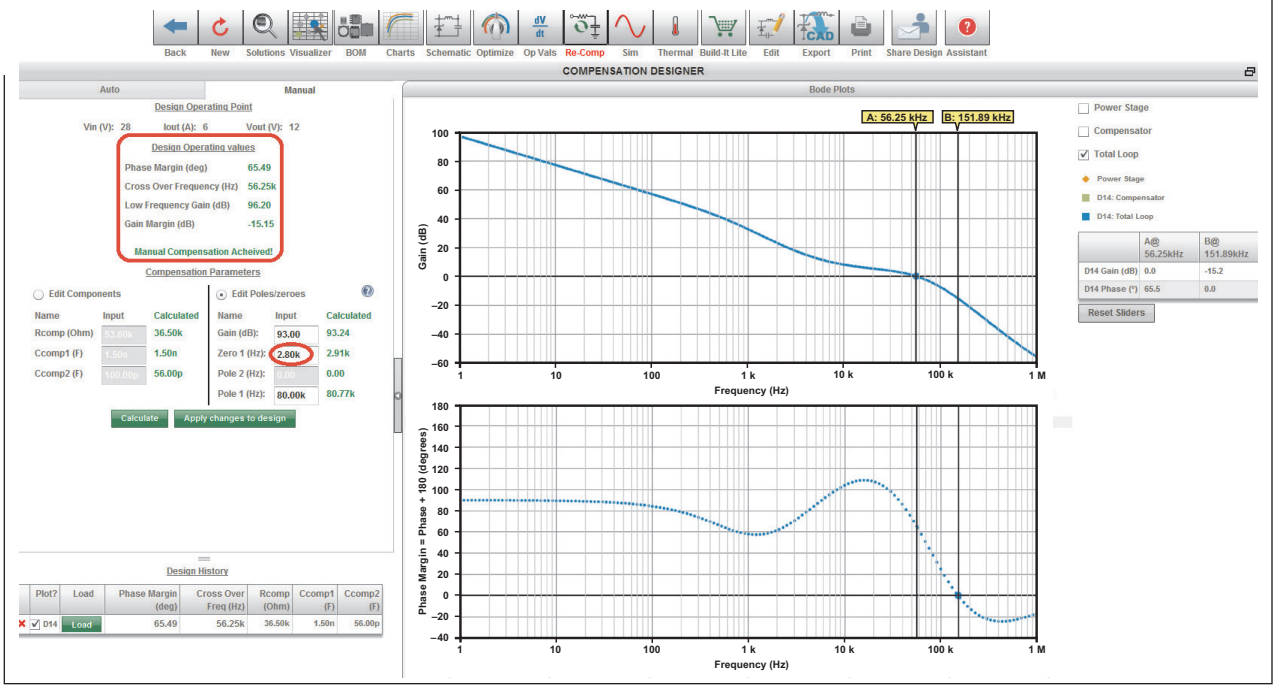
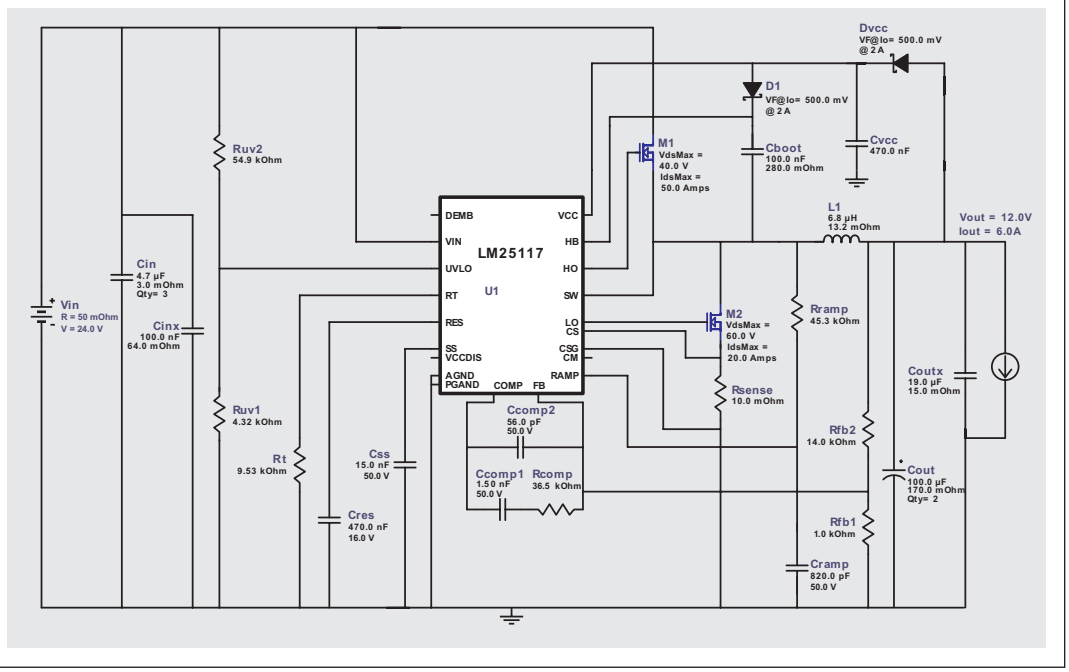


Figure 7. Final WEBENCH schematic with mixed output capacitors



The final schematic is shown in Figure 7. If the system does not already have bulk decoupling, an electrolytic should be added to the input for additional bulk capacitance. If needed, the 47-nF capacitor shown in Figure 3 could be added to the output to reduce EMI.

Conclusion

Low impedance of output capacitors across frequency and a high loop-crossover frequency provide good transient response. Using both ceramic and electrolytic output capacitors minimizes capacitor impedance across frequency. Ceramic capacitors are best for high frequency and large-value electrolytic capacitors are good for low frequency. Completing a stable design with mixed output capacitors using a pen and paper is challenging, but WEBENCH Power Designer makes it easy to design with mixed capacitors and also re-compensate for improved performance.

References

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2. Surinder P Singh, "Output Ripple Voltage for Buck Switching Regulators," Application Note (SLVA630A), Texas Instruments, October 2014

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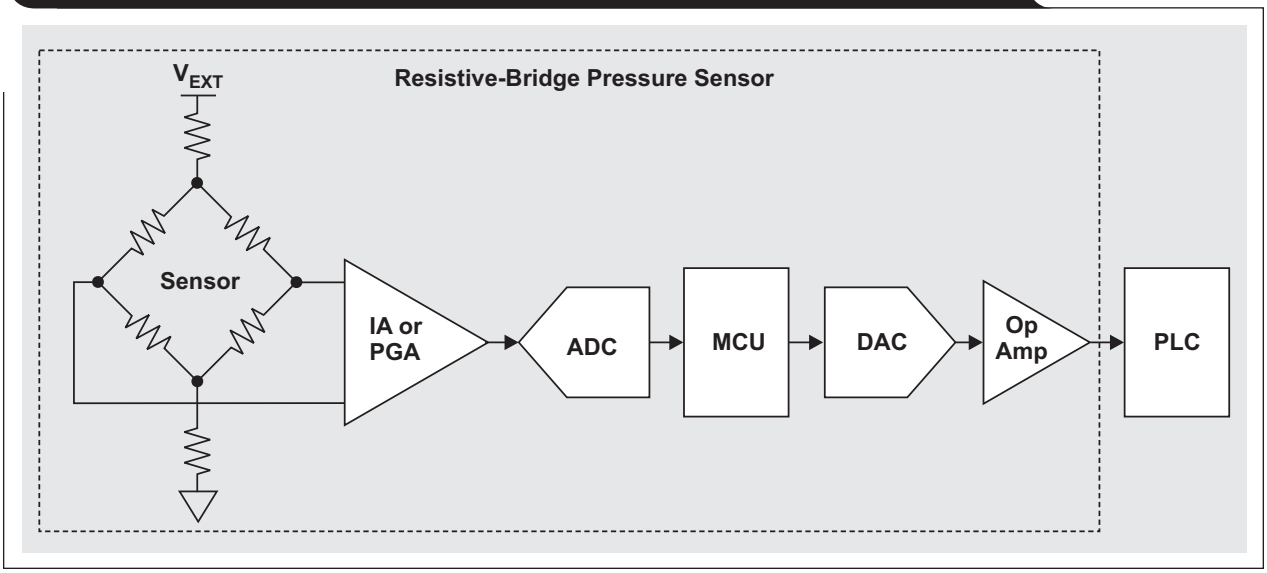
Design tips for a resistive-bridge pressure sensor in industrial process-control systems

By Peter Semig, *Application Engineer, Precision Analog*
Collin Wells, *Application Engineer, Precision Analog*
Miro Oljaca, *Senior Application Engineer, Medical, High Reliability and Sensing*

Figure 1. Resistive-bridge pressure sensor connection to process-control system



Introduction

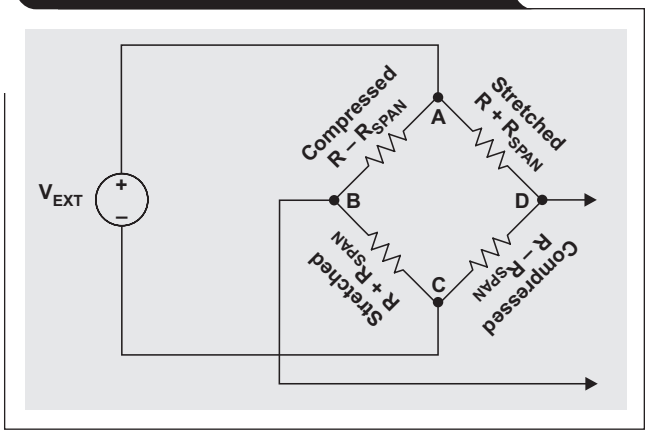
There are many physical parameters that need to be measured and controlled in industrial automation systems. Temperature, pressure, flow, and level are just a few of these physical parameters. Resistive-bridge sensors are commonly used in these applications. Figure 1 shows a typical diagram of a resistive-bridge pressure sensor in a process-control system. This article presents the primary design considerations for each block of the resistive-bridge pressure sensor.

Sensor basics

Industrial process-control systems commonly use resistive-bridge sensors to measure changes in resistance, which ultimately represent changes in physical parameters such as strain, pressure, temperature, humidity, and so on. There are numerous resistive-bridge topologies, but the Wheatstone bridge (Figure 2) is the most widely known and documented.

Each resistor in the pressure sensor either compresses or stretches (Figure 2). When pressure is applied to the sensor, the resistances of R_{AB} and R_{CD} decrease via compression while R_{AD} and R_{BC} increase by stretching. These changes in resistance yield a change in the differential voltage, V_{BD}, which is amplified by a differential amplifier (Figure 1). Designers often use differential amplifiers with very large input impedance, such as instrumentation amplifiers (IAs) and programmable gain amplifiers (PGAs) when interfacing with bridge sensors.

Figure 2. Resistive-bridge sensor with pressure applied



Common-mode voltage versus output voltage range

The bridge's common-mode voltage (V_{CM}) is the average voltage present at the differential amplifier's input terminals.

$$V_{CM} = \frac{V_{BC} + V_{DC}}{2} \quad (1)$$

If the bridge is balanced, V_{CM} is half of the bridge excitation voltage, $V_{EXT} = V_{AC}$. For example, if V_{AC} = 5 V, then V_{CM} = 2.5 V. The common-mode voltage of the bridge is perhaps the most important design consideration for resistive-bridge sensors. This is because the output voltage range (V_{OUT}) of an IA depends on many factors, including common-mode voltage, gain, reference voltage, topology, and supply voltage.[1] As an example, Figure 3 shows a V_{CM} versus V_{OUT} plot of an IA with three operational amplifiers (op amps).

Recall that V_{AC} = 5 V, then V_{CM} = 2.5 V. For unidirectional sensors, it is often desirable to power the IA with a single 5-V supply with V_{REF} connected to 0 V (GND). Unfortunately, this will limit the output swing of the IA. Using the INA826 as an example, notice in Figure 3 that if V_{CM} = 2.5 V, the output can only swing from 100 mV to approximately 3.2 V. As a result, the system cannot use the maximum resolution of the analog-to-digital converter (ADC) with a 5-V reference voltage. In this case, consider an alternate IA, select a different supply voltage and/or a different IA reference voltage, or modify the bridge common-mode voltage as shown in Figure 4.

Initial input offset voltage (V_{OS})

The input offset voltage is the DC error voltage between the differential amplifier's input terminals (for example, op amp, IA, PGA, and so on). For a traditional IA with three op amps, this voltage depends on the device's gain.[2] The offset voltage contributes to the solution's overall offset error and if not calibrated, it also shifts the common-mode voltage. Therefore, a better choice may be a zero-drift IA or PGA (for example, a PGA900) which has a very low offset voltage.

Zero-drift is a term that applies to a chopper or devices with auto-zero topology that will internally correct for offset errors, such as initial input offset voltage, input offset voltage drift, power supply rejection ratio (PSRR), common-mode rejection ratio (CMRR), and some others.

Input offset voltage drift ($\Delta V_{OS}/\Delta T$)

Input offset-voltage drift is the change in input offset voltage as the temperature deviates from room temperature (25°C). This offset error is in addition to the initial input offset voltage. Since most industrial systems must maintain accuracy over a wide temperature range, zero-drift IAs or PGAs are preferred. While the initial input offset voltage can be removed with a room temperature calibration, the offset-voltage drift requires a more complicated and time consuming over-temperature calibration routine. Each individual system must be calibrated at various temperatures because each system component may drift in different directions. In some cases the error over temperature may actually increase if the system is calibrated at 25°C without calibration at other temperatures.[3]

Figure 3. A V_{CM} versus V_{OUT} plot for the INA826 IA

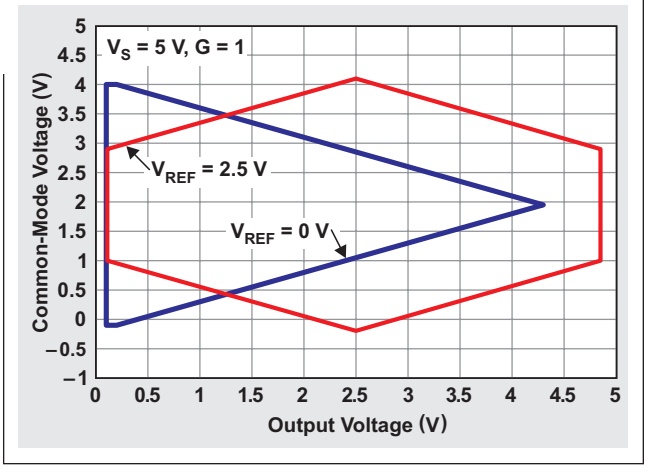
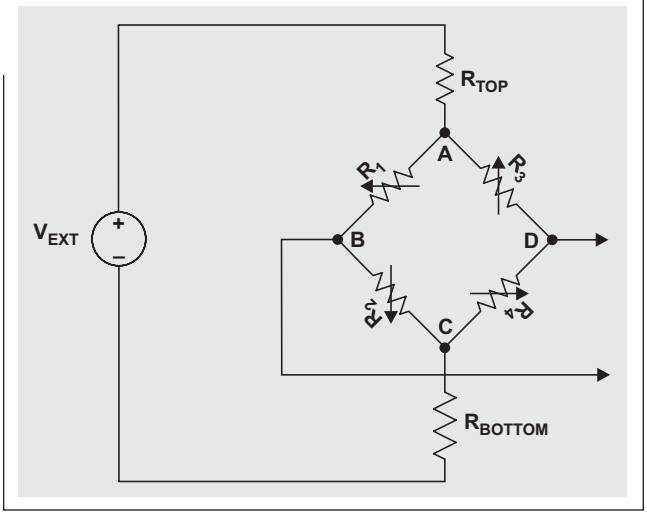


Figure 4. Adjust V_{CM} by adding R_{TOP} and/or R_{BOTTOM}



Noise

An amplifier's intrinsic noise is a primary concern when selecting the bridge amplifier. Of particular interest is the amplifier's low-frequency, or 1/f, noise because industrial systems are typically low-bandwidth. Noise generated by the amplifier sums with the noise of the ADC, which ultimately reduces the measurement's noise-fee resolution. While zero-drift amplifiers may be preferred because the 1/f region of their noise spectral-density curve is flat, some non-zero-drift IAs may have better overall noise performance. Conduct a complete noise analysis to determine the amplifier's total noise contribution.

Analog-to-digital converter

High-resolution (24 bit) delta-sigma analog-to-digital converters (delta-sigma ADCs) can be used to measure resistive-bridge signals. Generally, these ADCs include a modulator and digital filter. The total quantization energy is very high for the delta-sigma modulator because the number of bits-per-sample is extremely low. The decimator must filter unwanted noise in the spectrum above the Nyquist band so that the noise is not aliased into the baseband by the decimation process.

The decimator filter implemented in most delta-sigma ADCs is a Sinc filter. This filter topology is popular because it is inherently stable and simple to implement. The order and decimation ratio of this sinc filter determine the performance of the ADC.[4]

The ADC's noise-free code resolution is defined as the number of bits of resolution beyond which it is impossible to resolve individual codes. The noise-free resolution of the ADC can be calculated based on the total number of codes (2^N) and the peak-to-peak noise code measurement.

$$\text{Noise-free code resolution} = \log_2\left(\frac{2^N}{\text{Peak-to-peak noise codes}}\right) \quad (2)$$

Effective resolution can be calculated by adding $\log_2$ (6.6), or approximately 2.7 bits to the calculated noise-free code resolution.

$$\text{Effective resolution} = \text{Noise-free code resolution} + 2.7 \text{ bits} \quad (3)$$

For example, the delta-sigma ADC in the PGA900 has a second-order modulator operating at a sampling frequency of 1 MHz, and a third-order Sinc filter with 128 oversamples. The noise performance shown in Figure 5 is for an output data rate of 7.8 kHz with a bandwidth of 3.9 kHz, and a step response of 384 µs.

Applying additional digital filtering

It is common for the ADCs in this application to have data rates that are much higher than the required system bandwidth. Therefore, additional digital filtering can be applied to further reduce the ADC noise and therefore increase the noise-free resolution at the expense of the output data rate.

A simple averaging filter creates a low-pass filter that will lower the in-band noise by 3 dB and increase the measurement resolution by a half-bit for each two consecutive samples that are averaged. This is defined in Equation 4 where M is the number of consecutive samples averaged and W is the increase in output signal resolution.

$$W = \frac{1}{2}\log_2(M) \quad (4)$$

From Figure 5, a gain of 40 dB results in a noise-free output resolution of 13.84 bits. Applying a moving-average filter with M = 32 to the ADC output data should improve

Figure 5. Measured performance versus gain at output data rate of 7.813 kHz

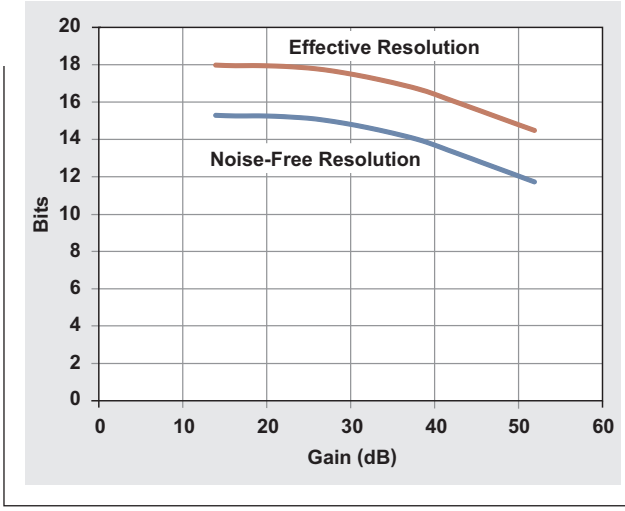
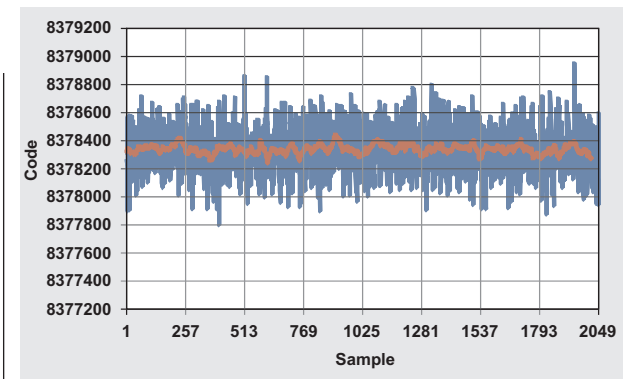


Figure 6. ADC output versus filter output



the noise-free output resolution by 2.5 bits as shown in Equation 5 and Figure 6.

$$W = \frac{1}{2}\log_2(32) = 2.5 \text{ bits} \quad (5)$$

Now the output noise-free resolution has increased from 13.84 to 16.34 bits. However, the data rate of the output signal decreases from 7.8 kHz to 244 Hz.

Analog output stage

Once the sensor signal has been acquired and processed, the next step is to create a linear analog-output signal that represents the sensor measurement from zero- to full-scale. The linear sensor output is transmitted over a 2-wire current loop or a 3-wire voltage output signal, depending on sensor transmitter requirements. The most common output range of a 2-wire sensor transmitter is 4 to 20 mA, although other output spans are occasionally

used. The most common 3-wire voltage output range is 0 to 10 V, but other output ranges can be implemented such as ±10 V, 0 to 5 V, and ±5 V.

The two main building blocks of the analog output stage are a digital-to-analog converter (DAC) and an op amp circuit configured to create the desired current or voltage output range. Be sure to match the performance of the analog output stage closely to that of the sensor acquisition circuitry; including resolution, offset, gain error, non-linearity and noise.

DAC considerations

The DAC commonly sets the performance capabilities for the analog output stage, so select it carefully. Many sensor transmitters are designed with 16-bit DACs, but systems with lower resolution requirements can use 12-bit DACs. Similar to the input stage and ADC, the DAC DC offset, gain and drift errors can be removed with calibration.

Integral non-linearity (INL) errors cannot be removed with a standard gain and offset calibration and set the post-calibration accuracy. Therefore, make sure that the DAC INL specification is well below the desired final system accuracy. A differential non-linearity (DNL) specification less than 1 LSB is almost always a requirement to ensure a monotonic output.

2-wire, 4- to 20-mA output op amp circuit

A standard 2-wire, 4- to 20-mA, transmitter op amp circuit is shown in Figure 7. This circuit requires an op amp with very-low quiescent current to minimize the impact on the limited 2-wire supply-current budget of 4 mA. A linear voltage regulator is typically used to lower the +24-V loop supply voltage, which allows the use of low-voltage op amps.

The op amp input common-mode range must include the negative rail. To maximize the available output voltage swing, the output swing should include both rails. The output-current requirement is low because the op amp is only required to drive the base current of the bipolar junction transistor (BJT). The majority of the 4- to 20-mA current flows through the BJT from the collector to the emitter.

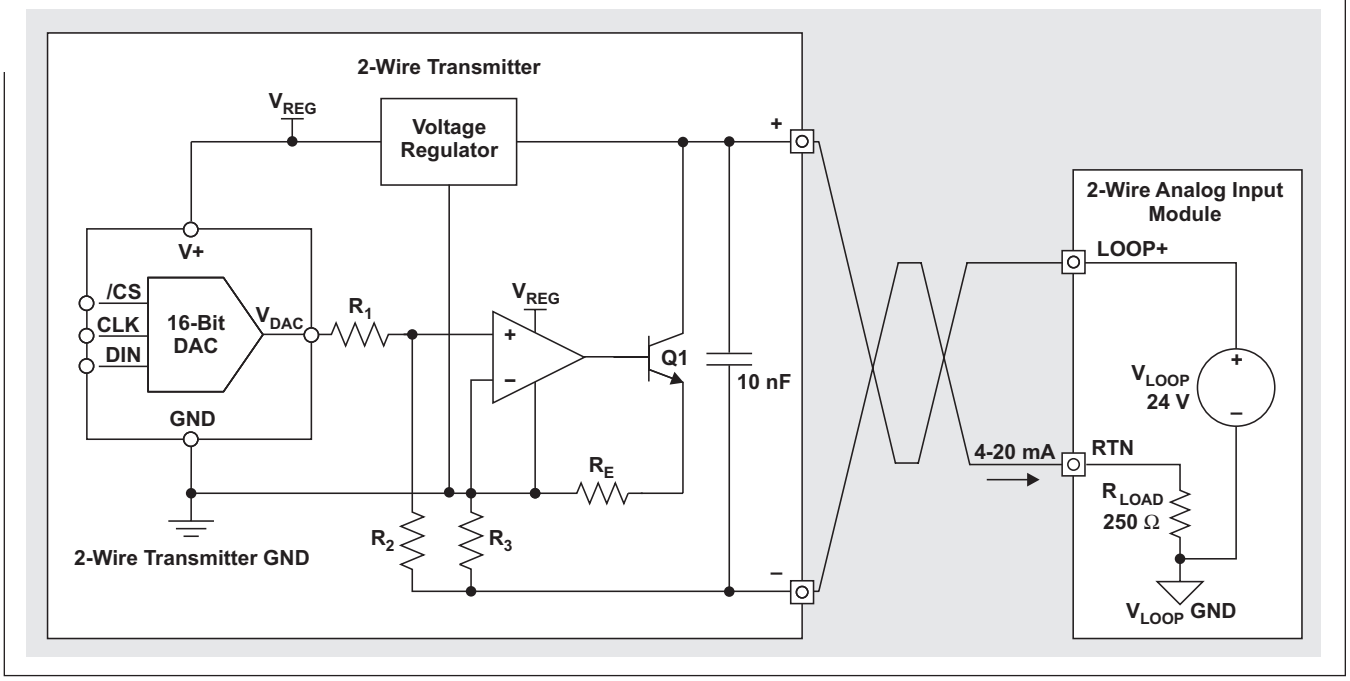
Select op amp performance specifications to match the DAC and the rest of the signal chain. The op amp must have low input offset voltage and drift. High CMRR and PSRR will improve DC performance and noise immunity of the design. eTrim™, laser trim and zero-drift (chopper/auto-zero) CMOS op amps are typically used to meet this circuit's performance requirements.

As shown in the transfer function in Equation 6, resistors R_1, R_2, and R_3 set the circuit's gain. Select precision resistors with low tolerance and temperature coefficients. Ratiometric tolerance and drift-matching the resistors greatly improves performance of the circuit over temperature.

$$I_{OUT} = \frac{V_{DAC}}{R_1 \times \left(1 + \frac{R_2}{R_3}\right)} \quad (6)$$

The circuit must maintain a stable output response to load transients and changes in the output current. Therefore, it is important to select the proper emitter resistor (R_E) based on the Q-point on the V-I curve load line.[5] A properly selected value for R_E results in a stable feedback network.

Figure 7. Loop-powered 4- to 20-mA transmitter



3-wire voltage-output op amp circuit

A standard op amp circuit used to create a 3-wire voltage output is shown in Figure 8. High-voltage op amps are required for 3-wire circuits to meet the output voltage-range requirements. Single-supply, 0- to 10-V outputs require an input common-mode range that includes ground (GND) with a rail-to-rail output stage to reduce zero code errors in the system.[6] Performance requirements for the op amp are the same as the 2-wire circuit; such as low-offset and drift with high CMRR and PSRR.

The gain is set by resistors R_F and R_G. Select them based on the same criteria as the gain-setting resistors in the 2-wire circuit.

$$V_{OUT} = V_{IN} \times \left(1 + \frac{R_F}{R_G}\right) \quad (7)$$

In a 3-wire voltage-output circuit, the op amp directly drives the system load, which can vary greatly depending on the final application. Therefore, a robust op amp output stage is required that can deliver upwards of ±30 mA of output current into a wide range of capacitive loads. Few amplifiers can directly drive large capacitive loads, so the compensation network formed by R_{ISO}, R_F, C_F, and C_L is required for a stable output.[7] To properly compensate the circuit, the op amp open-loop gain (A_{OL}) and open-loop output impedance (Z_O) must be known. Furthermore, the variations in the A_{OL} and Z_O curves over the system operating conditions need to be considered, or the design may become unstable.[8, 9]

Conclusion

There are many design considerations for resistive-bridge pressure sensors in industrial process-control applications. Performance and specifications of the input signal-conditioning stage, the ADC, and the analog output stage must all be evaluated. This article presented primary design considerations for each of these stages of the signal chain and provided guidance to the designer when selecting components for the design.

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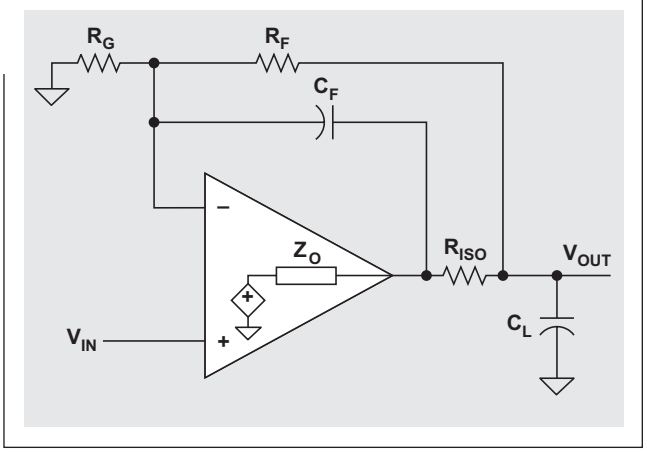
Figure 8. Compensation circuit for capacitive load drive



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Fast input-voltage transient response with digitally-controlled isolated DC/DC converters

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Introduction

Telecommunications equipment is often subjected to environmental and other electrical stresses such as lightning strikes, equipment faults, and capacitor-bank switching. These events can cause input-voltage transients of up to 100 V for durations of 10 ms. Various telecommunications standards, including the American National Standard (ANSI T1.315-2001 Specification) and Alliance for Telecommunications Industry Solutions (ATIS-0600315.2007 Specification), dictate the behavior of DC-powered equipment used in telecommunications environments.

In particular, these standards stipulate required behaviors when exposed to overvoltage transients. Overvoltage-transient conformance to the above specifications requires that a power supply must:

- Be able to handle an input surge voltage of 100 V for 10 ms
- Not be damaged or result in performance degradation

The design goals for today's state-of-the-art isolated DC/DC converters generally target an output voltage disturbance of less than 10% for all transient conditions of the input voltage. A large overshoot at the output may damage the downstream equipment and a big output-voltage undershoot can cause the equipment to shut down or reset. In the case of isolated DC/DC converters with synchronous rectification, a large reverse current may be generated that subjects electrical components to overstress and increases system noise, thus, disturbing the converter's normal operation.

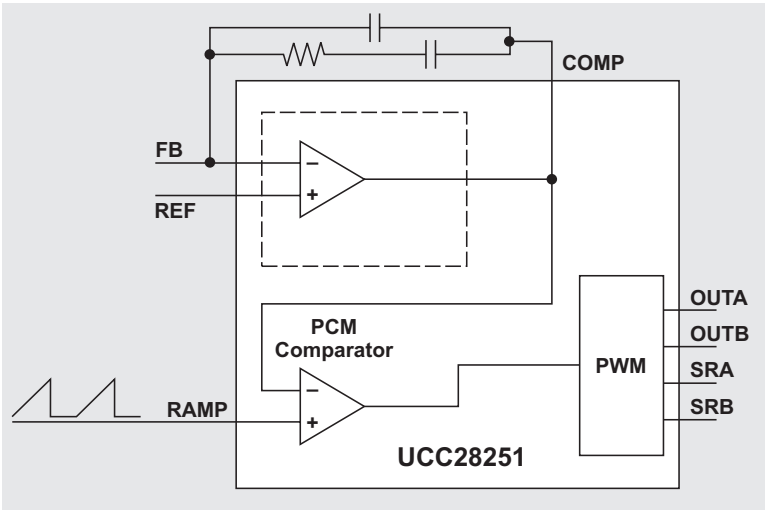
One condition that a designer must be mindful of is the input-voltage slew rate. An extremely-fast voltage slew rate (for example, 50 V to 75 V in 2 µs) often can cause the output-voltage disturbance to exceed ±10%. It is unlikely that these standards will be relaxed any time soon. In fact, these conditions most likely will become even more stringent. Therefore, today's isolated DC/DC power supplies must have a very good control method (or voltage feed forward) to limit the magnitude of the output-voltage undershoot and overshoot caused by an input-voltage transient.

Input-voltage feed forward within the power supply's nominal input range

A huge challenge for designers of digitally-controlled isolated DC/DC converters is the attenuation of the output-voltage fluctuations during abrupt input-voltage transients that are within the power supply's nominal input voltage range. However, in traditional primary-side controlled solutions (Figure 1), this is easy to manage. The sawtooth signal to the comparator has a peak value that is proportional to the input voltage and is used to terminate the duty cycle of the pulse-width modulator (PWM). In this way, the product of the input voltage and primary turn-on time is almost a constant value, no matter how fast the input voltage changes. Using this method, the output voltage has a very fast response for line-input transients.

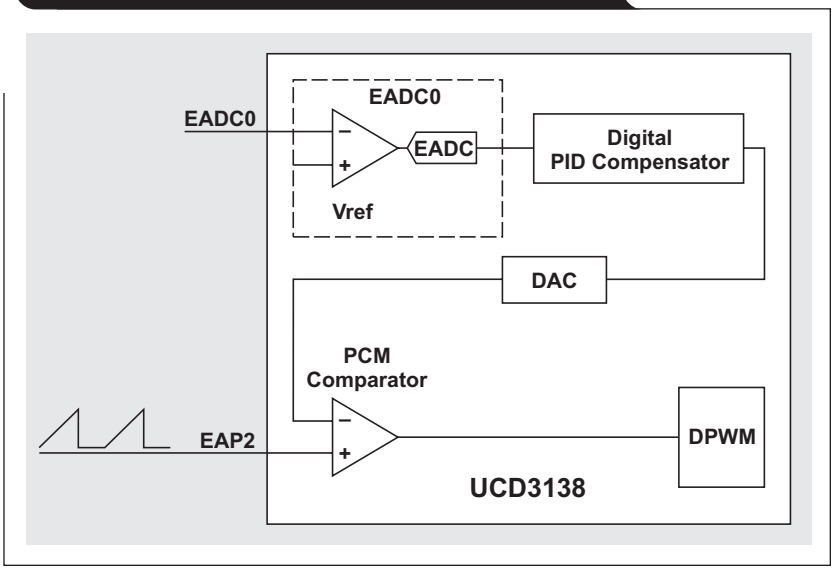
In digitally-controlled solutions, the digital controller is usually located on the transformer's secondary or output side. This allows the controller to achieve a better load-transient response and to easily perform communication with the host microcontroller via I^2C or PMBus™.

Figure 1. Analog controller with PWM generation



Compared with a primary analog controller solution, it becomes more difficult for the digital controller to quickly and accurately detect the input voltage transients occurring on the transformer's primary side. In a purely digital solution, the designer must consider further complexities such as A/D conversion delay, digital processing delay, and digital pulse-width modulator (DPWM) generating delay.

Figure 2. A digital controller configured similar to an analog PWM controller



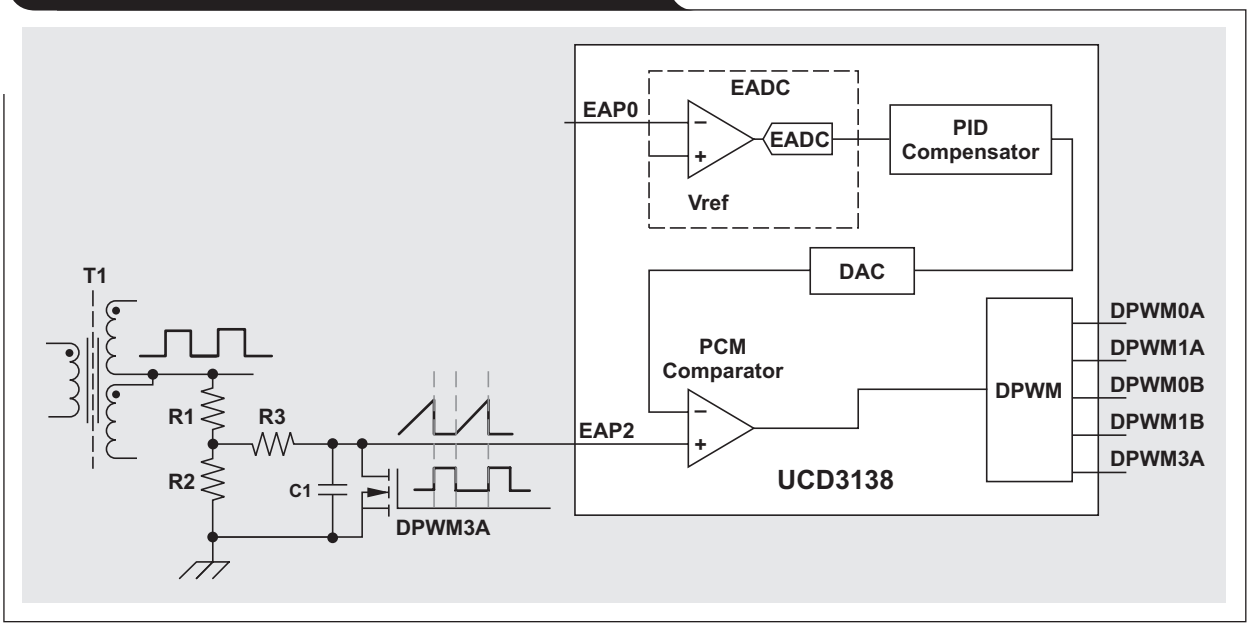
Solution

It is possible for a digitally-controlled solution to control duty cycle much like the analog solution. This means that the digital-power controller in Figure 2 can be configured with similar performance to the analog controller in Figure 1 while maintaining its digital flexibility.

The key challenge is how to generate a ramp similar to the analog solution. In buck-derived DC/DC isolated topologies, input voltage can be reflected on the transformer's secondary winding during the effective on time of the primary switch. The hard-switching full-bridge (HSFB) topology shown in Figure 3 is an example of the method for generating this ramp.

T1 represents the power transformer used in the HSFB topology. When a pair of primary switches are turned on, the input voltage reflected on the secondary winding charges C1 through R1 and R3. This continues until the PCM comparator terminates the pulse of the primary gate driver when the sawtooth voltage on the EAP2 pin exceeds the DAC's output. DPWM3A is a complementary signal of the primary gate driver that is generated by the digital controller. This controller is used to discharge C1 at every half switching cycle. R2 is added to limit the voltage on the EAP2 pin, which is lower than its maximum voltage rating at any condition.

Figure 3. RAMP generation with HSFB topology



Test results

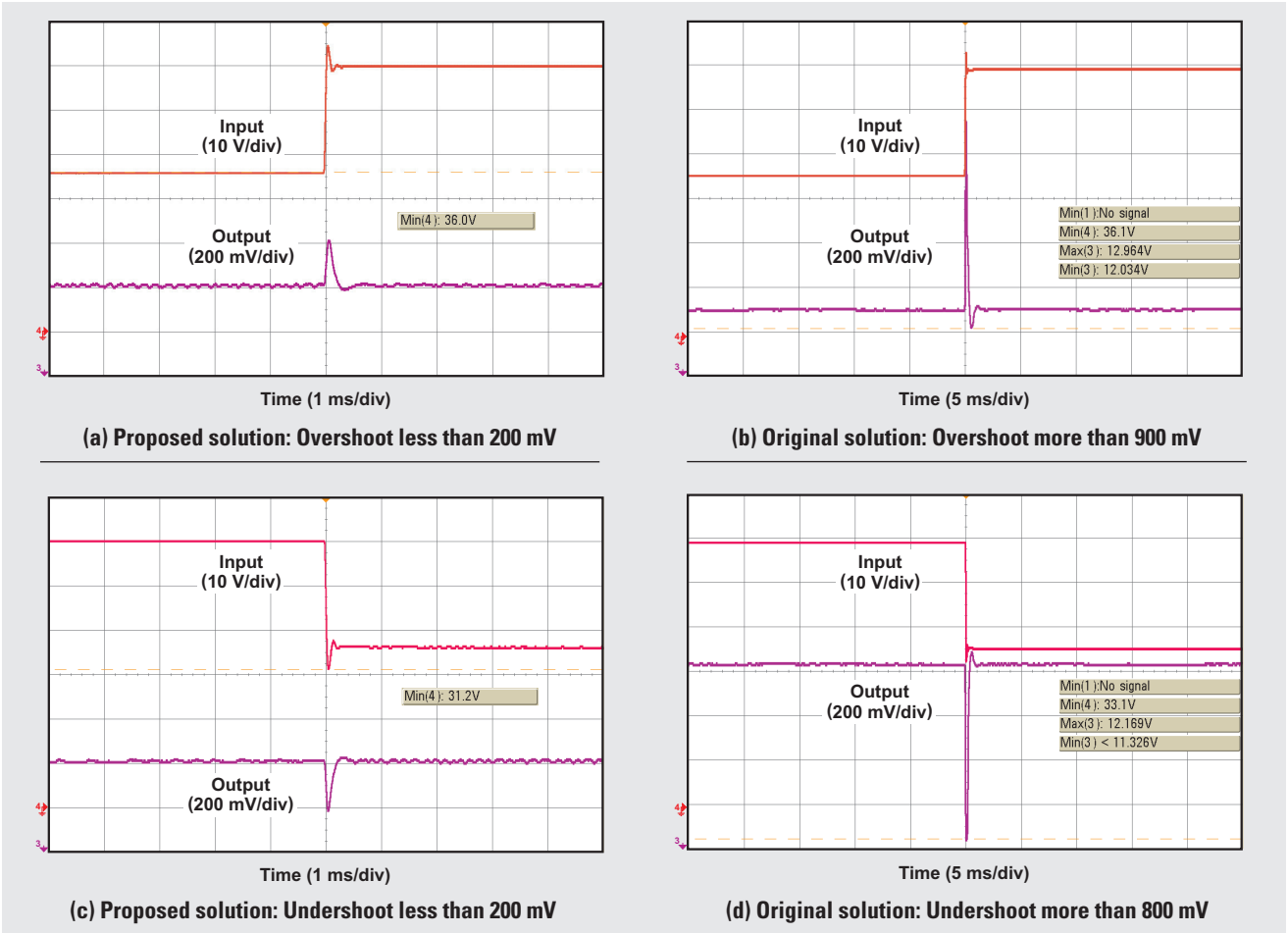
The test comparison in Figure 4 was generated with the UCD3138HSFBEVM-029 evaluation module (EVM), which is a HSFB demo module with a 12-V output. This EVM employs a non-linear multiplier solution to implement input-voltage feed-foward control that can achieve a good output response. However, the method proposed here can achieve an even better performance. The amplitude of both overshoot and undershoot is reduced by four times when the input voltage steps between 36 V and 60 V with a voltage slew rate of 1 V/µs. The 36-V minimum voltage of this transience test was chosen because the output voltage cannot maintain below that limit, or output voltage-hold threshold.

Avoid reverse current when input voltage drops below the output voltage-hold threshold

When the input voltage drops below the output voltage-hold threshold, the duty cycle reaches its maximum value. Now the product of the input voltage and duty cycle decreases. If the power stage still operates in the synchronous rectification mode, this causes the energy stored in the output capacitor to flow in a reverse direction to the input.

The reverse current could be huge, which may cause overcurrent stress on the power train. A popular solution is to add a reverse-current protection circuit where the synchronous rectifier (SR) is turned off when reverse

Figure 4. A comparison test for input-voltage transients between 36 V and 60 V



current is larger than a safe threshold. This way, the loop of the reverse current through the output inductance is cut off abruptly. The energy stored in the output inductance, causes an avalanche breakdown of the SR, which can cause SR failure.

Solution

To solve this problem, a voltage-detection circuit can turn off the SR immediately. This occurs before the reverse current is generated and when the input voltage drops to lower than the output voltage-hold threshold. The circuit shown in Figure 5 detects the input voltage from the transformer's center tap (V_TAP). The EAP1 pin, which belongs to the UCD3138 front-end block, can be configured to sample the voltage only at the on-time of the primary switch when the V-TAP's voltage reflects an input voltage.

In Figure 6, the scaled down input voltage is converted to a digital number stored in the ABS registers. A pair of digital window comparators inside the digital controller are configured to detect the undervoltage input and the input-voltage recovery. When an input voltage below the output voltage-hold threshold is detected, within nanoseconds, digital comparator 0 issues a fault signal to the DWPM module to shut down the DMPM0B/1B, SR-gate drive signal. When the input voltage recovers, the digital comparator 1 triggers a fast firmware interruption that enables the SR-gate driver. A pre-bias startup routine is started so that the output voltage can recover in the shortest amount of time.

Figure 5. Input-voltage detection circuit

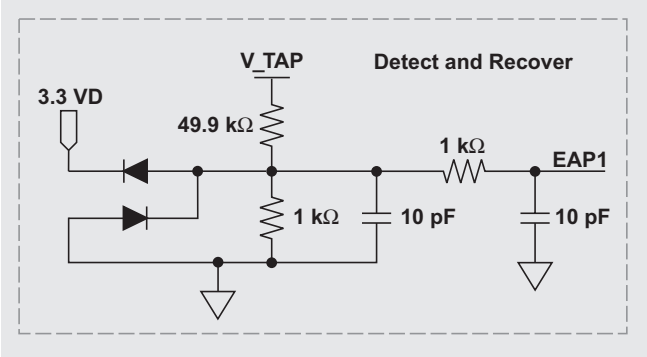


Figure 6. Turn-on/off control of a synchronous rectifier

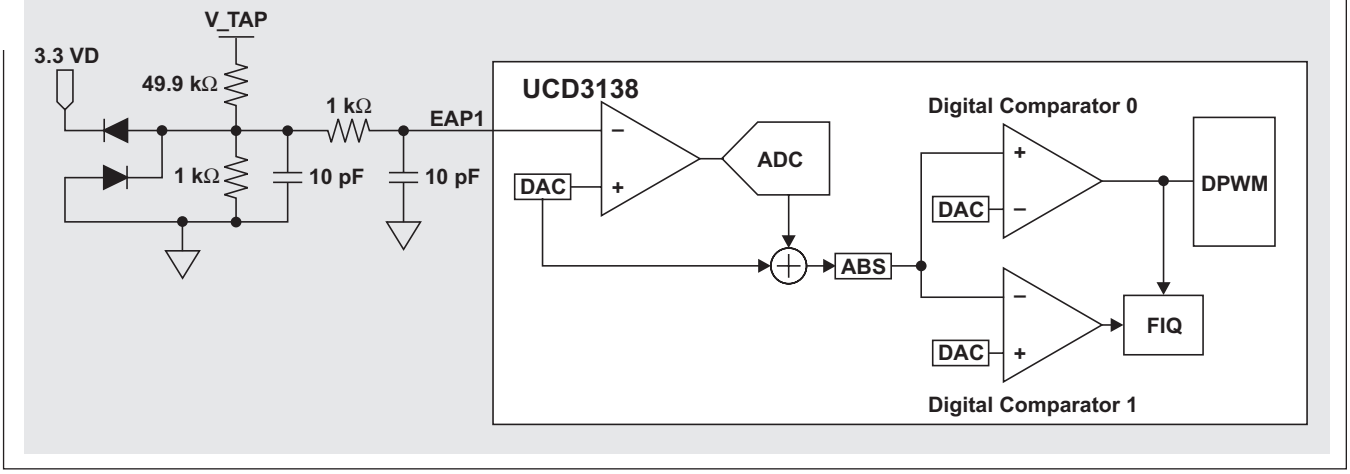
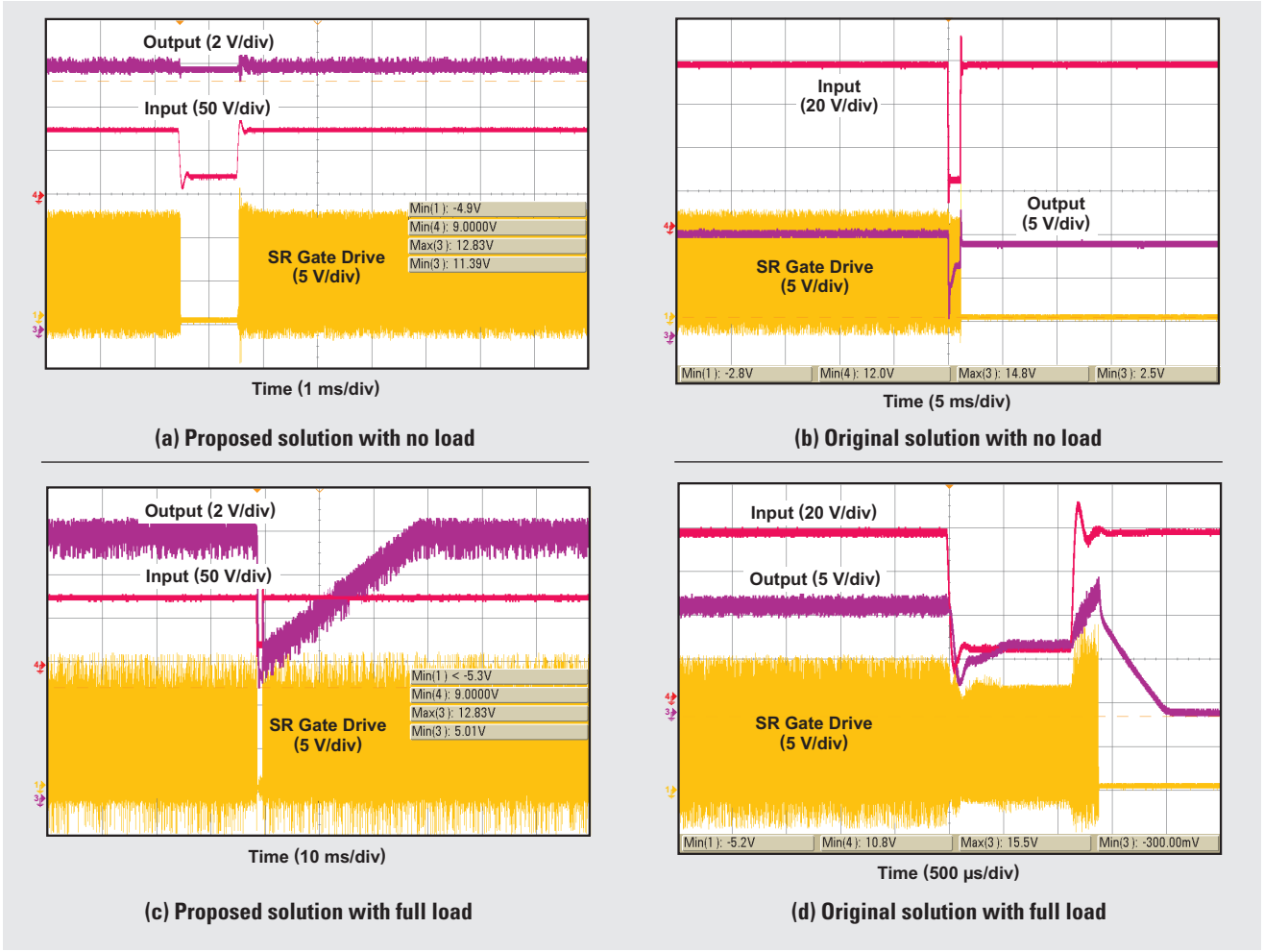


Figure 7. Test results when the input-voltage transient is between 60 V and 20 V



Test results

The proposed solution is designed to shut down the SR gate driver signal as soon as the input voltage drops below 36 V (Figure 7a). There is no reverse current discharging the output capacitor and the output voltage under no-load test barely changes while the input voltage stays at 22 V. In comparison, the original SR gate-driver EVM solution (Figure 7b) continues to run, even though the input voltage is below 36 V. The reverse current is generated, causing the output voltage to be discharged, even under no-load conditions.

The original EVM solution does not have a pre-bias start-up function when the input voltage recovers to its normal value, which causes an output voltage overshoot and triggers OVP after the input voltage recovers (Figure 7d). For a full-load test, the output voltage in the proposed solution is discharged by the load (Figure 7c). When the input voltage recovers, the output can immediately and monotonously rise back to the regulated voltage, which is controlled by the pre-bias startup routine.

Conclusion

It was shown that a secondary-side, digitally-controlled solution provides good performance under line-transient test conditions.

A proposed solution showed that the output voltage remained almost unchanged as long as the input-voltage transient is above the output voltage-hold threshold. The solution also avoided reverse current from occurring when the input voltage was lower than the output voltage-hold threshold. Additionally, a stringent and monotonous startup waveform was achieved when the input voltage recovered.

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