JESD204B multi-device synchronization: Breaking down the requirements

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Introduction

A common trend in wireless transceivers, such as cellular communications systems, is to adopt beamforming technology to enable better system sensitivity and selectivity. This trend results in an increased number of antennas per system and requires synchronization between each antenna to achieve precise control of signal phases during transmission and reception. Synchronization, however, is not limited to just communications systems. There are numerous applications that make use of synchronized signal chains, including phased-array radars, distributed antenna arrays, and medical imaging machines.

Most systems that require multiple synchronized signal chains also require synchronization of analog-to-digital converters (ADCs) and digital-to-analog converters (DACs). The JESD204B serialized interface for high-speed ADCs and high-speed DACs has simplified the process for achieving synchronization while also enabling higher antenna density by reducing layout size and the number of device pins. So it should not be a surprise that another trend is an increased adoption of JESD204B data converters in these systems. System and device requirements for synchronization of JESD204B ADCs and DACs can be a bit confusing for first-time users of the standard. The objective of this article is to clarify the requirements for achieving synchronization among subclass 1 JESD204B devices and simplify the discussion to just the applicable portions of the standard.

Synchronization requirements

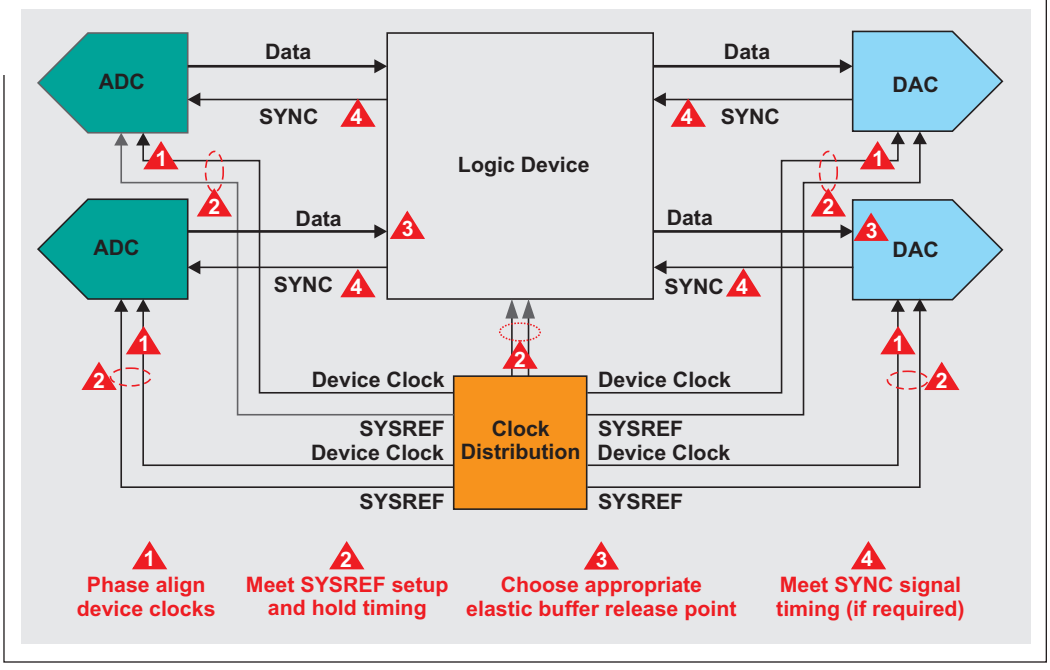
Achieving synchronization of data converters in a JESD204B system can be broken down into the four basic requirements visualized in Figure 1.

1. Phase align the device clocks at each data converter
2. Meet setup-and-hold times for SYSREF relative to the device clock at each data converter and logic element
3. Choose appropriate elastic buffer release points in the JESD204B receivers to guarantee deterministic latency
4. Meet SYNC signal timing requirements (if required)

Phase aligning device clocks

In a JESD204B system, the device clock is used either as the converter's sampling clock (with or without a divider), or as a reference for a phase-locked loop (PLL), which generates the sampling clock. As such, the phase alignment of the device clocks at each converter is critical for maintaining alignment of the sampling instances in each

Figure 1. Requirements for multi-device synchronization in JESD204B systems



converter. The alignment of the device clocks is dependent on how well the propagation delays on the clock distribution paths are controlled, including how well the alignment is maintained over temperature changes.

SYSREF requirements

The SYSREF signal is the most important signal for achieving repeatable system latencies and synchronization. The two requirements for the SYSREF signal are that it meets setup-and-hold times relative to the device clock, and that it runs at an appropriate frequency. Note that SYSREF can be implemented as a single pulse that removes the frequency requirement; however, this also requires DC coupling of the SYSREF signal. In many cases, DC coupling of the SYSREF signal is not possible due to input common-mode voltage requirements.

SYSREF timing requirements

The most challenging requirement for SYSREF is setup-and-hold timing. For lower-speed pipeline ADCs and baseband DACs (<1 GSPS), the setup-and-hold requirement is not as difficult. However, for faster devices such as gigasample ADCs and RF-sampling DACs, the higher device clock rate reduces the setup-and-hold window for SYSREF and may require dynamic delay adjustment to maintain timing over all conditions.

JESD204B allows for flexibility in how data converters are clocked. For instance, some devices contain an integrated PLL that allows a lower-frequency device clock to be used, which is then multiplied up to create the converter's sampling clock. The device clock still captures SYSREF, but the lower frequency greatly eases the setup-and-hold requirements. Additionally, devices may contain features that either aid in meeting timing or relaxing the requirements. If proper timing cannot be met, then an external calibration procedure will likely be needed to achieve synchronization.

Choosing the frequency of SYSREF

There is a limitation on frequencies that can be used for continuous or gapped-periodic SYSREF signals. Note that this does not apply for single-pulse implementations. The main requirement is that the SYSREF signal must run at a frequency equal to or at an integer division of the local multi-frame clock (LMFC) frequency. This requirement is given in Equation 1, where $f_{BITRATE}$ is the interface bit rate of the serializer/deserializer (SerDes), F is the number of octets per frame, K is the number of frames per multi-frame block, and n is any positive integer.

$$f_{SYSREF} = \frac{f_{BITRATE}}{10 \times F \times K \times n} \quad (1)$$

Note that the K parameter can be changed to adjust the SYSREF frequency, but each device may have its own limitations on possible K values in addition to the standard's limitation of $17 \le F \times K \le 1024$.

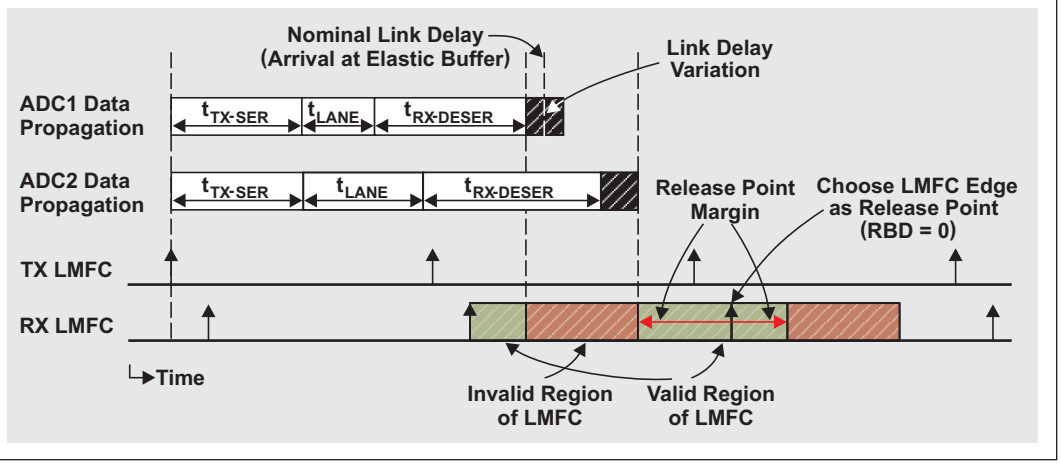
There may be additional requirements on the frequency of SYSREF if the device uses internal clock dividers or SYSREF for synchronization of other digital features. For instance, if a device uses an internal clock divider to generate the sampling clock, then the divider needs to be synchronized to maintain sampling clock phase alignment in all devices. This sets an additional limitation on the SYSREF frequency because it must be an integer division of both the LMFC frequency and the lowest internally-generated frequency. Typically, this is not an issue, but it should be verified that the calculated SYSREF frequency meets this requirement and then adjust it accordingly.

Elastic buffer release point

The third requirement for synchronization is to select a proper elastic buffer release point in the JESD204B receiver to achieve deterministic latency. The elastic buffer is the key block for achieving deterministic latency. It does so by absorbing variations in the propagation delays of the serialized data as it travels from the transmitter to the receiver. A proper release point is one that provides sufficient margin against variations in the delays. An incorrect release point will result in a latency variation of one LMFC period.

Choosing a proper release point requires knowing the average arrival time of data at the elastic buffer (referenced to an LMFC edge) and the total expected delay variation for all devices. With this information the region of invalid release points within the LMFC period can be defined, which stretches from the minimum to maximum delay for all lanes. Essentially, the designer must guarantee that the data for all lanes arrives at all devices before the release point occurs.

Figure 2. Defining the valid region of LMFC for elastic-buffer release point



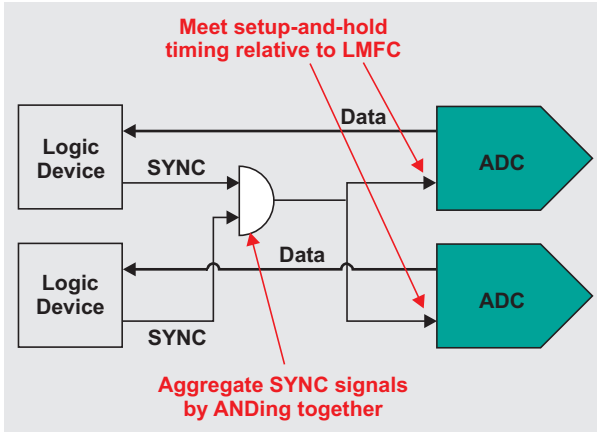
It is easier to demonstrate this requirement by using a timing diagram (Figure 2) that shows the data for two ADCs. The second ADC has a longer routing distance and results in a longer link delay. First, the invalid region of the LMFC period is marked off as determined by the data arrival times for all devices. Then, the release point is set by using the release buffer delay (RBD) parameter to shift the release point an appropriate number of frame clocks from the LMFC edge so that it occurs within the valid region of the LMFC cycle. In Figure 2, the LMFC edge (RBD = 0) is a good choice for the release point because there is sufficient margin on each side.

SYNC signal timing

As data converter sampling rates have increased, so has the desire to maintain low interface speeds. This is often accomplished by implementing digital up-converters (DUCs) in DACs or digital down-converters (DDCs) in ADCs. The DUCs and DDCs often implement numerically-controlled oscillators (NCOs) that must be synchronized in all devices to maintain overall system synchronization. The most common approach is to synchronize the NCOs by using the LMFC rising edge and elastic-buffer release point. In ADCs, the NCOs can be synchronized using the first LMFC edge that occurs after the SYNC signal is deasserted, which corresponds to the start of the initial lane alignment sequence (ILAS) transmission. In DACs, the typical approach is to synchronize the NCOs when the elastic buffer is released.

There is a timing requirement on the SYNC signal in order to achieve multi-device synchronization between multiple ADCs or DACs that utilize NCOs. The SYNC signal must be deasserted by all receivers on the same LMFC edge and received at the transmitters in the same LMFC cycle. The simplest approach to meeting the first requirement is to AND the SYNC signals from all receivers together, then distribute this aggregated signal to each transmitter (Figure 3). This also sets a requirement on the

Figure 3. Aggregating SYNC signals to synchronize NCOs in ADCs



SYNC signal in that it must meet the needed setup-and-hold times relative to the LMFC edge in the transmitting device. If DDCs or DUCs are not used in the ADCs or DACs, then there is no requirement for SYNC signal timing and each device can start up at independent times and still achieve synchronization.

Example clocking schemes

The most difficult synchronization requirement is meeting the SYSREF-to-device clock-timing relationship. To address these concerns, two examples of clocking implementations are examined.

Typical JESD204B clocking scheme

The easiest way to maintain proper setup-and-hold times for SYSREF is to use a single clocking device that implements device clock and SYSREF pairs. These pairs maintain good phase alignment over all conditions because of the matched outputs. One example is the LMK04828 from Texas Instruments, which implements seven pairs of

device-clock and SYSREF outputs. Figure 4 shows an example system using the LMK04828 to clock multiple ADS42JB69 ADCs. This scheme can be used for low-sample-rate converters or for gigasample converters with internal PLLs. A JESD204B-compliant clock jitter cleaner, such as the LMK04828, also can be used as a clock distributor and SYSREF generator by bypassing the PLLs in favor of a higher-performance input clock while still maintaining the benefit of the matched output pairs.

Gigasample ADC and DAC clocking schemes

Clocking of JESD204B gigasample converters is more challenging when the device does not have an internal PLL or if the PLL is bypassed to achieve certain performance targets. One example of such a high-speed data converter is the ADC12J4000, which can operate at up to 4 GSPS and requires a 4-GHz device clock. Figure 5 shows an example clocking tree using TRF3765 RF synthesizers to generate the 4-GHz clocks and the LMK04828 to generate the reference clocks and SYSREF signals.

In this case, the system designer can make use of programmable delays in the clock jitter cleaner and data converter to meet setup-and-hold times over all conditions. Furthermore, the ADC12J4000 has a dirty SYSREF capture feature that checks for setup-and-hold time issues. The combination of these features enables proper capture of SYSREF over all temperatures after some minor characterization of the delay variations in the system. First, the dirty SYSREF capture can be used to find the optimal nominal-delay settings. Then, as the system conditions change, the dirty capture bit can be monitored to find setup-and-hold time issues. When a timing issue is found, the clock jitter cleaner or data converter SYSREF delays can be used to shift the SYSREF signal back into the appropriate region. After characterizing the delays, the system can monitor the temperature and adjust the delays as necessary.

Figure 4. Using LMK04828 to synchronize multiple JESD204B data converters

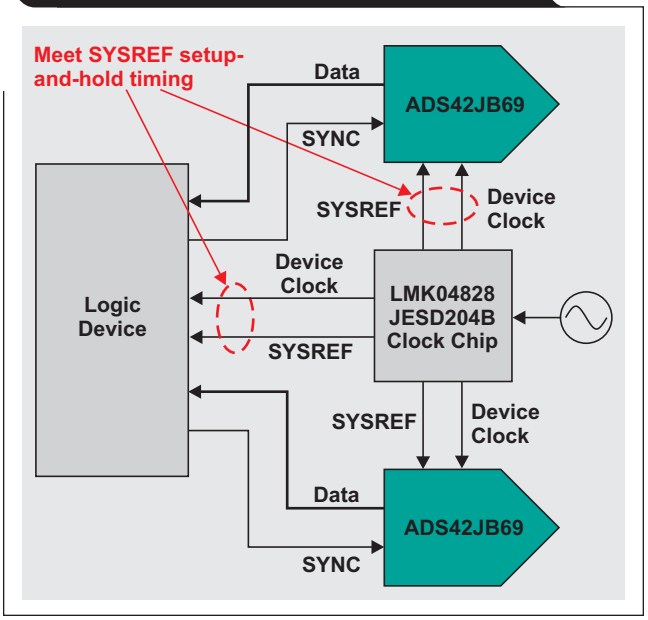
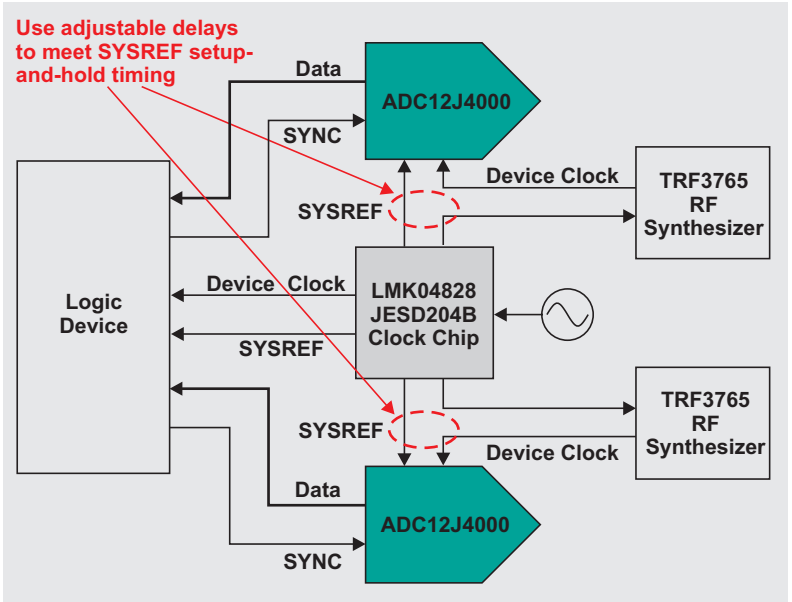


Figure 5. Using LMK04828 and TRF3765 to synchronize multiple gigasample data converters



Conclusion

System designers must have a good understanding of the four main requirements for synchronization of JESD204B ADCs and DACs. Clock-distribution path requirements are important to maintain phase control for both the device clock and SYSREF signals. Also, the SYSREF signal must meet setup-and-hold times relative to the device clock and at an appropriate frequency. Another synchronization requirement is a proper elastic buffer release point in the JESD204B receiver to archive deterministic latency. Additional SYNC timing may be required in systems that use DDCs or DUCs. Two examples of clocking implementations were provided to show how to achieve conditions for overall system synchronization.

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3. Thomas Neu, "Enabling Larger Phased-Array Radars With JESD204B," *RF Globalnet*, August 2, 2013.
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Related Web sites

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www.ti.com/jesd204b

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