Analog Applications Journal

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Contents

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Introduction

The *Analog Applications Journal* (AAJ) is a digest of technical analog articles published quarterly by Texas Instruments. Written with design engineers, engineering managers, system designers and technicians in mind, these "how-to" articles offer a basic understanding of how TI analog products can be used to solve various design issues and requirements. Readers will find tutorial information as well as practical engineering designs and detailed mathematical solutions as they relate to the following applications:

- Automotive
- Industrial
- Communications
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AAJ articles include many helpful hints and rules of thumb to guide readers who are new to engineering, or engineers who are just new to analog, as well as the advanced analog engineer. Where applicable, readers will also find software routines and program structures and learn about design tools. These forward-looking articles provide valuable insights into current and future product solutions. However, this long-running digest also gives readers archival access to many articles about legacy technologies and solutions that are the basis for today's products. This means the AAJ can be a relevant research tool for a very wide range of analog products, applications and design tools.

Distortion and source impedance in JFET-input op amps

By John Caldwell
Analog Applications Engineer

Designers of low-distortion analog circuits in industrial data acquisition, seismic measurement, and high-fidelity audio are aware that many operational amplifiers (op amps) produce greater distortion when configured as non-inverting amplifiers. In the non-inverting configuration, the input signal appears as a common-mode signal at both inputs. The subtraction performed by the op amp on the two inputs is finite and slightly non-linear, producing a small amount of additional distortion at the op amp output. This effect is often referred to as common-mode distortion.[1]

It is less widely known that some op amps show more severe common-mode distortion when the input-signal source has a high output impedance. Using the TL072, a JFET-input general-purpose op amp, let's compare the output distortion for two source impedances. Figure 1 shows the TL072's output distortion when the source impedance is 20 Ω and 10 kΩ. The total harmonic distortion and noise (THD+N) is substantially increased in the 10-kΩ case – more than could be attributed to the additional source resistor.

This behavior is typical of older JFET-input op amps like the TL072 and limits their usability in many circuits such as Sallen-Key active filters.[2] At the time, JFETs offered some advantages over bipolar transistors when used as the input devices of an op amp. For example, the reduced current noise allowed JFET-input op amps to be used in high-impedance applications. Furthermore, JFETs could be fabricated with the existing bipolar semiconductor processes, giving them a major advantage over MOSFETs.

Figure 2 shows the cross section of a p-channel JFET fabricated using ion implantation on a p-type substrate in a junction-isolation process.[3] The channel was formed by implanting p-type impurities into an n-type region. An n-type region is then implanted on top of the channel (n-type top gate) and connected to the region below the channel to form the gate.

The junction between the p-type substrate and n-type gate acts as a reverse-biased diode. This allows the JFET to have extremely low input current, while creating a parasitic capacitance (C_{GSS}) from the gate to the substrate.

At the interface of p-type and n-type semiconductor material, a process of diffusion occurs where electrons and holes migrate across the interface leaving behind charged ions on their respective sides. The migrating charge carriers recombine with the opposing charge carriers from the opposite side and are eliminated, which produces an area with no mobile charge carriers. This area is called the depletion region because the mobile charge carriers have been depleted. In this region, the semiconductor material behaves as an insulator. The resulting structure resembles a capacitor with n- and p-type regions being the conductive electrodes, and the depletion region acts as the dielectric. Due to the large contact area between the gate

Figure 1. THD+N measurement of a TL072 op amp

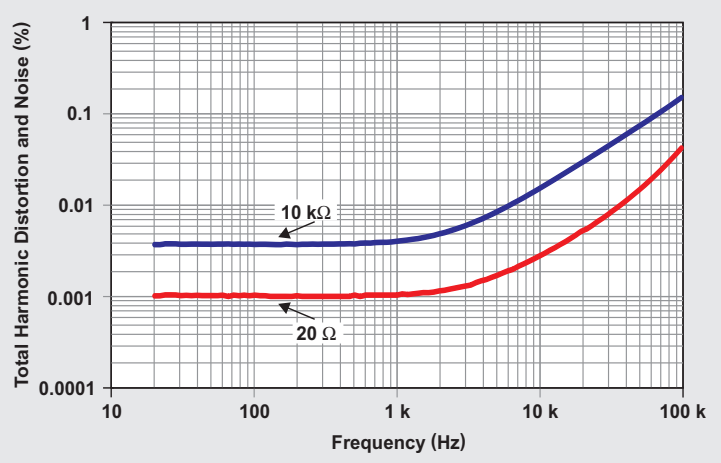
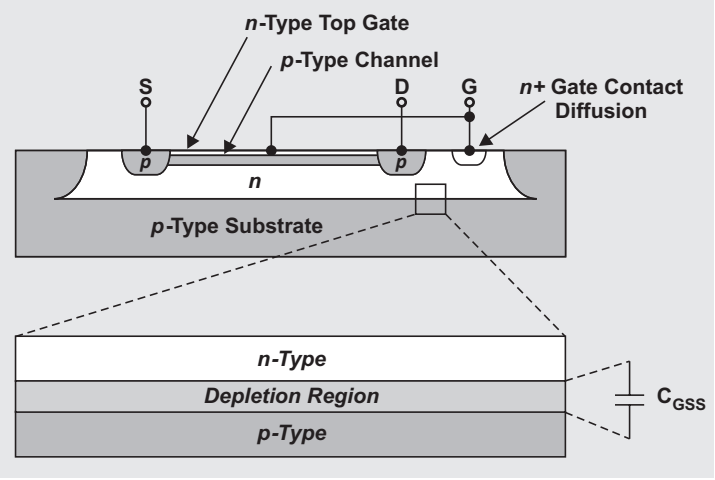


Figure 2. Ion-implanted p-channel JFET structure



and the substrate, the gate-to-substrate capacitance, C_{GSS}, is typically much larger than the gate-to-source and gate-to-drain capacitances.[3] Therefore, the C_{GSS} of the input JFETs is the dominant contributor to the input common-mode capacitance of these op amps.

Like all capacitors, the capacitance of the p-n junction is dependent on the area of its electrodes and the distance they are separated. Although the area of the junction is fixed, the width of the depletion region is not. It depends on the direction and intensity of the electric field across the depletion region.

During the initial diffusion, the ions left behind by the diffusing charge carriers produce an electric field which opposes further diffusion. This is called the built-in voltage of the junction. The application of an external voltage to the junction has the effect of growing or shrinking the width of the depletion region and changing the capacitance of the junction. The gate-to-substrate capacitance of a JFET varies as a function of gate-to-substrate voltage according to the equation:

$$C_{GSS} = \frac{C_{GSS0}}{\sqrt{1+\frac{V_{GSS}}{\psi_0}}} \quad (1)$$

In Equation 1, C_{GSS0} is the junction capacitance at 0 V, V_{GSS} is the gate-to-substrate voltage. Further, ψ_0 is the built-in voltage of the junction, which typically is about 0.7 V. In most op amps, the substrate is held at the negative supply voltage (V_{EE}). Therefore, as the common-mode voltage changes, the V_{GSS} term in Equation 1 changes, which increases or decreases the gate-to-substrate capacitance, C_{GSS}.

In Figure 3, input common-mode capacitances, C_{CM1} and C_{CM2}, were added to represent C_{GSS} of the input JFETs.

The input common-mode capacitance of the non-inverting input, C_{CM1}, must be charged and discharged by a small current, I_S, from the input source, V_S. If the input capacitance is not a constant, but depends on the input voltage, the charging current drawn from the source is no longer linearly related to the rate-of-change of the input voltage signal:

$$I_S \neq C_{CM1}\frac{dV_S}{dt} \rightarrow I_S = \frac{C_{GSS0}}{\sqrt{1+\frac{V_{IN}-V_{EE}}{\psi_0}}} \times \frac{dV_S}{dt} \quad (2)$$

This behavior is similar to the voltage coefficient of discrete ceramic capacitors.[4,5] The change in capacitance with applied voltage distorts the current in the capacitor. This distorted current drawn from the source produces a distorted signal at the op-amp input due to the voltage drop across R_S.

$$V_{IN} = V_S - I_S R_S \quad (3)$$

It is possible to cancel this distortion by placing a resistance equal to the source impedance in the op amp's feedback loop. This produces an identical distortion signal at the op amp's inverting input. Because the distortion is now common to both inputs, it is removed by the op amp's common-mode rejection. Unfortunately, the resistance in the feedback path introduces additional noise and also can cause stability issues if it is very large.[6]

Figure 3. The varying common-mode capacitances of a JFET-input op amp

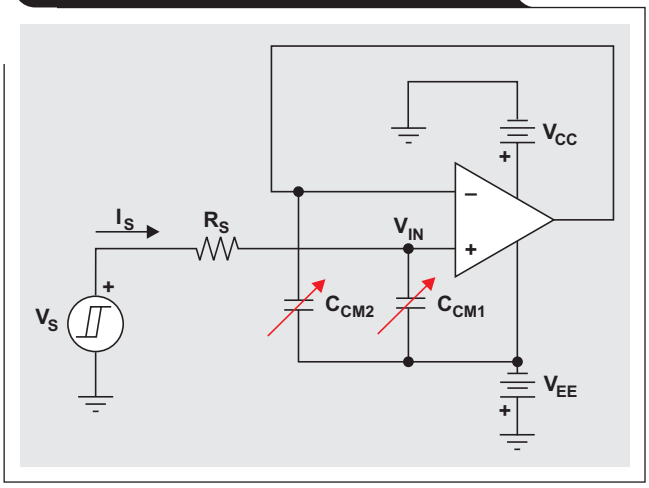
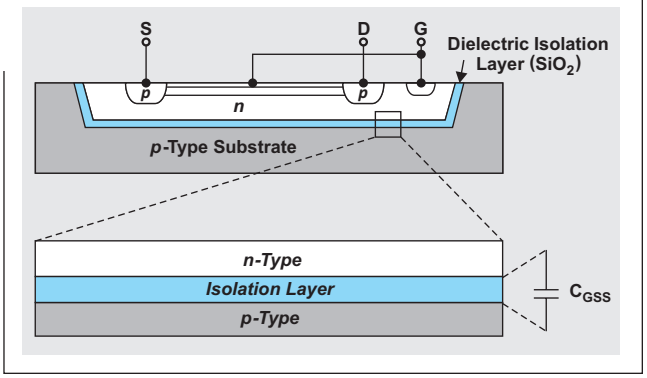


Figure 4. The isolation layer in DI processes



Ideally, to preserve low distortion when operating with high source impedances, the input common-mode capacitance needs to be stabilized to a constant value. One method to accomplish this is to fabricate the op amp with a dielectrically isolated (DI) process. As shown in Figure 4, DI processes use a layer of dielectric material, such as silicon dioxide (SiO_2), to isolate devices from the substrate and other adjacent structures. These processes were originally introduced to improve the speed of on-chip transistors by reducing the capacitance at their collectors.[3]

An additional benefit of dielectric isolation is that the JFET's gate-to-substrate capacitance no longer varies with the input common-mode voltage. The value of the gate-to-substrate capacitance is determined by the size of the device and width of the isolation layer, which is completely unaffected by an applied electric field. Furthermore, the isolation layer prevents the diffusion of charge carriers across the p-n interface that would form a depletion

region. There is still an electric field across the barrier, but its effect on the mobile charge carriers in the silicon is not large enough to affect the total capacitance.

In Figure 5, the common-mode capacitance of two op amps was measured very precisely with a network analyzer. The TL072 op amp was fabricated with a standard junction-isolated process. Over the measurement range, the input common-mode capacitance varies from 4.87 pF at +10 V to 7.10 pF at –10 V, a total change of 2.23 pF. As expected, the input common-mode capacitance increases with negative common-mode voltages because the gate-to-substrate voltage is decreasing.

Alternatively, the OPA1642 was fabricated with a DI process. The input common-mode capacitance is greatly stabilized and shows a variation of only 30 fF over the entire measurement range.

The improved stability of the input common-mode capacitance is immediately apparent in distortion measurements. Figure 6 shows the measured THD+N of the OPA1642 configured in a gain of +1 for source impedances of 20 Ω and 10 kΩ. Unlike the TL072, the distortion of the OPA1642 is unaffected by an increase in source impedance.

The need for JFET-input op amps is still prevalent today because they continue to offer a unique combination of low noise, low bias current, and excellent AC/DC performance. The introduction of DI processes in their fabrication and the resulting stabilization of the input capacitance allow modern JFET-input op amps to achieve extremely low distortion regardless of source impedance.

Figure 5: Common-mode capacitance of two JFET-input op amps

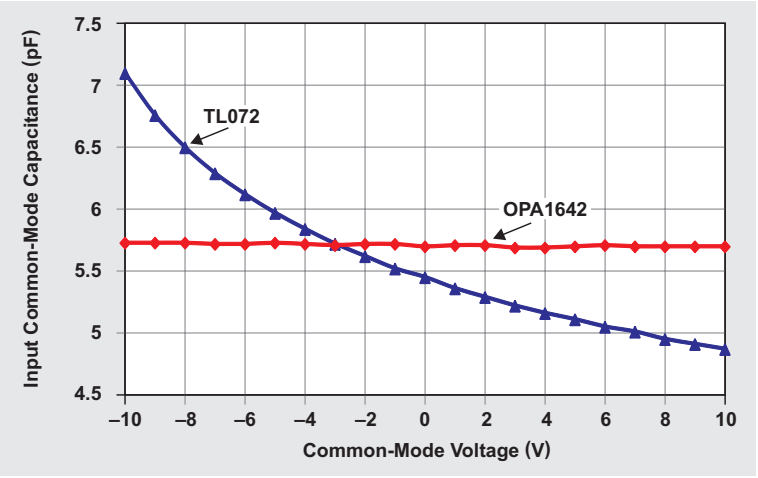
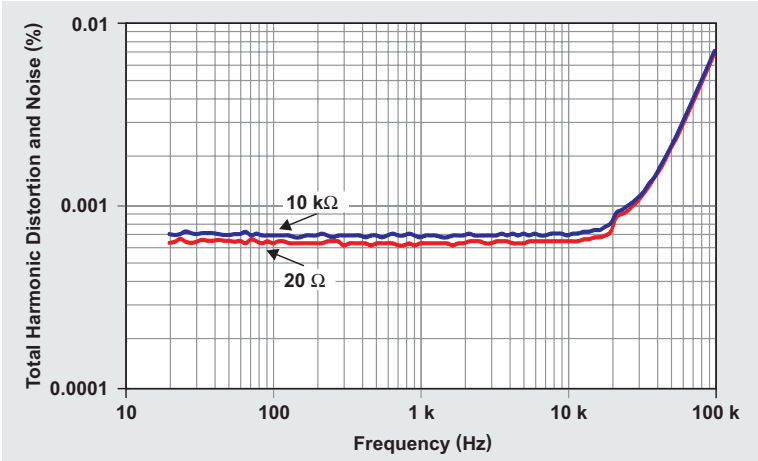


Figure 6. THD+N measurements of an OPA1642 op amp



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SPICE models for Precision DACs

By Rahul Prakash
Electrical Design Engineer

The challenge – complete system verification

Predicting the performance of a design before it is implemented is a challenge faced by every design engineer. IC designers have myriads of tools and models at their disposal to simulate their designs even before fabrication. However, when considering the full system design, there are very few components for which accurate models exist.

This means that a full system-level verification has to be done manually by the designer via budgeting, spot checks, modeling, visual inspection and modifications based on previous experience. Unfortunately, this leaves a potential for errors and bugs in the design. In some cases, several board revisions are required to achieve the intended functionality and performance.

The building blocks – Precision DAC models

The latest TINA-TI™ software models for precision DACs, such as the DAC8411 family from Texas Instruments, enable full system-level verification. The DAC8411 family consists of 8- to 16-bit single-channel, voltage-output digital-to-analog converters (DACs). The SPICE models for this family are available in two variants. The first is a parallel n-bit wide interface with output buffer, compatible with all TINA versions (Figure 1).

The second is a serial peripheral interface (SPI) with output buffer, compatible with professional TINA-TI software (Figure 2).

Both variants can be useful in simulating the analog signal chain from the DAC output buffer. The SPI model with the output buffer completely models the full DAC functionality. It can be used to simulate the digital signal chain from the DAC's input.

The output buffer model for the DAC includes common DC parameters such as end-point errors with respective temperature coefficients, quiescent current, as well as AC parameters such as capacitive load stability, slew rate, settling time, and power-on glitch, among others. For example, simulation results for DAC8411 gain (Gerr) and offset (Offs) error are shown in Figure 3. Note that the gain error is a percentage of the full-scale range, and the offset error is in microvolts (µV).

Figure 1. DAC parallel interface model

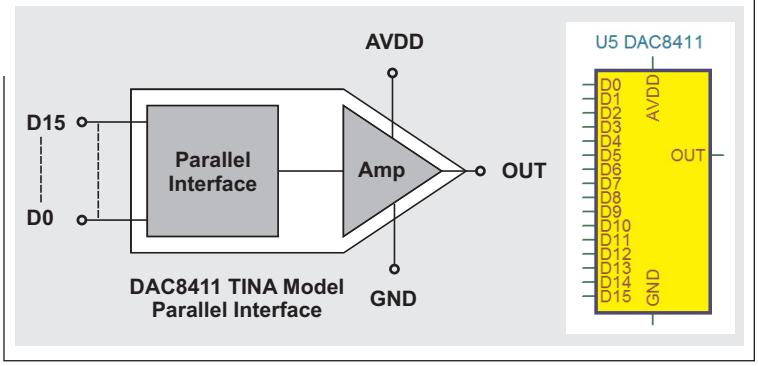


Figure 2. DAC serial interface model

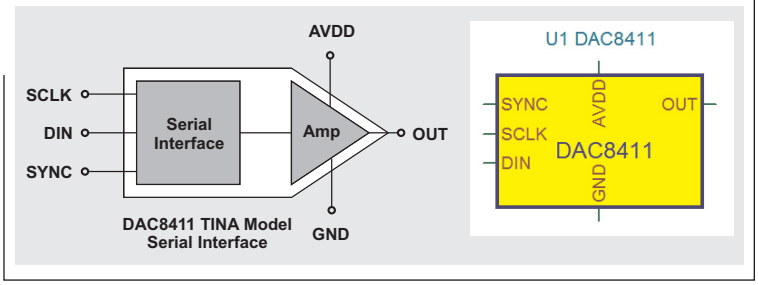


Figure 3. Gain and offset error DC simulations

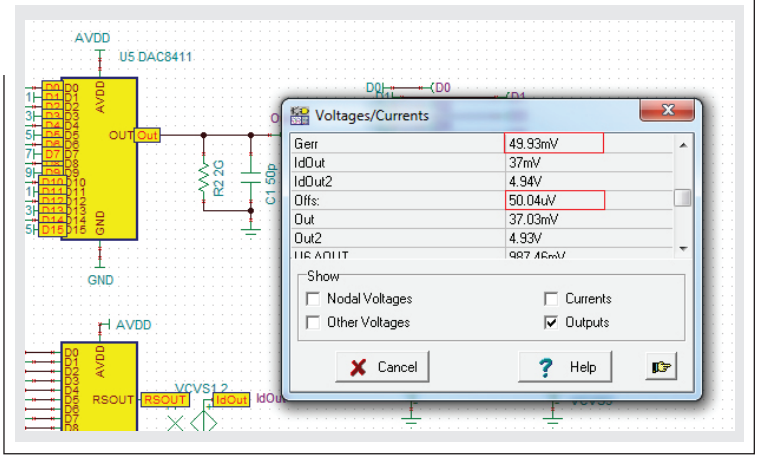


Figure 4 shows a transient simulation that was performed on the DAC with a code step from quarter to three-quarter scale. The plot shows close correlation of the simulated plot to the datasheet plot for this analysis.

The models also allow the designer to enter specific values for some parameters such as the DAC gain and offset errors. This is particularly useful in running what-if simulations for estimating system performance.

Bringing it together – complete system models

Case Study: 0- to 20-mA DAC

One of the most common DAC applications is to create a 0- to 20-mA signal in an industrial automation system, also known as a three-wire system. There are multiple ways to implement this system that range from a fully discrete implementation using a DAC, operations amplifiers, and passive components, to fully-integrated implementations using devices such as the DAC8760.

For this exercise, let's design a basic 0- to 20-mA system using a fully discrete implementation with TINA models for the DAC8411 and OPA192 (Figure 5).

Theory of operation

This implementation uses models for the DAC8411, two OPA192 operational amplifiers (OP1 and OP2), two MOS transistors (T1 and T2), and four resistors (R1, R2, R4, and RLOAD). This system generates an output load current into RLOAD that is proportional to a 16-bit input digital code. For this design, OP1 and OP2 are required to handle rail-to-rail inputs.

In order to understand this basic system, we will assume that OP1 and OP2 are ideal. However, subsequent sections use the OPA192 TINA models to simulate the complete system. The DAC8411 model converts the 16-bit DAC code into a proportional analog output voltage (VDAC) in the 0- to 5-V range. This voltage is then applied to the positive input of the operational amplifier (OP2). The negative input of OP2 is also driven to the DAC output voltage (VDAC), thus forcing a current through resistor R4 (VDAC/R4). The operational amplifier (OP2) ensures this current by controlling the gate voltage of MOSFET (T2). This current is drawn from the supply (V2) via resistor R1. This completes the first stage of this design in which a code proportional current is generated.

The operational amplifier (OP1) maintains equal voltage drops across R1 and R2. Since the value of R2 in this design is a 100 times less than R1, for an equal voltage drop, the current flowing through R2 must be a 100 times greater than the current flowing through R1. This current can be expressed by the formula (VDAC/R4) × (R1/R2).

The operational amplifier (OP1) ensures this current by controlling

Figure 4. Transient simulation showing half-scale settling time

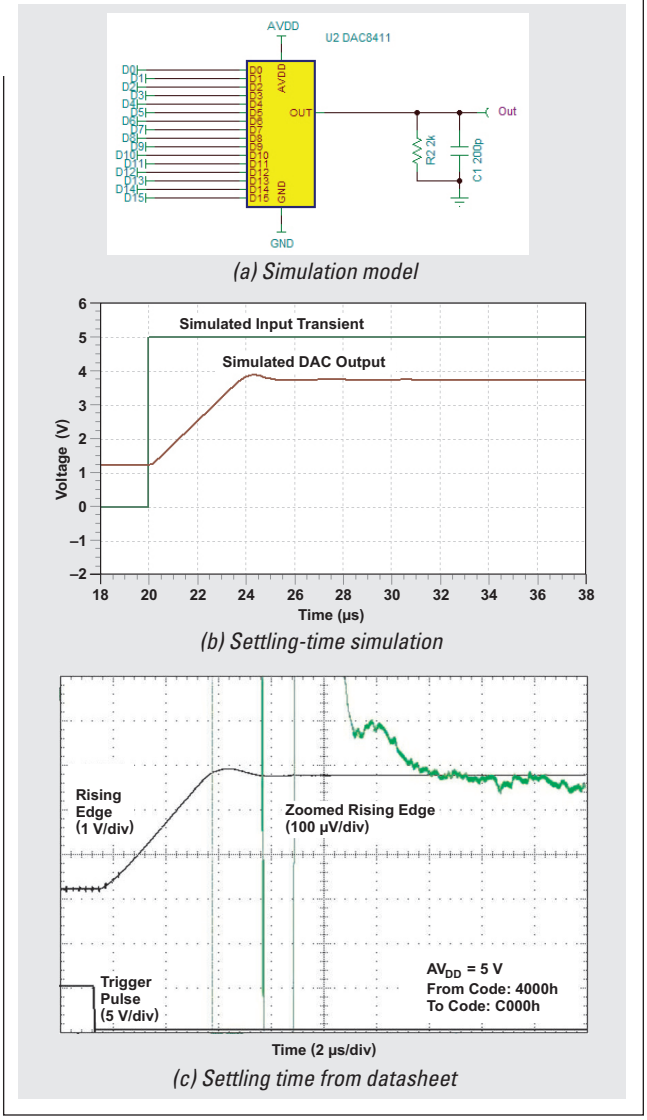


Figure 5. DAC 0- to 20-mA system model

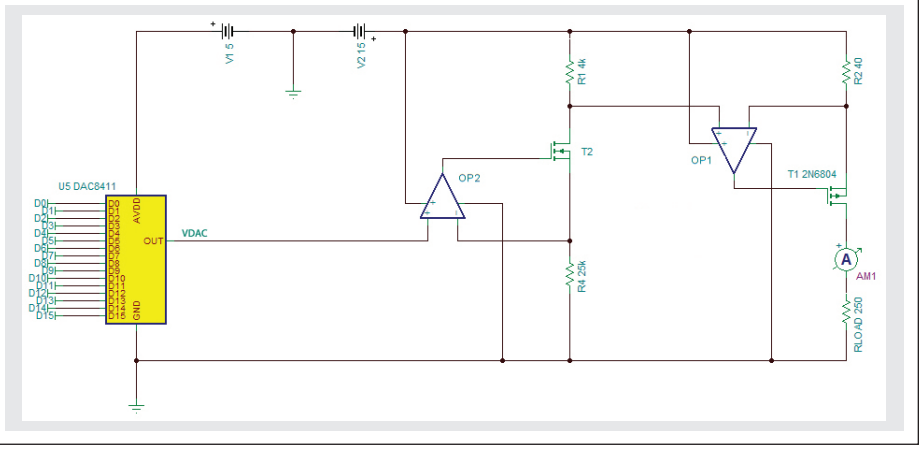
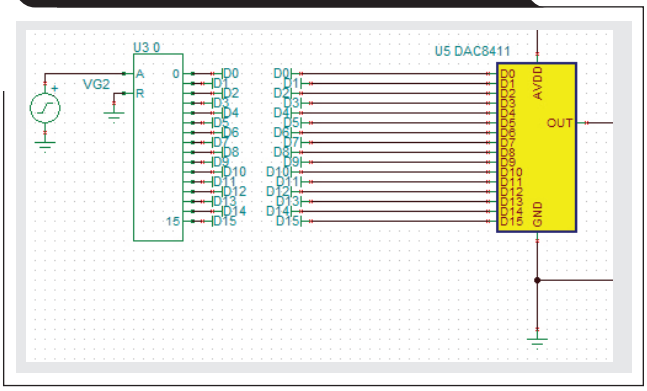


Figure 6. Input interface test bench for 0- to 20-mA DAC system



the gate of MOSFET T1. The drain of the T1 is connected to the 250-Ω load resistor (RLOAD) via an ammeter (AM1).

Simulation setup and results

The test-bench configuration shown in Figure 6 uses an ideal 16-bit analog-to-digital converter (ADC) to convert a 0- to 1-V analog signal (VG2) into the 16-bit code for the system. A DC sweep of VG2 generates full 16-bit code for the system. The resulting output current is shown in Figure 7.

Figure 8 shows a transient analysis for the same circuit. The DAC code is toggled from zero scale to full scale and the resulting output current is plotted.

Real system non-idealities

Previously, the 0- to 20-mA system was simulated with DAC8411 and OPA192 parameters modeled as typical. As with any integrated chip, the parameters listed in the datasheet have a typical value, and for some, a max/min value. The intent of placing these boundaries is to guarantee a level of performance on these parameters over a specified temperature range, supply voltages, and process variations. Thus, it is useful to have the system simulated for these variations in the specifications.

The latest TINA-TI software models for the DAC allow designers to modify some critical parameters and run what-if simulations. To illustrate this feature, an example simulation was chosen in which the DAC offset voltage is varied from a typical to the maximum value. This spec is captured in the models by the OFFS parameter shown in Figure 9.

Figure 7. DAC system simulation of output current DC sweep

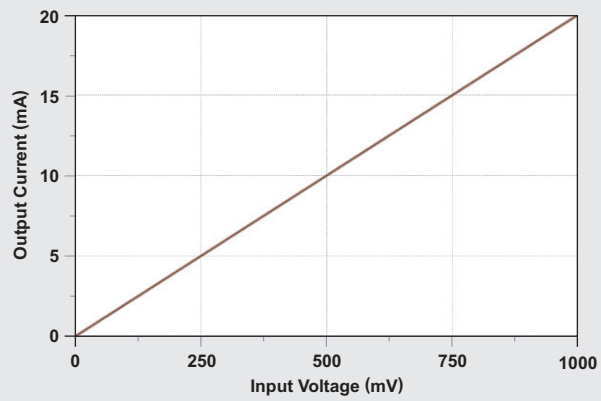


Figure 8. DAC system simulation of output current transient

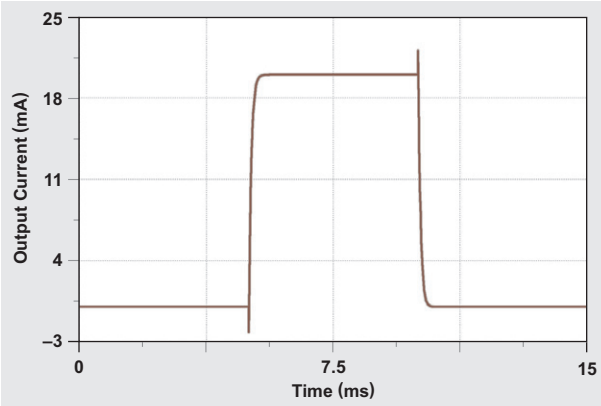


Figure 9. DAC model, user-adjustable DAC offset voltage

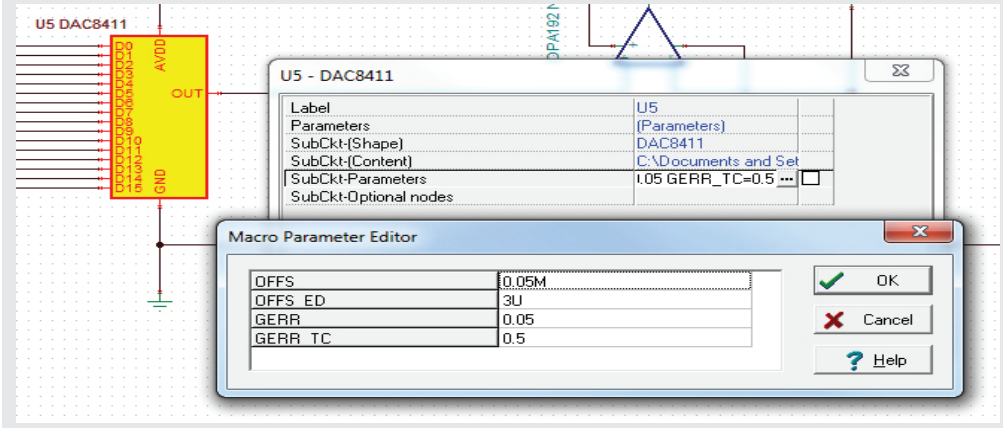
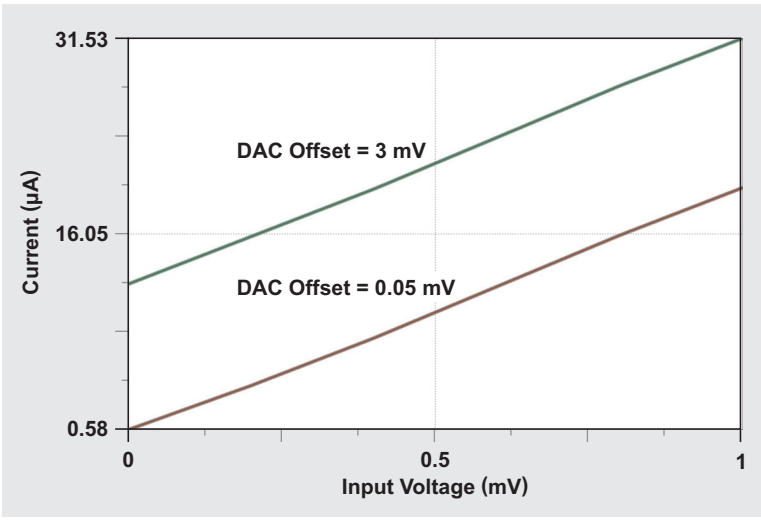


Figure 10 shows the system's DC performance (system output current of model in Figure 5) for two values of DAC offset voltage.

Note that the green curve is the simulation result with the worst-case offset voltage (3 mV), and the red curve is with offset voltage set to typical value of 0.05 mV. For simplicity, the displayed output current in Figure 10 is zoomed in to show the offset in the output. This particular simulation is useful to predict the response of the system for the worst-case DAC offset voltage.

Figure 10. DAC system simulation for output-current DC sweep with user-adjusted offset error



Conclusion

The DAC models described allow full system verification. However, the level of accuracy and system parameters that can be verified depend on the accuracy of the models as well as the capability of the simulation tool. Using the system shown in Figure 5 as an example, the level of verification depends on the DAC models, operational amplifiers, MOSFETs, and discrete components along with the capability of the TINA simulator. The simulator capability can be improved by using the professional version of the simulation software. This leaves the accuracy of the component models to be the limiting factor for comprehensiveness of the system verification.

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Isolated sensing systems with low power consumption

By Jose Duenas
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Applications Engineer

Current-shunt-monitor (CSM) ICs have been a mainstay in industrial applications for many years. Designed for either unidirectional or bidirectional current monitoring, CSMs offer excellent performance when used in either high-side or low-side current-shunt applications. However, many modern applications require some level of insulation to protect the end user from hazardous voltages.

The level of insulation that a particular circuit needs is driven mainly by the type of end equipment and where the end equipment will be deployed. For instance, is the end equipment a solar inverter to be mounted on a roof top or is it part of a servo motor drive used on an industrial robot? Global location of the end equipment plays a part as well. In the United States the Underwriters Laboratory (UL) maintains safety standards for various end-equipment. For Canada, it is the Canadian Standards Association (CSA). Europe has the International Electromechanical Commission (IEC) and the Association for Electrical, Electronic and Information Technologies (referred to as the VDE).

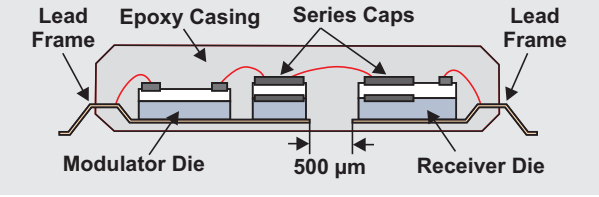
There are four main categories of insulation. The first is functional, which offers no protection against electric shock. As the name implies, functional insulation is provided to allow proper operation of a circuit or device. Think of this as the minimum trace spacing across a printed circuit board from a shunt resistor to the input terminals of the monitoring device.

The second level of insulation is basic. Basic insulation relates to the ability of an isolation device (an optocoupler or digital isolator, for example) to provide a level of protection against electric shock across an isolation barrier.

Next is supplemental or double insulation. This is an independent insulation layer that is applied in addition to basic insulation to ensure protection against electric shock in the event that the basic insulation fails. This is similar to adding a section of heat-shrink tubing over an input wiring harness. The fourth category is reinforced insulation. Reinforced insulation is a single insulation system that provides a level of protection against electric shock equal to double insulation.

For a typical insulation example, the AMC1305 is a precision, delta-sigma (ΔΣ) modulator with the output separated from the input circuitry by a capacitive isolation barrier that is highly resistant to magnetic interference. This barrier is certified to provide reinforced isolation of up to 7000 V_{PK}, according to the VDE V 0884-10, UL1577, and CSA standards. As shown in Figure 1, the isolation barrier of this device is constructed with two series capacitors, each having an equivalent of basic insulation through a silicon dioxide (SiO_2) layer of 13.5 µm (27 µm total). The surge immunity is rated to ±10,000 V and the working voltage is 1500 VDC and 1000 V_{RMS}, respectively.

Figure 1. Example of the dual-capacitor isolation barrier



Unlike traditional CSM devices that provide an analog output, the AMC1305 provides a digital bit stream. The differential analog input is a switched-capacitor circuit feeding a second-order delta-sigma modulator stage that digitizes the input signal into a 1-bit output stream. The converter's isolated output (DOUT) provides a digital bit-stream of ones and zeroes that are synchronous to an externally provided clock source at the CLKIN pin. The output bit-stream can be fed directly to the SD-24B module of an MSP430™ microcontroller (MCU) or the sigma-delta filter module (SDFM) of a C2000™ Delfino™ TMS320F2837x MCU.

In addition to dictating the level of isolation required, the type of application determines how many currents and voltages need to be monitored. In many cases, the variables of a polyphase system are monitored. One of the most common types of polyphase system is the three-phase case. Typically, three currents and three voltages could be measured in three-phase systems, and sometimes a fourth voltage is measured, primarily in cases where a connection to neutral or ground is available.

Supplying power to the sensing circuitry is greatly simplified when the variables measured in a polyphase system have low common-mode voltages with respect to a common reference point. This could be the case when performing low-side current measurements and voltage measurements using resistive dividers. However, many systems require measuring currents and voltages that can

have significantly different common-mode components. In such cases, isolated power supplies are required and the design becomes a bit more complex.

Consider the system depicted in Figure 2. There are seven circuit functions that could be monitored: Three line currents, three phase-to-phase voltages and one common-to-ground voltage. For simplicity, only three current shunts (R_S) are depicted and the divider circuits for voltage measurement are not shown.

Depending upon which power transistors (elements labeled 1 through 6) are conducting, the common-mode voltage of the shunt resistors can be either near the full DC-Link voltage or near ground potential.

In order to take advantage of a design using isolated delta-sigma modulators, each of the seven monitoring circuits require a separate isolated power supply for the high side of the delta-sigma modulators. The term "high side" is often used to refer to the analog input side of the galvanic isolation barrier.

For example, in a system with a 48-V DC-Link voltage, one approach to design the required power supply could start by producing 3.3 VDC from the 48-VDC source with a buck-bias, step-down switching regulator (Figure 3). Figure 4 shows how a second stage could generate an isolated 5-VDC supply from the 3.3-VDC supply with a small isolation transformer in conjunction with a transformer driver.

Figure 2. Example of a polyphase system with current shunts (R_S)

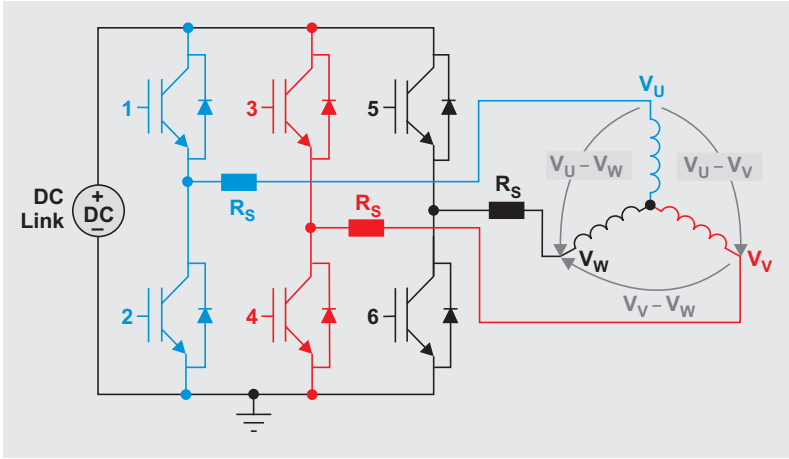


Figure 3. Step-down switching regulator design

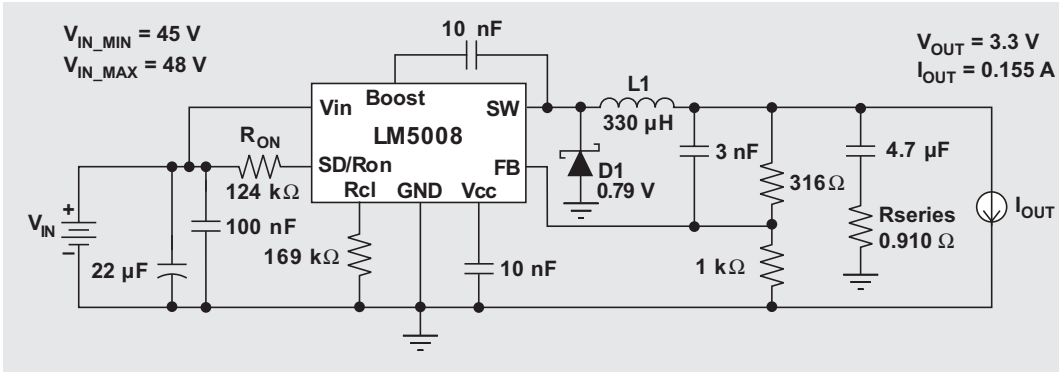


Figure 4. Isolated 5-VDC supply from 3.3 VDC

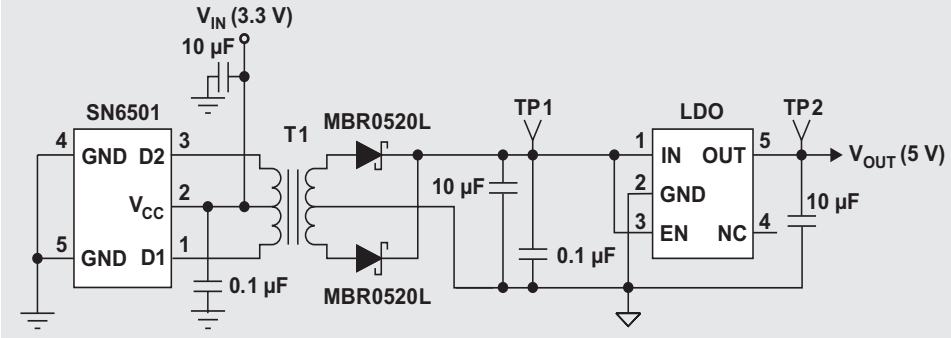


Table 1. A comparison between two acquisition systems based on isolated delta-sigma modulators

ISOLATED DELTA-SIGMA MODULATOR	IAVDD (max) (mA)	UNITS PER SYSTEM	SUM OF CURRENTS REQUIRED IN THE 5-VDC BUSES (mA)	EFFICIENCY OF THE 3.3-VDC TO 5-VDC STAGE (%)	POWER REQUIRED ON THE 3.3-V BUS (W)	CURRENT REQUIRED FROM THE 3.3-V BUS (A)*	POWER DRAWN FROM THE 48-VDC BUS (W)
AMC1305	7	7	49	54	0.45	0.155	0.69
Alternative Device	36	7	252	74	1.7	0.57	2.27

* An additional 10% to 12% margin has been added to the current requirement.

Table 1 compares two scenarios. In one scenario, seven AMC1305 units were used for monitoring. Figures 3 and 4 show the circuits that fulfilled the power requirements for the design with seven AMC1305 devices. The second scenario used an alternative device for the delta-sigma modulator and different components were used for the 48-V to 3.3-V power section.

The alternative-device scenario shows the implications of using seven units of a device that has higher power consumption on its analog input side (high side).

TI's family of isolated delta-sigma modulators includes some components with a specified input range of ±250 mV and others of ±50 mV. Compared to devices with a higher input range, devices with a lower input range allow system designers to reduce power dissipation in the sensing-current shunt by 80%.

Using a low-power, isolated-sensing solution brings about more efficient acquisition systems (from an energy point of view) as well as better performance. The greatest impact that higher power consumption can have in the acquisition system's performance is in gain-error drift and offset-error drift. An isolated delta-sigma modulator with higher power consumption is bound to experience a higher internal temperature rise during normal operation. Moreover, the ambient temperature of the isolated delta-sigma modulator is bound to be higher for systems with power-management circuitry that is tasked to deliver more than three times more power. The combination of higher internal and ambient temperatures in systems with higher power consumption yields solutions with more errors and poorer signal-to-noise ratio (SNR).

The best-in-class drift performance provided by the AMC1305 reduces temperature dependency and yields higher system performance over a wider temperature range. Also, gain-error drift is cut by as much as 58% and offset drift by 74% when compared to the closest competitor.

Conclusion

Many modern applications require isolation. The specific isolation level needed is driven by the type of end equipment in question and the regulatory body certifying the equipment.

Although power consumption is sometimes neglected as a key design criterion, the performance and efficiency of isolated sensing systems can be greatly improved by carefully selecting devices that have high-precision, isolated front-ends with optimized power-consumption specifications, such as the TI family of AMC1305 products.

Related Web sites

www.ti.com/4q14-AMC1305L25

www.ti.com/4q14-AMC1305M25

www.ti.com/4q14-AMC1305M05

C2000™ Delfino™ MCU
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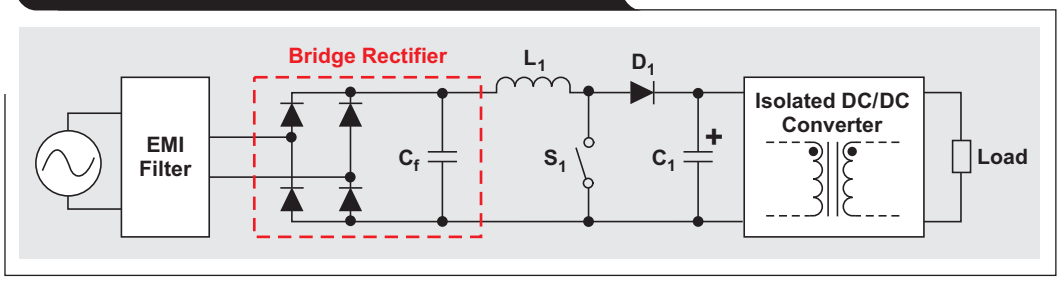
Design a transition-mode, bridgeless PFC with a standard PFC controller

By Sheng-Yang Yu
Application Engineer, Power Design Services

Figure 1. Conventional two-stage power-supply system with high power-factor requirements



Introduction

This article presents design information for using a standard, low-cost, power factor correction (PFC) controller to construct a high-efficiency transition-mode (TM) bridgeless-PFC power supply. Driven by the Northwest Energy Efficiency Alliance's 80 PLUS® program,[1] computer power-supply manufacturers are eager to investigate ways to improve converter efficiency. A standard power-supply system with high power-factor requirements is shown in Figure 1.

The rectified input voltage is boosted to a level higher than the maximum input to ensure that a high power factor is achieved over the whole input range. After the boost PFC, an isolated DC/DC converter steps the boost voltage down through a safety isolated transformer. For a two-stage power supply with 400-W output power, power dissipation of the bridge diodes could go up to 6 W with a full load and the input at 120 VAC/60 Hz. That is a 1.5% efficiency reduction just because of the power dissipation by the bridge diodes. As a result, bridgeless PFCs[2] (a combination of rectifier and boost converters) replace conventional PFCs for better converter efficiency. However, the complexity of bridgeless-PFC control makes its controller more expensive than a standard analog-PFC controller. Additionally, the parasitic capacitance on the bridgeless-PFC MOSFETs creates more electromagnetic interference (EMI) than the conventional PFC.[3]

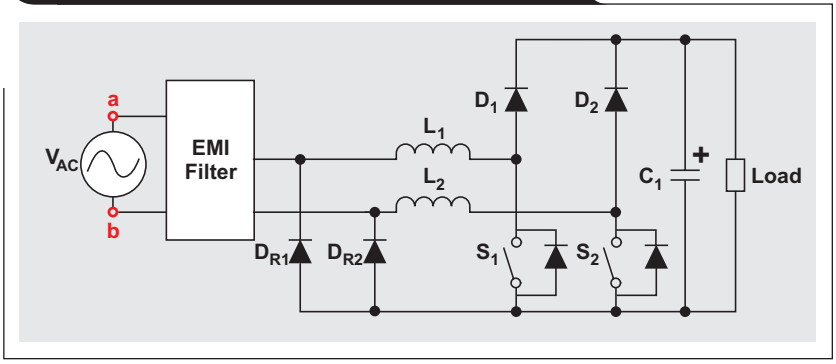
The aforementioned issues greatly increase the cost of a bridgeless PFC circuit. An alternative bridgeless PFC with return diodes[4] is shown in Figure 2.

Slow-recovery return diodes, D_{R1} and D_{R2} in Figure 2, alleviate EMI concerns. Moreover, the same pulse-width modulation (PWM) signal can be used to drive both MOSFETs, which greatly reduces control complexity and controller cost.

This article focuses on the design considerations of using low-cost standard analog-PFC controllers for TM-bridgeless PFCs with return diodes. Two 370-W reference boards were built for performance evaluations with the UCC28051 TM-PFC controller; a TM-bridgeless PFC and a TM-conventional PFC. The results show that over 97% efficiency can be achieved with the TM-bridgeless PFC prototype at 120 VAC, which is about 1% higher than that of the TM-conventional PFC prototype.

Digital controllers such as TI's C2000™ real-time microcontrollers[5] are also widely used for controlling bridgeless PFCs.

Figure 2. Bridgeless PFC with return diodes

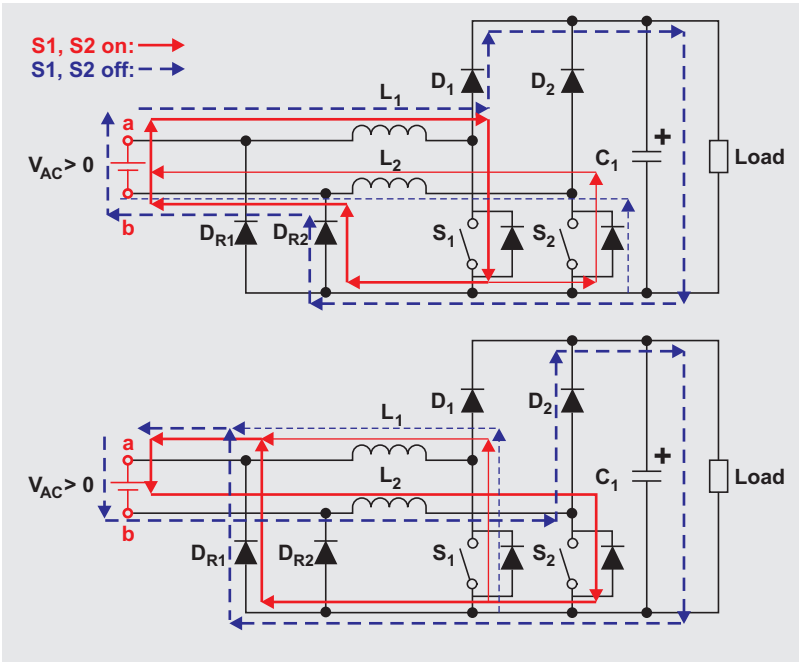


Circuit operations and design considerations

Circuit operations

The circuit operations of a TM-bridgeless PFC, shown in Figure 3, are similar to a boost converter. When $V_{AC} > 0$ (or $V_a - V_b > 0$), the main currents flow through the first boost converter components, L_1, S_1, D_1, C_1 and the load, then back to the source through D_{R2}. When $V_{AC} < 0$ (or $V_a - V_b < 0$), the main currents flow through the second boost converter components, L_2, S_2, D_2, C_1 and the load, then back to the source through D_{R1}. The return diodes allow both switches S_1 and S_2 to be on and off at the same time to keep the boost converters operating normally.

Figure 3. Operations of bridgeless PFC with return diodes



Design considerations

A standard TM-PFC controller relies on the sensing results of current-sensing and zero-current-detection (ZCD) circuits as the on/off trigger of the driving signal. A current-sensing circuit is used to detect the peak value of the inductor current to turn off the switch. A ZCD circuit detects the zero-current point of the inductor current to turn on the switch.

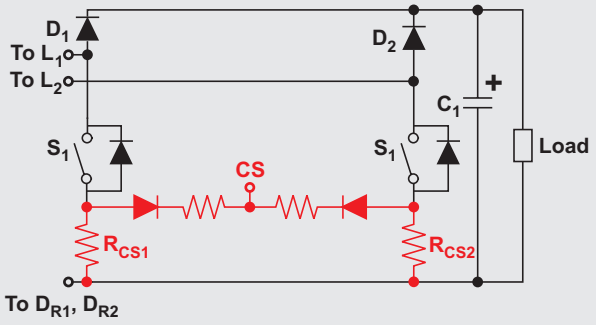
Another characteristic of a standard TM-PFC controller is that the switching-frequency range is much narrower than costly digital controllers. It is important to properly design the PFC inductors because they determine the switching frequency. There are three key considerations when applying a standard TM-PFC controller to the TM-bridgeless PFC: Current-sensing circuit design, ZCD design, and PFC-inductor design.

Current-sensing design

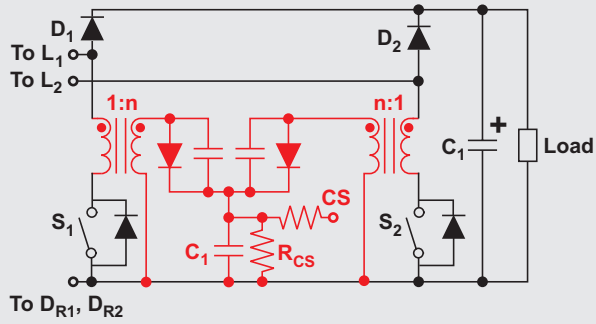
Power resistors for a peak current-sensing circuit (R_{CS1} and R_{CS2} in Figure 4a) are no longer the first choice for bridgeless-PFC current sensing. This is mainly because there are two switch legs to be sensed. If each switch is in series with a current-sensing resistor, then additional circuitry is needed to be sure the controller receives the current-sensing signal from the desired switch leg. Because these circuits generally require higher current-sensing resistance, higher power losses occur with current-sensing resistors. Higher resistance is needed for R_{CS1} and R_{CS2} because of the diode voltage drop.

Instead of using current-sensing resistors, current transformers for current sensing are suggested as shown in Figure 4b. Diodes in the current-sensing circuit with current transformers ensure that peak-current from the desired switching leg is detected and also minimize power losses in the current-sensing circuit.

Figure 4. Current-sensing circuits



(a) Sensing with power resistors



(b) Sensing with current transformers

Zero-current-detection design

In a standard TM-boost PFC, ZCD is achieved by detecting the voltage signal from an auxiliary winding of the PFC inductor (Figure 5a). This ZCD circuit uses the inductor's voltage-second characteristic. When boost diode D_1 is conducting, positive voltage appears at the IC's ZCD pin. Also, with a proper turns-ratio design of L_1, V_{ZCD} is greater than V_{REF}. Once the inductor current decreases to zero, the inductor's voltage changes its polarity. Now the ZCD voltage changes from positive ($V_{ZCD} > V_{REF}$) to negative ($V_{ZCD} < V_{REF}$). This voltage polarity-changing transient is detected by the internal comparator and pulls the driving signal high to turn on S_1.

When using a TM-bridgeless PFC, all zero-current events must be detected. It may be necessary to apply the ZCD circuit for a TM-boost PFC to both inductors in the TM-bridgeless PFC and include blocking diodes. However, blocking diodes extend the V_{ZCD} falling duration and make the ZCD pin sensitive to noise, which causes incorrect trigger and protection. Instead of using the inductor auxiliary winding, a series-connected RC circuit (Figure 5b) provides a simple detection option.

When both S_1 and S_2 are turned off, there is still one switch (generally MOSFET) conducting current through its body diode. Hence, a voltage difference is created between the two switch legs. The capacitors in the ZCD circuit are charged and result in $V_{ZCD} > V_{REF}$. The voltage difference becomes zero when the inductor current goes to zero, which makes $V_{ZCD} < V_{REF}$ and triggers the turn-on event. In short, this circuit uses the capacitor charge/discharge to achieve ZCD.

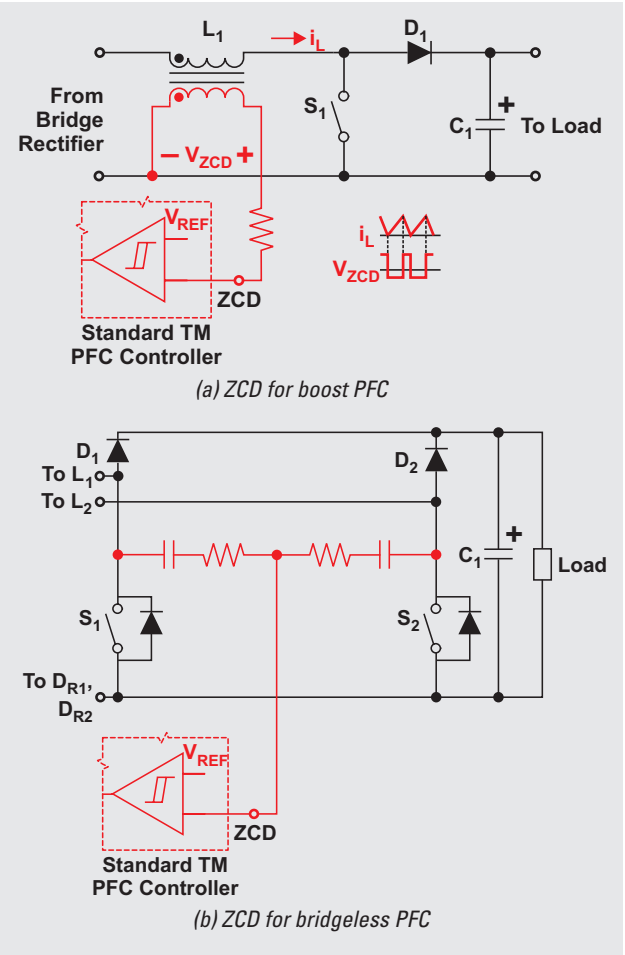
PFC inductor design

Unlike a continuous-conduction-mode (CCM) PFC circuit, a TM PFC requires various switching frequencies in an AC cycle to ensure that the inductor current is discharged to zero before the next switching cycle begins. Generally, an analog TM-PFC controller has a narrower operational frequency range than a digital controller. Therefore, choosing the proper inductance for the boost inductors in the TM-bridgeless PFC becomes an important task to ensure that the switching frequencies are within the IC limits in most conditions. The inductor value can be calculated.

$$L_1 = \frac{V_{in\_min(rms)}}{2I_{in(rms)}\left[\text{at } V_{in\_min(rms)}\right]} \times t_{on\_max} = \frac{V_{in\_min(rms)}}{2I_{in(rms)}\left[\text{at } V_{in\_min(rms)}\right]} \times \frac{V_{out} - \sqrt{2} \times V_{in\_min(rms)}}{V_{out} \times f_{sw\_min}} \quad (1)$$

where t_{on_max} is the maximum on time of switches S_1 and S_2 at the minimum input voltage (V_{in_min}), and f_{sw_min} is the minimum switching frequency at V_{in_min}. The rms value of the input current ($I_{in(rms)}$), can be determined by $I_{in(rms)} = P_{out}/(V_{in(rms)} \times \eta)$, where η is the PFC efficiency.

Figure 5. Zero current detection circuits



Once inductance is determined, the converter switching frequencies over an AC switching period with a fixed-input AC voltage can be found.

$$f_i = \frac{D_i}{t_{on}} = \frac{V_{out} - \left|\sqrt{2} \times V_{in(rms)} \times \sin\left(\omega_{AC} x_i\right)\right|}{V_{out} \times t_{on}} \quad (2)$$

where D_i is the duty cycle in the i-th switching action, $\omega_{AC} = 2\pi f_{AC}$ and f_{AC} is the AC switching frequency. The time that the i-th switching begins is x_i, so with $x_1 = 0$, x_{i+1} can be determined.

$$x_{i+1} = \sum_{j=1}^{i} \frac{t_{on}}{D_j} \quad (3)$$

Now consider a TM-bridgeless PFC with a 380-V output voltage, 380-W output power, and universal AC input range of 90 to 264 VAC. With f_{sw_min} set to be 65 kHz and η assumed to be 96%, the inductance can be calculated as 104 µH with Equation 1. Now apply equations 2 and 3 with

the calculated inductance. The switching frequency variations at 120 VAC and 240 VAC are shown in Figure 6. The results show that a high power factor can be ensured in both low-line and high-line inputs for this design ($f_{sw\_max} \cong 400$ kHz) because the switching frequencies during high-current operation are all below the controller's frequency limitation.

Circuit implementation and experimental verifications

Two 380-W, TM-PFC reference boards (conventional-boost and bridgeless) were built to compare performance. For boost switches, an N-channel MOSFET with $R_{DS(on)}$ = 140 mΩ was used for the boost PFC and N-channel MOSFETs with $R_{DS(on)}$ = 199 mΩ were used for the bridgeless PFC. The UCC28051 TM-PFC controller and inductors with a PQ3220 ferrite core were applied to both reference boards. Note that two 260-µH inductors were connected in parallel for the boost PFC reference board to share the magnetic flux density and power losses on the boost inductor. Two 100-µH inductors were used as boost inductors in the bridgeless-PFC reference board. Identical low-cost bridge diodes were used for the rectifier in the conventional-boost PFC and for the return diodes in the bridgeless PFC. Current sensing with current transformers and a RC-connected ZCD circuit was applied to the bridgeless-PFC reference board.

Inductor current waveforms of the TM-bridgeless PFC are shown in Figure 7. Notice that when one inductor processes a switching operation, the other inductor conducts negative current. This is because the inductance of the boost inductors is very low at the 50-/60-Hz frequencies. Therefore, part of the return current flows back to the source through the boost inductors instead of the return diodes.

Figure 6. Switching frequencies of TM-bridgeless PFC over a half AC cycle

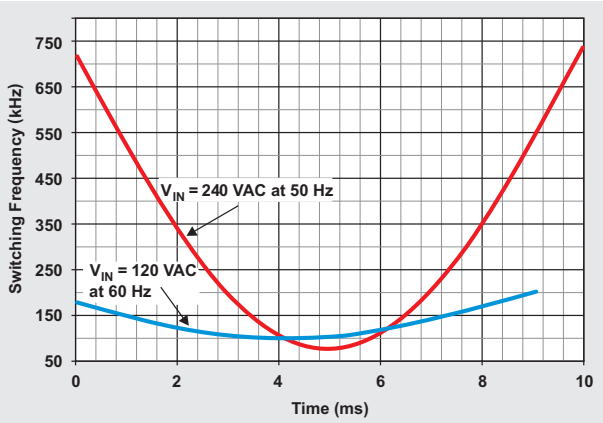


Figure 7. Inductor current of TM-bridgeless PFC at 350-W output

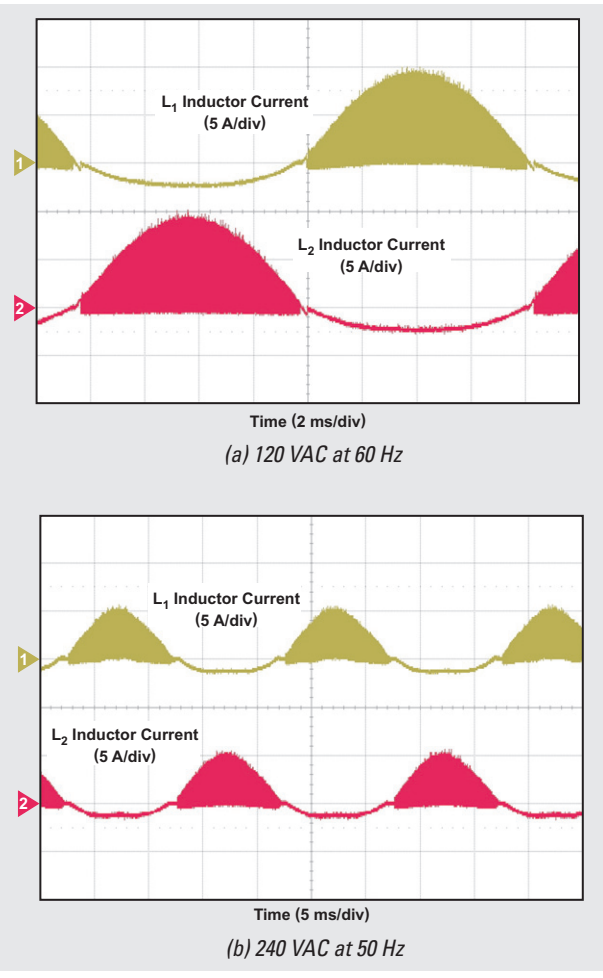


Figure 8 compares the efficiency of these two prototypes. In the light- to mid-load range, an efficiency improvement of approximate 1% was noted for the TM-bridgeless PFC compared to the boost PFC. The power-factor measurements of the prototypes are shown in Figure 9. The high power factor was obtained for both 120 VAC and 240 VAC, which verifies the previous analysis.

Conclusion

Design considerations of a low-cost TM-bridgeless PFC show that standard PFC controllers can be used to greatly reduce overall circuit cost while keeping the advantages of a bridgeless PFC circuit. Experimental comparisons to the conventional TM PFC show strong evidence of efficiency improvement with the TM-bridgeless PFC.

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Figure 8. Converter efficiencies for reference boards

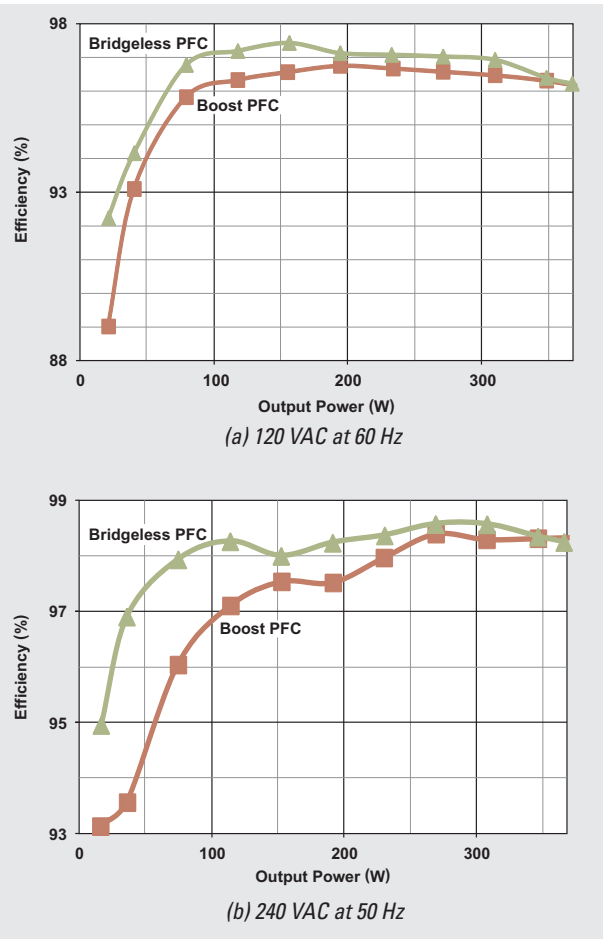
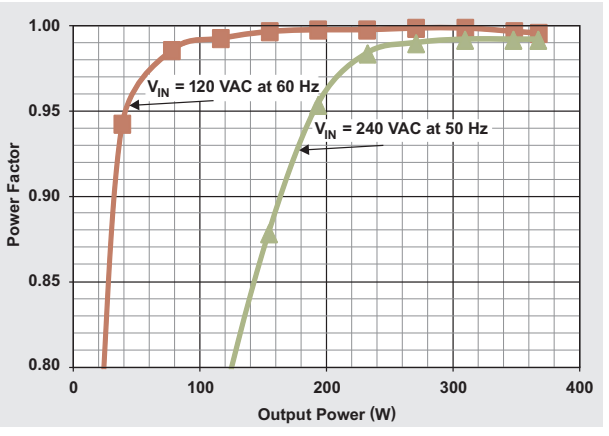


Figure 9. Power factor for TM-bridgeless PFC



Power-supply sequencing for FPGAs

By Sami Sirhan
Analog Systems Engineering
Sureena Gupta
Applications Engineer

Introduction

Power-supply sequencing is an important aspect to consider when designing with a field programmable gate array (FPGA). Typically, FPGA vendors specify power-sequencing requirements because an FPGA can require anywhere from three to over ten rails.

By following the recommended power sequence, excessive current draw during startup can be avoided, which in turn prevents damage to devices. Sequencing the power supplies in a system can be accomplished in several ways. This article elaborates on sequencing solutions that can be implemented based on the level of sophistication needed by a system.

Sequencing solutions addressed in this article are:

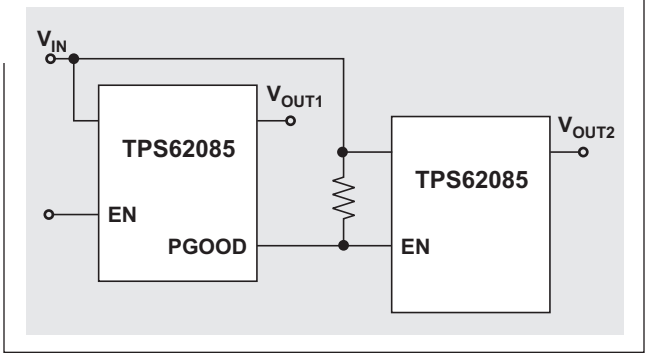
1. Cascading PGOOD pin into enable pin
2. Sequencing using a reset IC
3. Analog up/down sequencers
4. Digital system health monitors with PMBus interface

Method 1: Cascading PGOOD pin into enable pin

A basic, cost-effective way to implement sequencing is to cascade the power good (PG) pin of one power supply into the enable (EN) pin of the next sequential supply (Figure 1). The second supply begins to turn on when the PG threshold is met, usually when the supply is at 90% of its final value. This method offers a low-cost approach, but timing cannot be easily controlled. Adding a capacitor to the EN pin can introduce timing delays between stages. However, this method is unreliable during temperature variations and repeated power cycling.

Also, this method does not support power-down sequencing.

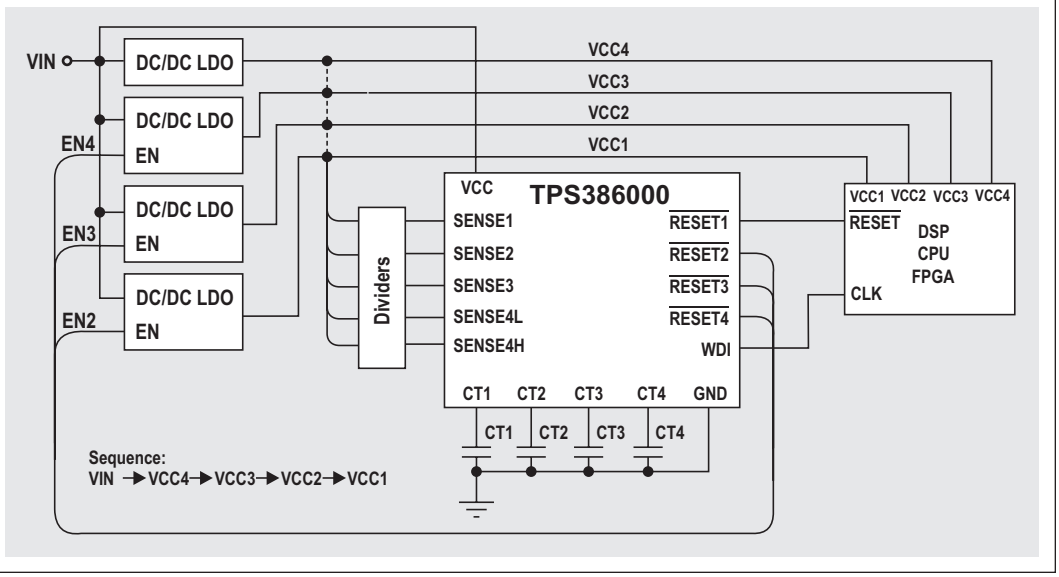
Figure 1. Cascading PGOOD pin into enable pin



Method 2: Sequencing using a reset IC

Another simple option to consider for power-up sequencing is a reset IC with time delay. With this option, the reset IC monitors the power rails with tight threshold limits. Once the power rail is within 3% or less of its final value, the reset IC enters the wait period defined by the solution before powering up the next rail. The wait period can be programmed into the reset IC using EEPROM or be set by external capacitors. A typical multi-channel reset IC is shown in Figure 2. The advantage of using a reset IC for power-up sequencing is that the solution is monitored.

Figure 2. Power-up sequencing with a multi-output reset IC



Each rail is confirmed to be within regulation before releasing the next rail and there is no need for a PGOOD pin on the power converter. The drawback of using a reset-IC solution for sequencing is that it does not implement power-down sequencing.

Method 3: Analog up/down sequencers

Implementing power-up sequencing can be easier than implementing power-down sequencing. To achieve power-up and power-down sequencing, there are simple analog sequencers (Figure 3) that can reverse (Sequence 1) or even mix (Sequence 2) the power-down sequence relative to the power-up sequence. Upon power up, all the flags are held low until EN is pulled high. After EN is asserted, each flag goes open drain (pull-up resistor is required) sequentially after an internal timer has elapsed. The power-down sequence is the same as power up, but in reverse order.

Cascading multiple sequencers

Sequencers can be cascaded together to support many power rails, as well as provide fixed and adjustable delay times between enable signals. In Figure 4, two sequencers cascade together to achieve six sequenced rails. Upon power up, the AND gate ensures that the second sequencer does not trigger until it has received both an EN signal and rail C has triggered. On power down, the AND gate ensures that the second sequencer sees the EN falling edge, irrespective of output C. The OR gate ensures that the first sequencer is triggered with the EN rising edge. Upon power down, the OR gate ensures that the first sequencer can't see the EN falling edge until D has fallen. This guarantees power-up and power-down sequencing, but does not offer a monitored sequence.

Monitored up/down sequencing

Monitored sequencing can be added to the circuit in Figure 4 by simply adding a couple of AND gates between the FlagX output and the PG pin as shown in Figure 5. In this example, PS2 is enabled only if PS1 is greater than 90% of its final value. This method offers a low-cost, monitored sequencing solution.

Method 4: Digital system health monitors with PMBus interface

If a system requires the utmost flexibility, a good solution is a PMBus/I²C-compatible, digital-system health monitor such as the UCD90120A. Such solutions offer maximum control for any sequencing need by allowing the designer to configure ramp up/down times, on/off delays, sequence dependencies, and even voltage and current monitoring.

Figure 3. Implementation of an analog up/down sequencer

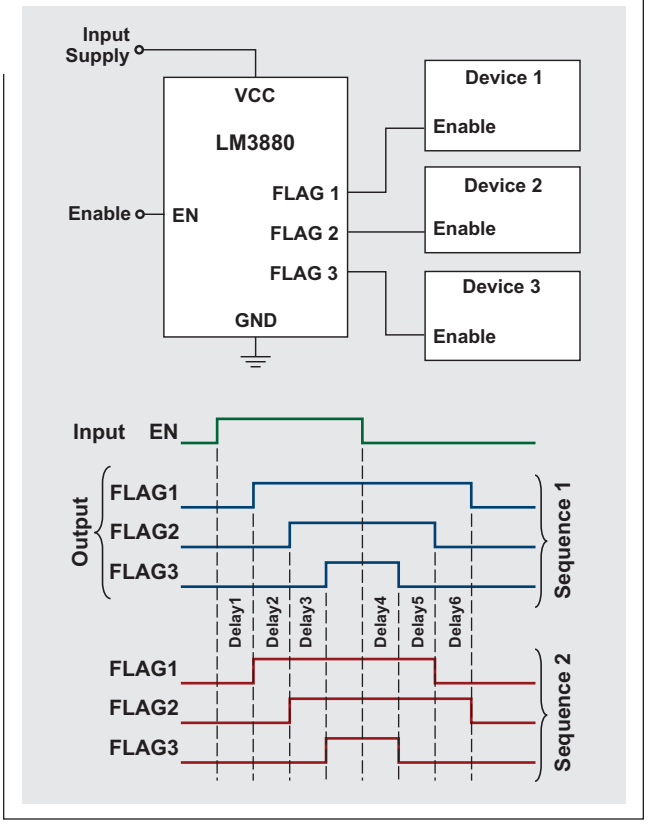


Figure 4. Cascading multiple analog sequencers

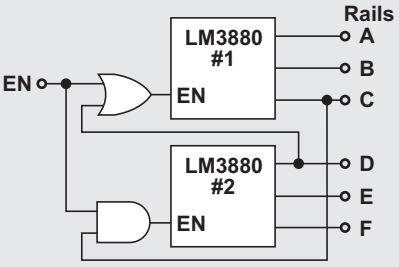


Figure 5. Adding monitored sequencing to a simple time-based sequencer

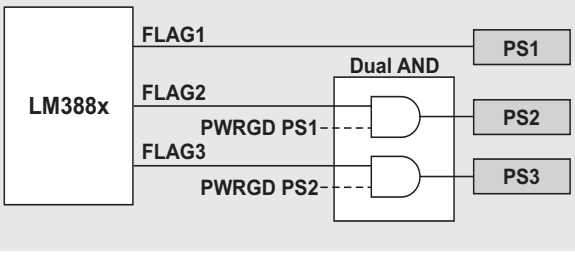
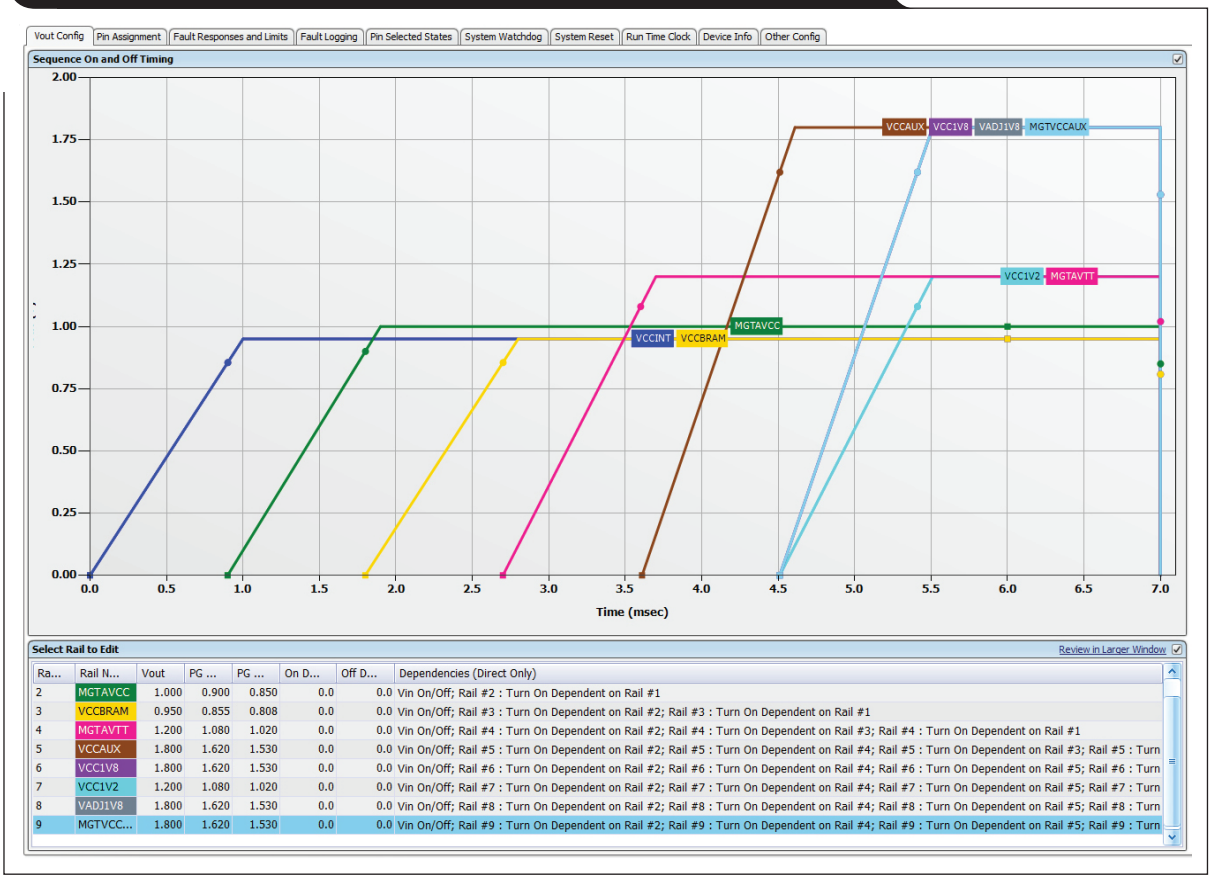


Figure 6. Example of power up sequencing using the UCD90120A GUI



Ra...	Rail N...	Vout	PG ...	PG ...	On D...	Off D...	Dependencies (Direct Only)
2	MGTAVCC	1.000	0.900	0.850	0.0	0.0	Vin On/Off; Rail #2 : Turn On Dependent on Rail #1
3	VCCBRAM	0.950	0.855	0.808	0.0	0.0	Vin On/Off; Rail #3 : Turn On Dependent on Rail #2; Rail #3 : Turn On Dependent on Rail #1
4	MGTAVTT	1.200	1.080	1.020	0.0	0.0	Vin On/Off; Rail #4 : Turn On Dependent on Rail #2; Rail #4 : Turn On Dependent on Rail #3; Rail #4 : Turn On Dependent on Rail #1
5	VCCAUX	1.800	1.620	1.530	0.0	0.0	Vin On/Off; Rail #5 : Turn On Dependent on Rail #2; Rail #5 : Turn On Dependent on Rail #4; Rail #5 : Turn On Dependent on Rail #3; Rail #5 : Turn
6	VCC1V8	1.800	1.620	1.530	0.0	0.0	Vin On/Off; Rail #6 : Turn On Dependent on Rail #2; Rail #6 : Turn On Dependent on Rail #4; Rail #6 : Turn On Dependent on Rail #5; Rail #6 : Turn
7	VCC1V2	1.200	1.080	1.020	0.0	0.0	Vin On/Off; Rail #7 : Turn On Dependent on Rail #2; Rail #7 : Turn On Dependent on Rail #4; Rail #7 : Turn On Dependent on Rail #5; Rail #7 : Turn
8	VADJ1V8	1.800	1.620	1.530	0.0	0.0	Vin On/Off; Rail #8 : Turn On Dependent on Rail #2; Rail #8 : Turn On Dependent on Rail #4; Rail #8 : Turn On Dependent on Rail #5; Rail #8 : Turn
9	MGTVCC...	1.800	1.620	1.530	0.0	0.0	Vin On/Off; Rail #9 : Turn On Dependent on Rail #2; Rail #9 : Turn On Dependent on Rail #4; Rail #9 : Turn On Dependent on Rail #5; Rail #9 : Turn

Digital-system health monitors come with a graphical user interface (GUI) that can be used to program power-up and power-down sequencing along with other system parameters (Figure 6). Some digital system health monitors also have non-volatile-error and peak-value logging that helps with system-failure analysis in case of a brown-out event.

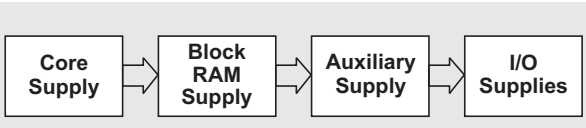
FPGA sequencing requirements examples

FPGA vendors such as Xilinx or Altera provide either a recommended or required power-up sequence in their datasheets that are easily accessible online. Sequencing requirements vary between vendors and vary from one vendor's FPGA family to another. Also listed in datasheets are timing requirements for ramp-up and shutdown. The recommended power-down sequence is typically the reverse order of the power-up sequence. An example of power-up sequencing is shown in Figure 7.

Conclusion

There are several sequencing solutions that can be utilized to follow the requirements specified by FPGA vendors. System requirements may include power monitoring in addition to power-up and power-down sequencing, but the optimal power solution for an FPGA will depend on system complexity and specifications.

Figure 7. Example of a FPGA power-logic sequence



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