# High-efficiency, low-ripple DCS-Control™ offers seamless PWM/power-save transitions

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Texas Instruments (TI) offers synchronous buck converters with DCS-Control™ technology, a regulation topology of Direct Control with Seamless transition into power-save mode. This topology incorporates the advantages of the voltage-mode, current-mode, and hysteretic control topologies while providing a clean entry into power-save mode. This article discusses how the DCS-Control topology works, demonstrating its low output-voltage ripple in power-save mode, its superb transient response, and its seamless mode transitions. These performance attributes cleanly power processors, FPGAs, radios, and other dynamic loads in PLC systems, motor control, industrial PCs, smartphones and solid-state drives (SSDs).

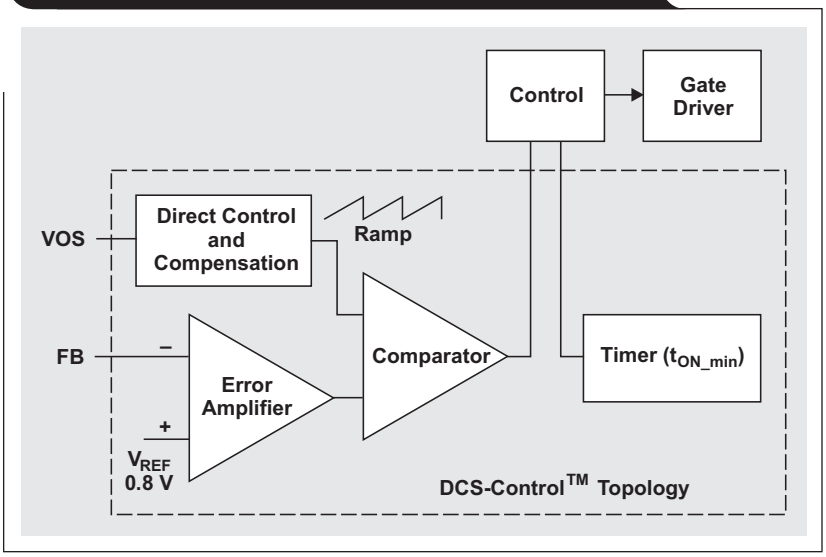
## Basic operation

The DCS-Control topology fundamentally is a hysteretic topology. However, it incorporates several circuits that provide the advantages of the voltage- and current-mode topologies. Figure 1 shows the basic block diagram of the DCS-Control topology, taken from the datasheet of TI's TPS62130 step-down converter.[1]

There are two inputs to the DCS-Control topology: a feedback (FB) pin and an output-voltage sense (VOS) pin. The FB pin's input behaves the same as in most DC/DC converters. It is the high-impedance input to an error amplifier, or operational amplifier, whose purpose is to output an error signal of the FB pin to an internal reference voltage, $V_{REF}$. As in other DC/DC converters, the error amplifier provides precise output-voltage regulation. A voltage divider between the output voltage, FB pin, and ground programs the output voltage's set point. For some devices, like TI's TPS62131, the FB pin is connected internally by using a voltage divider from the VOS pin. This sets the output voltage, reduces the external component count by two, and reduces the FB pin's sensitivity. Appropriate compensation is included around the error amplifier to ensure its stability.

The VOS pin is connected directly to the converter's output voltage at the output capacitor. Like the FB pin, this is a high-impedance input into the control loop. Unlike the FB pin, the VOS pin enters a proprietary circuit, which creates a voltage ramp. This ramp is then compared to the error signal from the error amplifier, as in voltage- or current-mode control. This path from the VOS pin to the comparator provides the fast hysteretic response of the DCS-Control topology. Changes in the output voltage at VOS are directly fed to the comparator and immediately affect the device's operation. For this reason, the VOS pin is noise-sensitive; so the output voltage's route should be as short and direct as possible from the output capacitor back to the device's VOS pin. Appropriate compensation is included around the VOS pin's circuitry to ensure its stability.

**Figure 1. Block diagram of DCS-Control™ topology**



The comparator then outputs a signal to the control circuit, telling it whether or not to output a switching pulse to the gate driver, which controls the high-side MOSFET. The comparator works with the timer circuit to provide both the fastest response to load transients and a regulated switching frequency.

Based on the ratio of $V_{OUT}$ to $V_{IN}$, the timer sets a minimum ON time ($t_{ON\_min}$) that can extend the ON-time control from the comparator. The minimum ON time set by the timer typically is shown in the device datasheet with an equation, such as

$$t_{ON} = \frac{V_{OUT}}{V_{IN}} \times 400 \text{ ns}.$$

In this example based on the TPS62130, the target switching period is 400 ns; therefore, the switching frequency is its reciprocal, or 2.5 MHz. A regulated switching frequency is maintained over the input and output voltage ranges due to the $V_{OUT}/V_{IN}$ factor, which adjusts the minimum ON time based on the ideal duty cycle for a buck converter. Thus, the ON-time equation also can be written as $t_{ON} = D \times t_{Period}$, which is the exact definition of ON time for any buck converter.

The control of the low-side MOSFET is simple. After the high-side MOSFET turns off, the low-side MOSFET turns on and efficiently ramps down the inductor current. The low-side MOSFET turns off when either the inductor current decays to zero, or the high-side MOSFET is told by the comparator to turn on again. An appropriate dead time is implemented to avoid shoot-through currents in the MOSFETs.

## Power-save mode

A key component of the DCS-Control topology is its power-save mode. Generally, most power-save modes activate at lower load currents and increase the conversion efficiency by skipping switching pulses and reducing the device's current consumption (quiescent current). Skipping switching pulses operates the device in discontinuous conduction mode (DCM), which eliminates the negative inductor current (current flowing from the output towards the input) that otherwise would occur at light loads. Such current merely undoes the work of previous switching cycles and incurs additional losses, which decrease efficiency. Reducing the quiescent current improves the efficiency at very light loads, as explained in detail in Reference 2.

The power-save mode in the DCS-Control topology is very simple. It is implemented with the same circuitry as described earlier—there is no switching between two different control modes during the transition from power-save mode to PWM mode. Some other control topologies switch between one control method for power-save mode and a different one for PWM mode. This creates the opportunity for glitches and random noise to occur during the transition. More details about these phenomena are provided later in this article under "Seamless transition."

The DCS-Control topology implements its power-save mode in a straightforward way: If the comparator does not need a switching pulse, then no pulse is given. So, if the output voltage is above its set point (as measured by the error amplifier) when the inductor current decays to zero, the device does not output a new switching pulse; instead, it reduces its quiescent current and enters power-save mode. It waits until the error amplifier tells the comparator that the output voltage has decreased to its set point and should now be increased. Then the device outputs a switching pulse that lasts for the minimum ON time, raising the output voltage just high enough to stay within regulation. Minimum propagation delays through these circuits result in high efficiency and well-regulated output voltage during power-save mode.

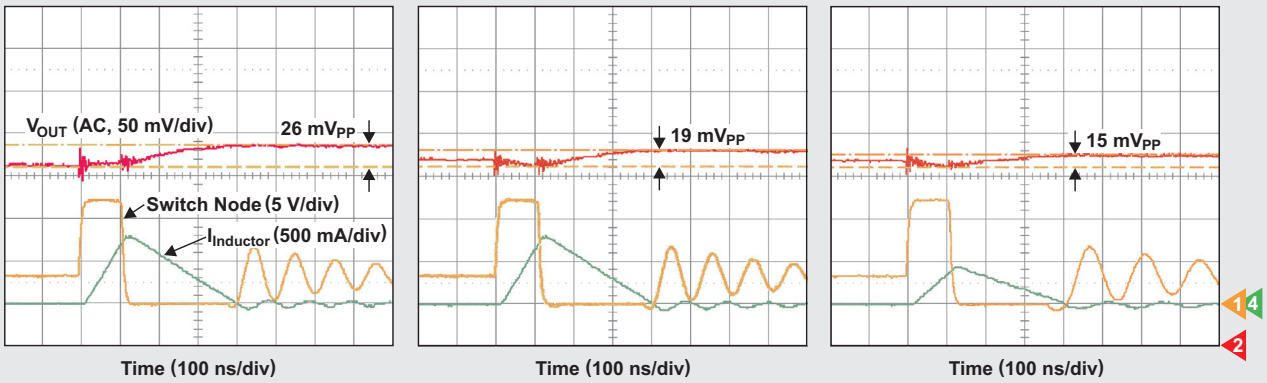
A single switching pulse persisting for the minimum ON time transfers the smallest possible amount of energy to the output, creating the smallest amount of output-voltage ripple. As the light-load current increases, the single pulses occur closer together and increase the switching frequency above the audio band at a faster rate than other power-save topologies. Other topologies use groups or bursts of pulses during the power-save mode that cause much more energy than required to be transferred to the output during a burst. Since the output voltage takes more time to drop back down to its set point, the bursts are spaced further apart, keeping the effective frequency in the audio range longer. The single-pulse architecture of DCS-Control allows operation above the audio band at lower load currents than these other topologies. A case study of the noise performance in power-save mode is given in Reference 3.

When the load increases enough such that there is no time between the single pulses, the inductor current does not return to zero before the comparator tells the high-side MOSFET to turn on again. This load condition occurs at the DCM boundary and is where the converter exits power-save mode and enters PWM mode.

### Output-voltage ripple in power-save mode

This combination of predictable operation in power-save mode (a single pulse for the minimum ON time) and entry into PWM mode when a zero inductor current is reached makes the DCS-Control topology much more flexible than other topologies, allowing easier configuration to system

**Figure 2. TPS62130's output-voltage ripple**




(a) With default EVM

(b) With additional 22-µF output capacitor

(c) With additional 22-µF output capacitor and inductor increased to 2.2 µH

requirements. As an example, consider the output-voltage ripple in the power-save mode of a system with a 12-V input and 3.3-V output. TI's TPS62130 evaluation module (EVM),[4] operating at the 2.5-MHz setting, was used for Figure 2 to demonstrate how to decrease the ripple by increasing the external inductance and output capacitance. The no-load condition was used to show the worst-case output-voltage ripple in power-save mode.

Figure 2a shows the already low output-voltage ripple of 26 mV peak-to-peak, or 0.8% of the 3.3-V output voltage, obtained with the default circuit. Increasing the output capacitance decreases the output-voltage ripple, since the same amount of energy is transferred during each switching pulse. With more output capacitance, this fixed energy results in less voltage ripple (Figure 2b). Increasing the inductance reduces the peak current reached in a switching pulse, since the ON time remains the same. Since a lower peak current stores less energy ($E = \frac{1}{2} \times L \times I^2$), less energy is transferred to the output, again resulting in less voltage ripple (Figure 2c). Note that the ON time is the same for each circuit because it is fixed inside the device and cannot be changed by the external components.

The engineer can also set the load current at which power-save mode is entered by adjusting the inductance, which changes the boundary to DCM. A larger inductance results in less inductor-current ripple, which means the inductor current remains above zero down to lower output-current levels. This ability to adapt the power-save mode's entry point and output-voltage ripple to specific needs allows this topology to be used in a variety of applications, including those that are highly sensitive to noise. Examples include low-power wireless transmitters and receivers in medical or industrial applications (see Reference 5), portable power in consumer devices, and power for solid-state drives.

## Transient response

Since the DCS-Control topology detects the actual output voltage through the VOS pin, it is well-suited to respond to load transients. This signal is fed directly to the comparator and does not travel through the bandwidth-limited error amplifier before affecting the ON time. Being hysteretic, the DCS-Control topology responds fastest to load transients, a capability that is further enhanced by its device's 100% duty-cycle mode.

In this mode, the device keeps the high-side MOSFET on for as long as necessary for the output voltage to recover. In other words, the ON time demand of the comparator is fully met. Figure 3 shows the TPS62130 EVM's response to a no-load to 1-A-load transient through its 100% duty-cycle mode. The 300-ns time delay between the

**Figure 3. TPS62130 EVM's 100% duty-cycle mode during transient response**

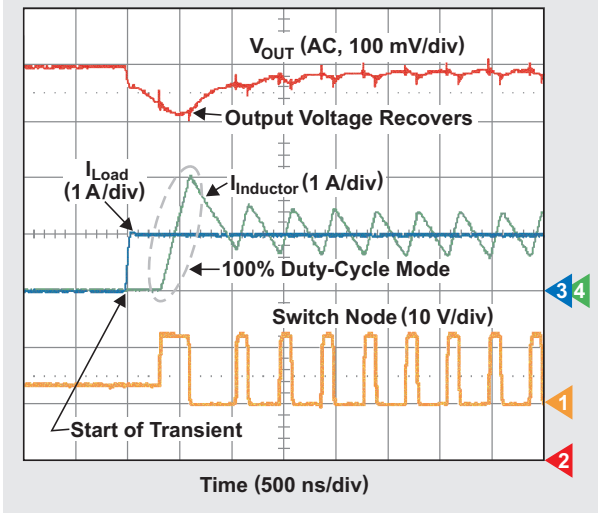
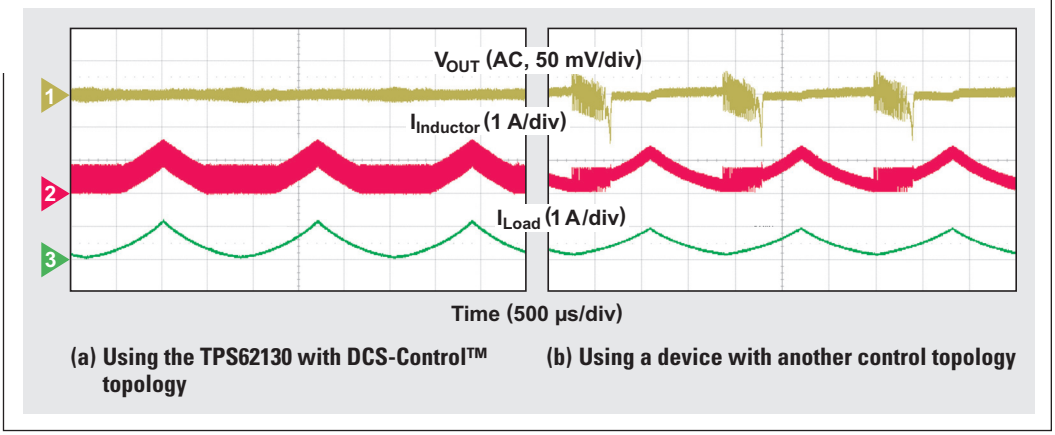


**Figure 4. Transition from PWM mode to power-save mode**




start of the transient and when the high-side MOSFET turns on means that the transient response is limited almost entirely by large-signal concerns (the inductance) and not by small-signal concerns (the control topology). Thus, the DCS-Control topology is not the main limitation of the transient-response capabilities of the device; rather, it enables outstanding transient response for given output-filter components.

## Seamless transition

It was previously noted that, in the DCS-Control topology, only one circuit controls both the PWM and the power-save modes. This allows a faster but also a seamless transition between control modes. It also allows for better performance when the circuit's operating conditions approach the boundary between modes. Since there is no mode switch, there is no glitch at the output.

Figure 4 compares the mode-transition behavior of the TPS62130 to that of a device using another control topology. The load current (bottom trace in green) varies from 10 mA to 1 A in a triangle-like pattern. Both the inductor current and the output-voltage ripple are observed for perturbations or disturbances.

For the TPS62130, which uses the DCS-Control topology, Figure 4 shows much smoother output-voltage and inductor-current waveforms than for the device using another control topology. The TPS62130 outputs lower voltage ripple at all load currents. The ripple increases slightly at lower loads; but, since the device enters power-save mode, this increase is far less than for the device with the other topology. Finally, and most important, there is a relatively large drop in the output voltage (under some limited operating conditions, such as with this load ramp) as the load increases and the device with the other topology exits power-save mode and enters PWM mode. Clearly, this is not desirable for the load or the system and is eliminated with the DCS-Control topology.

## Conclusion

The DCS-Control topology is a great improvement over other control topologies because it provides excellent transient response with a seamless transition into power-save mode. Its single-pulse power-save mode provides low output-voltage ripple and improves the performance of numerous types of end equipment and systems, including noise-sensitive applications.

## References

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3. Brian Berner, "Designing for lowest noise with the TPS62125," Application Report. Available: www.ti.com/slva523-aaj
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5. "Step down converter with bypass mode for ultra low power wireless applications," TPS62732/33/30 Datasheet. Available: www.ti.com/slvsac3-aaj

## Related Web sites

Power Management:
**www.ti.com/power-aaj**

**www.ti.com/dcs-control-aaj**
**www.ti.com/tps62130-aaj**
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