Digital current balancing for an interleaved boost PFC

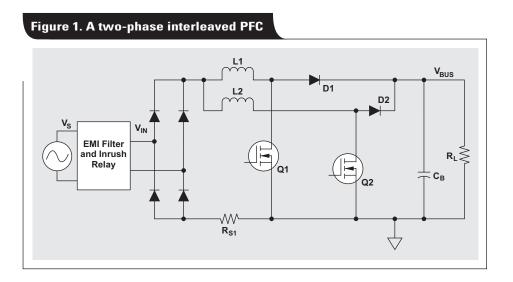**By Bosheng Sun**

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Introduction

A power-factor correction (PFC) converter lets the input current track the input voltage so that the load appears like a resistor to the voltage source that powers it. The most popular power topology used in active PFC is the non-isolated boost converter. For high power levels, two boost units can connect to the same bridge rectifier and operate at 180° out of phase (Figure 1). This is called two-phase interleaved PFC. By controlling two phases' inductor currents 180° out of phase, both input- and output-current ripple can be reduced. As a result, a smaller electromagnetic-interference filter can be used, which reduces material costs. Due to discrepancies between the two sets of components used in the two boost circuits, the two inductor currents inevitably will be different. This situation gets worse when PFC enters continuous-conduction mode (CCM). While the unbalanced current causes more thermal stress on one phase, it may also mistrigger over-current protection. Therefore, a current-balancing mechanism is necessary for the interleaved PFC design.[1–4]
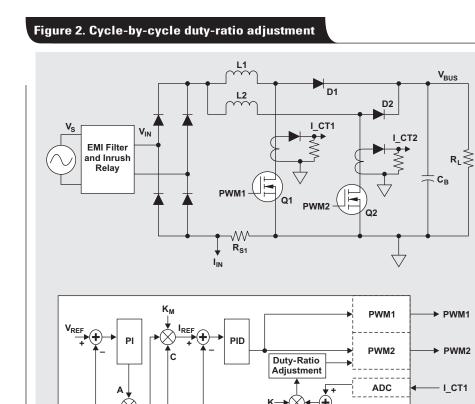
This article discusses three different digital-control methods of balancing inductor currents. The first method senses the inductor current on each switching cycle, compares the current difference between the two phases, then adjusts the duty ratio of one phase cycle-by-cycle. The second method only adjusts the duty ratio in each half AC cycle. The third method uses two independent current loops to control each phase individually. Since these loops share the same current reference, the current is balanced automatically.

Method 1: Cycle-by-cycle duty-ratio adjustment

In this approach, a shunt is used to sense the total current. An average-current mode control is employed to force the input current to track input voltage. The pulse-width-modulation (PWM) controller generates two signals, each with the same duty ratio but shifted by 180° to drive the two boost stages. A current transformer (CT) is put right above the MOSFET in each phase to sense the switching current. The CT outputs are sampled and compared to each other; then the error is multiplied by a gain K, and the multiplier output is used to adjust the duty ratio of phase 2 accordingly. For example, if phase 1 has higher current than phase 2, the error is positive. The multiplier
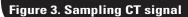
Figure 1. A two-phase interleaved PFC

Figure 2. Cycle-by-cycle duty-ratio adjustment
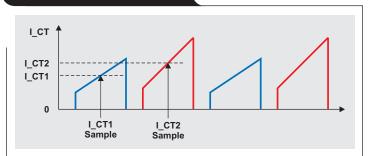

output, which is also positive, increases the duty ratio of phase 2 and thus its current. This configuration is shown in Figure 2.

Properly sampling the CT currents is critical for this approach. Since the CT outputs are saw waves, both currents need to be sampled at the same point for a fair comparison. An example would be to sample both at the middle of the switch's ON time, as shown in Figure 3. Here the unbalanced current causes different magnitudes of CT output.

Figure 3. Sampling CT signal
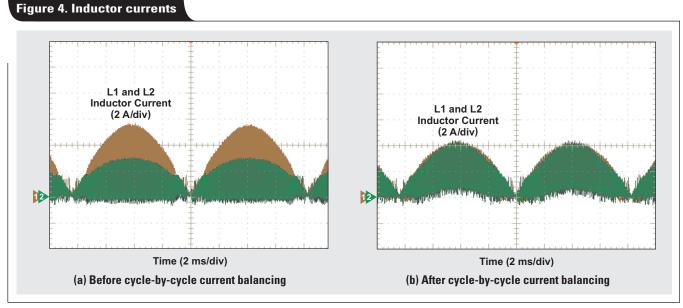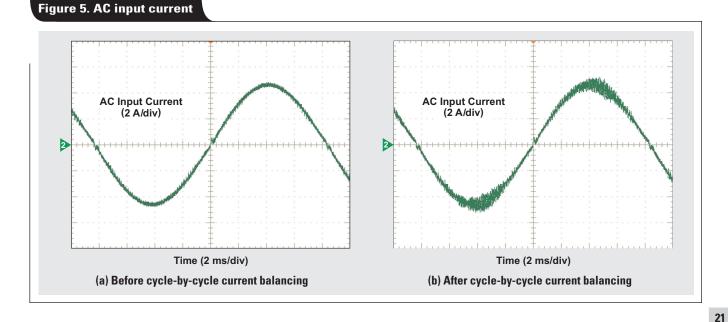
With proper sampling of the CT currents, the cycle-by-cycle approach gives good current balancing. Figure 4 shows test results from a 360-W, digitally controlled interleaved PFC. As can be seen, there is a big difference between the inductor currents, but they almost overlap after being balanced.

Because the second-phase duty ratio is adjusted on each switching cycle, and the adjustment may be different for each cycle since the current difference may vary between cycles, this method inevitably brings high-frequency noise to the AC input current. Figure 5a shows that the waveform of the AC input current before current balancing is smooth and clean. Once current balancing is introduced, high-frequency noise appears (Figure 5b).

Method 2: Half-AC-cycle duty-ratio adjustment

Since adjusting the duty ratio on each switching cycle brings high-frequency noise to the total input current, it seems reasonable to try adjusting the duty ratio only once in each half AC cycle. Either average or peak inductor current in each half AC cycle can be used for current balancing. An example is to force the peak inductor currents to be equal in each half AC cycle by using a configuration similar to that in Figure 2. I_CT1 and I_CT2 are still sampled in each switching cycle, and the firmware finds out the peak value of I_CT1 and I_CT2 in each half AC cycle. These peak values are then compared, and the error is used to adjust the duty ratio. Since the current difference is calculated only once in each half AC cycle,

Figure 4. Inductor currents

L1 and L2 Inductor Current (2 A/div)

Time (2 ms/div)

(a) Before cycle-by-cycle current balancing

L1 and L2 Inductor Current (2 A/div)

Time (2 ms/div)

(b) After cycle-by-cycle current balancing

Figure 5. AC input current

AC Input Current (2 A/div)

Time (2 ms/div)

(a) Before cycle-by-cycle current balancing

AC Input Current (2 A/div)

Time (2 ms/div)

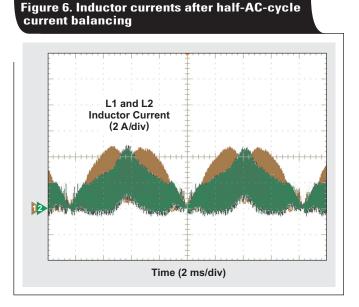**(b) After cycle-by-cycle current balancing**

the same duty-ratio adjustment is applied to the next half AC cycle. This essentially solves the issue of high-frequency noise. Test results showed that the AC current's waveform was almost the same as before current balancing was enabled; the high-frequency noise went away.

This approach also has a drawback. Because the relationship of the duty ratio to the input-current transfer function is different for continuous-conduction mode (CCM) and discontinuous-conduction mode (DCM),[5] the converter dynamics may change abruptly. Applying the same duty-ratio adjustment along the half AC cycle distorts the inductor current (Figure 6) even though the total input current is still sinusoidal. Moreover, because of discrepancies between the two component sets used in the two boost circuits, the circuits enter CCM at different points in each half AC cycle. Thus, the distortions of the two phases are also different. On the other hand, unlike the unbalanced currents in Figure 4a, this approach can force the peak values of inductor currents in each half AC cycle to be equal, so the current does get balanced to some level.

Method 3: Dual current-control loops

In the preceding approaches, there is only one current-control loop. The total current is used for current-loop control, and the two phases get the same duty ratio from the same control loop. If two current-control loops with the same current reference are used, with each controlling one phase individually, the closed-loop control will force the current to be balanced automatically, making duty-ratio adjustments unnecessary.
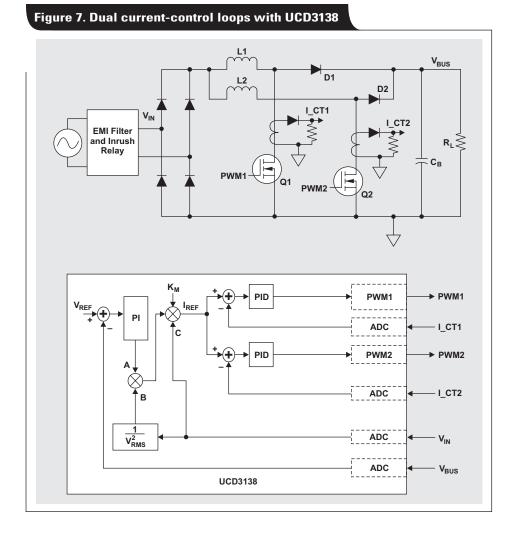
For analog controllers, adding one more loop means adding another compensation network and another feedback pin. Inevitably, this increases the cost and design effort. With a general digital controller, the current-control loop is implemented by firmware. Adding a second loop means adding extra code, which at first seems to be a good solution. However, the extra code takes extra CPU execution time. The CPU that used to do only one loop calculation now needs to do two. For this to happen without causing any interruption overflow, the CPU speed needs to be increased. This requires a higher-cost CPU with more power consumption. Another choice can be to

Figure 6. Inductor currents after half-AC-cycle current balancing

L1 and L2 Inductor Current (2 A/div)

Time (2 ms/div)

reduce the control-loop speed—for example, from 50 kHz to 25 kHz. The CPU speed can then be kept the same, and the dual-loop calculation can be completed without causing any interruption overflow. However, the loop bandwidth suffers due to the reduced control-loop speed, and a reduced bandwidth deteriorates PFC performance.
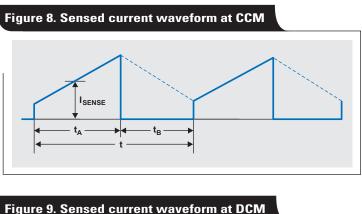
Integrated control solution

A second-generation digital controller such as the Texas Instruments UCD3138 offers a different solution. This is a fully programmable digital controller, but the control loop is implemented by hardware. Based on the proportional integral derivative (PID), the control loop is a two-pole, two-zero digital compensator. All the loop calculations are done by hardware with a speed of up to 2 MHz. The firmware just needs to configure the PID coefficients. This allows a low-speed CPU to be used because it needs to do only the low-speed tasks, such as housekeeping and communication. Moreover, the UCD3138 has three independent loops inside the chip, so the dual current-control loops can be implemented without any extra hardware or a

Figure 7. Dual current-control loops with UCD3138

higher-speed CPU. Figure 7 shows the configuration of these dual control loops implemented with the UCD3138. The current-feedback signal from each phase needs to be measured. Normally, a CT placed above the MOSFET can be used. Since no current shunt is needed, this configuration also can improve efficiency.

Because the CT is placed right above each switch (Figure 7), it senses only the switching current. This is only the rising part of the inductor current, whereas each current loop controls the average inductor current. The CT current signal is still sampled at the middle of the PWM ON time (Figure 3). It is an instantaneous value, represented as I_{SENSE} in Figures 8 and 9. The sampled switching current (I_{SENSE}) is equal to the average PFC inductor current only when the current is continuous (Figure 8). When the current becomes discontinuous (Figure 9), I_{SENSE} is no longer equal to the average PFC inductor current. In order to control the average inductor current, the relationship between the middle point where I_{SENSE} is sampled and the average inductor current over a switching period needs to be derived and applicable to both CCM and DCM.

Figure 8. Sensed current waveform at CCM

Figure 9. Sensed current waveform at DCM

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For a boost-type converter in steady-state operation, the volt-second of the boost inductor maintains balance in each switching period:

$$t_A \times V_{IN} = t_B \times (V_{OUT} - V_{IN}), \qquad \textbf{(1)}$$

where t_A is the current rising time (PWM ON time), t_B is the current falling time (PWM OFF time), V_{IN} is input voltage, and V_{OUT} is output voltage, assuming all power devices are ideal. From Figures 8 and 9, the average inductor current (I_{AVE}) can be calculated in terms of I_{SENSE}:

$$I_{AVE} = I_{SENSE} \times \frac{t_A + t_B}{t}, \qquad \textbf{(2)}$$

where t is the switching period. Combining Equations 1 and 2 results in

$$I_{SENSE} = \frac{I_{AVE} \times t \times (V_{OUT} - V_{IN})}{t_A \times V_{OUT}}. \qquad \textbf{(3)}$$

Through Equation 3, the average inductor current (I_{AVE}) is interpreted via instantaneous switching current (I_{SENSE}). I_{AVE} is the desired current, and I_{SENSE} is the current reference for the current-control loops. The real instantaneous switching currents are sensed and compared with this reference, and the error is sent to the current-control loops.

Figure 10 shows the test result of this approach. As shown in Figure 4, even though the two inductor currents have a wide variance, they almost overlap completely after current balancing is enabled. Meanwhile, the total AC current remains smooth and clean.

Conclusion

Three different digital-control methods of balancing inductor currents have been evaluated for an interleaved boost PFC. By comparing the current difference and adjusting the duty ratio cycle-by-cycle, the current can be balanced very well. However, this method also injects high-frequency noise into the total input current. Adjusting the duty ratio only once in each half AC cycle eliminates the high-frequency noise, but each individual inductor current gets distorted even though the total AC current is sinusoidal. A better approach is to use two current loops, with each controlling one phase individually. Since the two current loops share the same current reference, the current is balanced automatically. With a digital controller, the cost for a second loop is just a few extra codes. Test results show that the third approach gives the best performance.

References

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Figure 10. Inductor currents balanced with UCD3138 dual control loops

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