High-Performance Analog Products

Analog Applications Journal

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Contents

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Introduction

The *Analog Applications Journal* is a digest of technical analog articles published quarterly by Texas Instruments. Written with design engineers, engineering managers, system designers and technicians in mind, these "how-to" articles offer a basic understanding of how TI analog products can be used to solve various design issues and requirements. Readers will find tutorial information as well as practical engineering designs and detailed mathematical solutions as they apply to the following product categories:

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Analog Applications Journal articles include many helpful hints and rules of thumb to guide readers who are new to engineering, or engineers who are just new to analog, as well as the advanced analog engineer. Where applicable, readers will also find software routines and program structures.

Grounding in mixed-signal systems demystified, Part 2

By Sanjay Pithadia, *Analog Applications Engineer,*
and Shridhar More, *Senior Analog Applications Engineer*

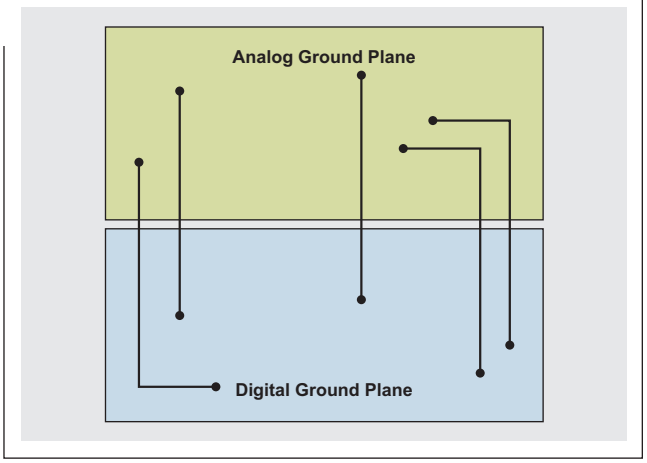
This article is the second of a two-part series. Part 1 (see Reference 1) explained typical terminologies and ground planes and introduced partitioning methods. Part 2 discusses the pros and cons involved in splitting the ground planes. It also explains grounding in systems with multiple converters and multiple boards.

If the ground planes are split and the traces are run across the split as shown in Figure 1, what will be the current return path? Assuming that the two planes are connected somewhere, usually at a single point, the return current has to flow in that large loop. High-frequency currents flowing in large loops produce radiation and high ground inductance. Low-level analog currents flowing in large loops are susceptible to interference.

If the two planes are connected only at the power supply (Figure 2), the return current is forced to flow all the way back to the power-supply ground, which is a really big loop! Also, the analog and digital ground planes, which are at different RF potentials and connected with long wires, unfortunately form a very effective dipole antenna.

It is preferred to have a continuous ground plane to avoid such long ground loops, but if it is absolutely necessary to have a split ground plane and traces are run across the split, the planes should first be connected at one location to form a bridge for the return current (Figure 3). Routing all the traces so they cross at this bridge provides a return path directly underneath each of the traces, producing a very small loop area. A typical application of this method is a weighing scale where high-resolution (≥20-bit) delta-sigma analog-to-digital converters (ADCs) are used.

Figure 1. Signal traces crossing a split on ground plane



Other options for passing the signal over a split plane are to use optoisolators (through light), transformers (through a magnetic field), or a true differential signal (where the signal flows down one trace and returns on the other trace with no ground needed for the return current).

A better approach is *partitioning*. It is always preferable to use only one ground plane, partitioning the PCB

Figure 2. Split planes connected at power supply

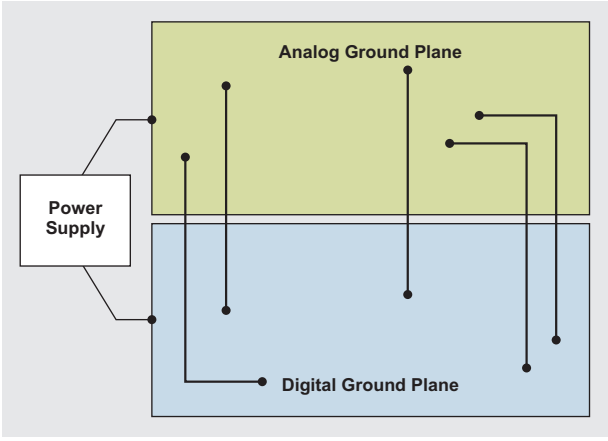


Figure 3. Ground-plane bridge for traces

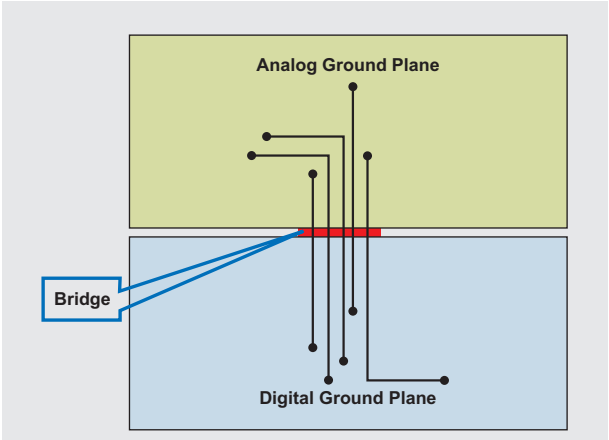
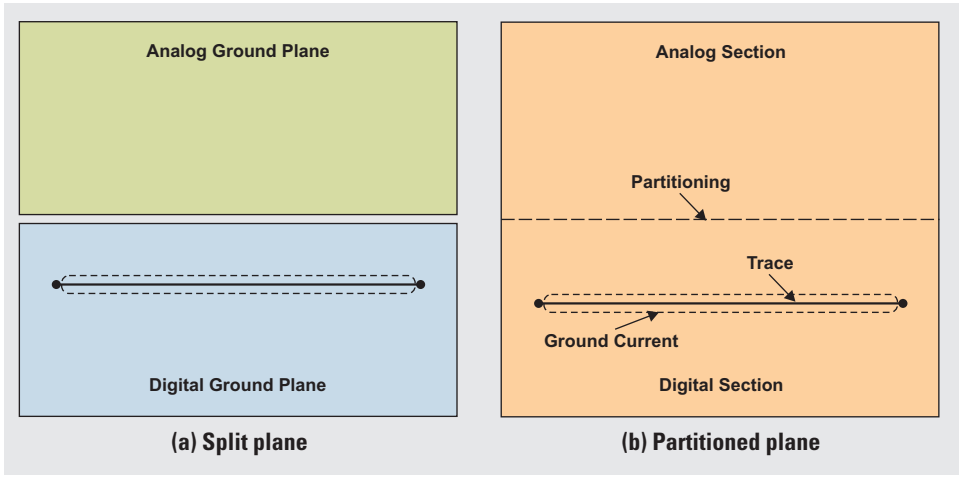


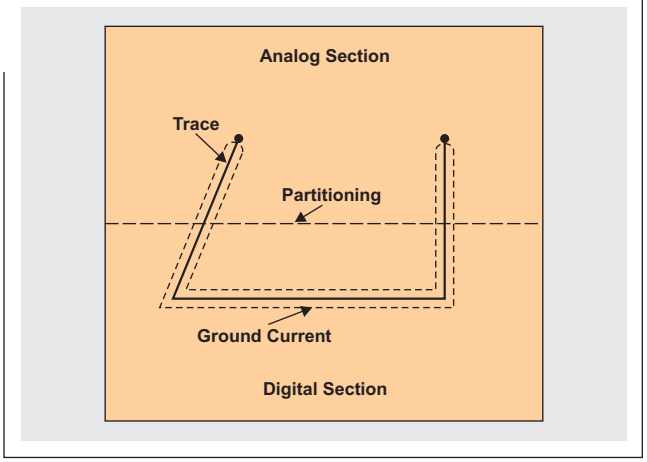
Figure 4. Ground-plane layouts



into analog and digital sections (see Figure 4b). Analog signals must be routed only in the board's analog section, and digital signals must be routed only in the board's digital section, with both on all layers. Under these conditions, the digital return currents do not flow in the analog section of the ground plane and remain under the digital signal trace. Figure 4 compares a split plane and a partitioned plane.

The only problem with partitioning is that it is difficult when analog signals are improperly routed into the board's digital section, or vice versa (Figure 5). So for any PCB layout, the important points are to use a single ground plane, partition it into analog and digital sections, and apply discipline in routing.

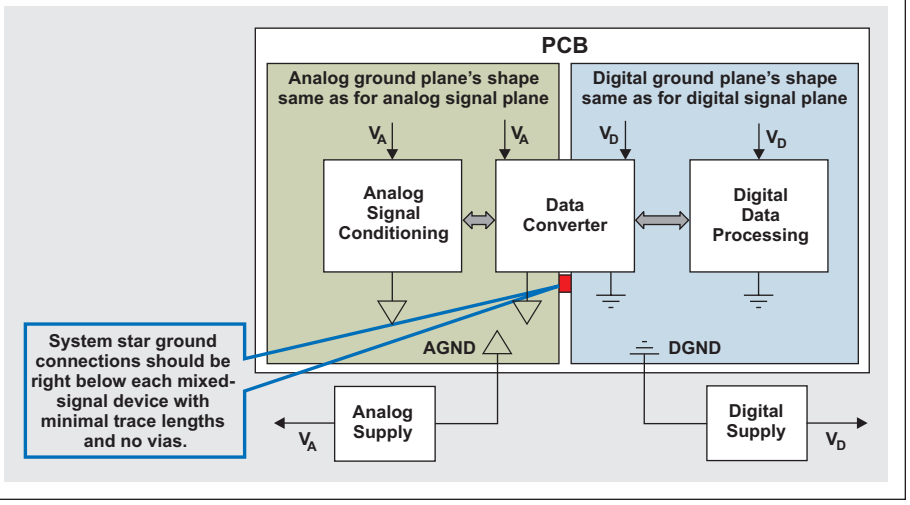
Figure 5. Improperly routed digital signal trace



Grounding when multiple data converters are used on a single board

Most datasheets for data converters discuss grounding relative to a single PCB, usually the manufacturer's own evaluation board. Usually the recommendation is to split the PCB ground plane into an analog plane and a digital plane. It is further recommended that the analog ground (AGND) and digital ground (DGND) pins of a converter be tied together and that the analog and digital ground planes be connected at that same point, as shown in Figure 6. This essentially creates the system's star ground point at the mixed-signal device. As explained in Part 1, all voltages in the circuit are measured with respect to this particular point, not just to an undefined ground wherever one can clip a probe.

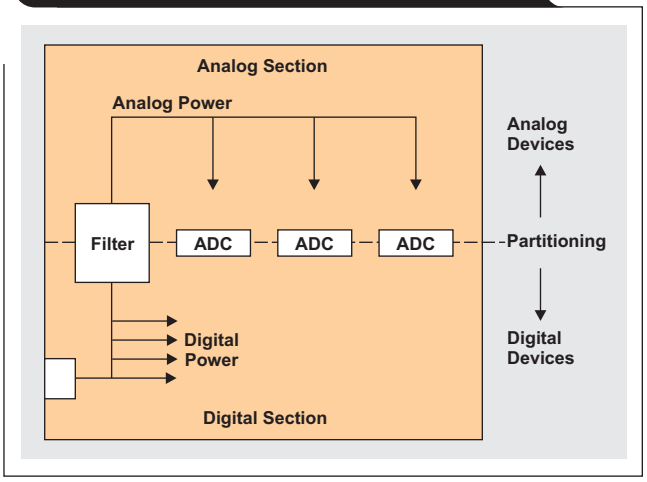
Figure 6. Grounding mixed-signal devices on a single PCB



All noisy digital currents flow through the digital power supply to the digital ground plane and back to the digital supply, thus being isolated from the board's sensitive analog portion. The system's star ground point occurs where the analog and digital ground planes are joined together at the data converter. While this approach generally works in a simple system with a single PCB and a single data converter, it usually is not good for multicard and multiconverter systems. If there are several data converters located on different PCBs, the concept breaks down because the analog and digital ground systems are joined at each converter on the PCB, creating ground loops.

Suppose a designer is working on an eight-layer PCB that has three DACs and two ADCs. To minimize noise, the analog and digital ground planes should be connected together solidly under all the ADC and digital-to-analog converter (DAC) chips. The AGND and DGND pins should be connected to each other and to the analog ground plane, and the analog and digital ground planes should be connected individually back to the power supply. The power should enter the board in the digital partition and be fed directly to the digital circuitry, then filtered or regulated to feed the analog circuitry. Then only the digital ground plane should be connected back to the power supply. Figure 7 shows the partitioned analog and digital ground planes and the power-supply connection for a PCB with multiple data converters.

Figure 7. Power and ground for PCB with multiple ADCs



Multicard mixed-signal systems

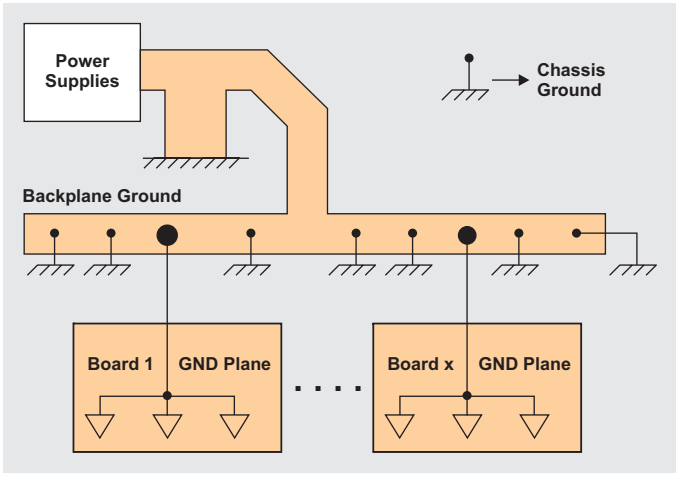
Confusion about mixed-signal grounding has increased since designers started applying single-card grounding concepts to multicard systems. In systems having several data converters on different PCBs, the analog and digital ground planes are connected at several points, creating the possibility of ground loops and making a single-point star ground system impossible.

The best way to minimize ground impedance in a multicard system is to use a motherboard PCB as a backplane for interconnections between cards. This provides a continuous ground plane to the backplane. The PCB connector should have at least 30 to 40% of its pins devoted to ground. These pins should be connected to the ground plane on the backplane motherboard. To complete the overall system grounding scheme, there are two possibilities:

1. The backplane's ground plane can be connected to the chassis ground at numerous points, thereby diffusing the various ground-current return paths. This is commonly referred to as a multipoint grounding system (Figure 8).
2. The ground plane can be connected to a single star ground point (generally at the power supply).

The first approach is most often used in all-digital systems but can also be used in mixed-signal systems, provided that the ground currents from digital circuits are sufficiently low and diffused over a large area. The low

Figure 8. Grounding scheme for multicard system



ground impedance is maintained all the way through the PCBs, the backplane, and ultimately the chassis. However, it is critical that good electrical contacts be made where the grounds are connected to the sheet-metal chassis. This requires self-tapping sheet-metal screws or biting washers. Special care must be taken where anodized aluminum is used for the chassis material, since its surface acts as an insulator.

The second approach, a single-point star ground, is often used in high-speed mixed-signal systems having separate analog and digital ground systems.

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Synchronous rectification boosts efficiency by reducing power loss

By Anthony Fagnani
Power Applications Engineer

Introduction

Some applications require the highest possible power efficiency. For example, in a harsh environment that requires a DC/DC power supply to operate in high ambient temperatures, low-power dissipation is needed to keep the junction temperature of semiconductor devices within their rated range. Other applications may have to meet the strict efficiency requirements of ENERGY STAR® specifications or green-mode criteria. Users of battery-operated applications desire the longest run time possible, and reducing the power loss can directly improve run time. Today it is well known that using a synchronous rectifier can reduce power loss and improve thermal capability. Designers of buck converters and controllers for step-down applications are already employing this technique. Synchronous boost controllers also have been developed to address power efficiency in step-up applications.

Typical application

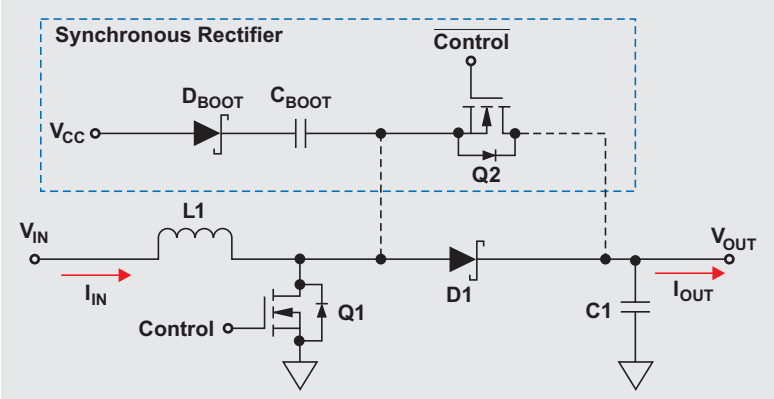
Two typical boost applications can be used to demonstrate the difference between synchronous and nonsynchronous rectification. The first is a lower-input-voltage application that may operate at low duty cycles or, in other words, when the output voltage is close to the input voltage. Example inputs for this system are a USB port or a lithium-ion (Li-Ion) battery pack with two or three series cells. The DC/DC power supply steps up the voltage for charging a two-cell Li-Ion battery or the battery of a tablet PC. The other application boosts the voltage of a system power rail to a high output voltage that can operate at higher duty cycles where the output voltage is much higher than the input voltage. An example input is a 12-V power rail. The high output voltage may be needed for power amplifiers, industrial PCs, or pump-and-dump energy storage for higher energy density.

To evaluate the benefits of synchronous rectification, each application is tested with a real circuit to compare efficiency and power loss. The TPS43060/61 synchronous boost controllers from Texas Instruments (TI) are used to demonstrate the synchronous designs. These current-mode boost controllers integrate the control and gate-drive circuitry for both low-side and high-side MOSFETs. TI's TPS40210 current-mode, low-side-switch boost controller is used for the nonsynchronous designs.

Basic operation

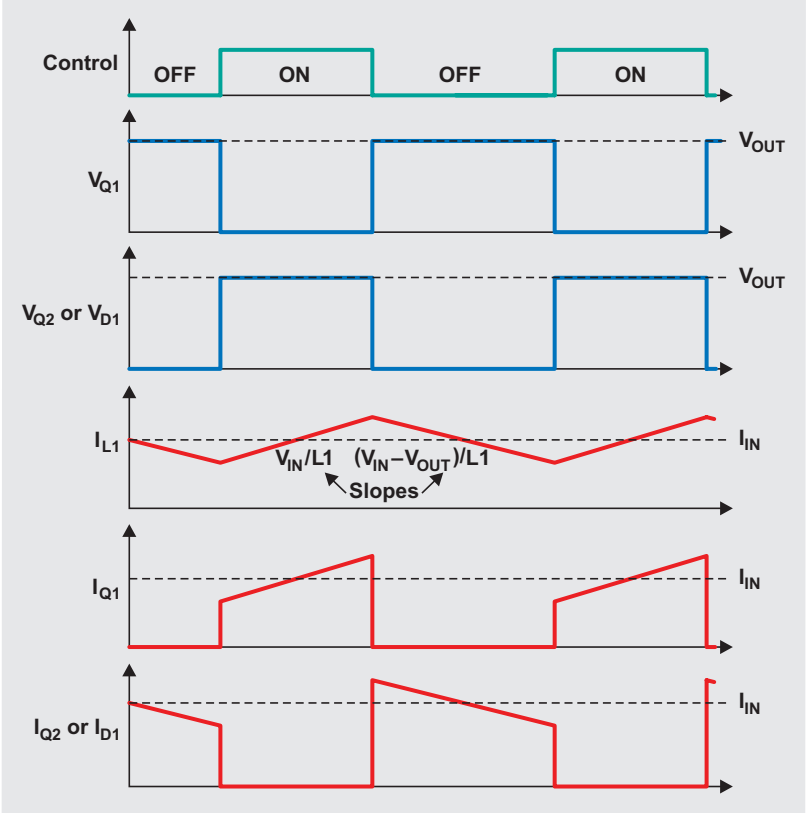
A typical block diagram for a step-up (boost) topology is shown in Figure 1. This topology consists of the low-side power MOSFET (Q1), the power inductor (L1), and the output capacitor (C1). For a synchronous topology, the high-side MOSFET (Q2) is used for the rectifying switch.

Figure 1. Synchronous and nonsynchronous boost circuits



In a nonsynchronous boost topology, a power diode (D1) is used. Figure 2 shows the equivalent waveforms for the voltage and current through the switches and inductor. During the ON time of Q1, the inductor current ramps up, and V_{OUT} is disconnected from V_{IN}. The output capacitor must supply the load during this time. During the OFF time, the inductor current ramps down and charges the output capacitor through the rectifying switch. The peak current in the rectifier is equal to the peak current in the switch.

Figure 2. Ideal voltage and current waveforms in a boost circuit



Selecting the rectifying switch

Nonsynchronous controllers use an external power diode as the rectifying switch. Three main considerations when selecting the power diode are reverse voltage, forward current, and forward voltage drop. The reverse voltage should be greater than the output voltage, including some margin for ringing on the switching node. The forward current rating should be at least the same as the peak current in the inductor. The forward voltage should be small to increase efficiency and reduce power loss. The average diode current is equal to the average output current. The package of the diode chosen must be capable of handling the power dissipation.

Synchronous controllers control another MOSFET for the rectifying switch. If an n-channel MOSFET is used, a voltage higher than the output voltage must be generated for the gate driver. A bootstrap circuit is used to generate this voltage. Figure 1 also includes the typical block diagram for a standard bootstrap circuit consisting of the bootstrap capacitor (C_{BOOT}) and the bootstrap diode (D_{BOOT}). During the ON time of Q1, the bootstrap capacitor is charged to a regulated voltage (V_{CC}), which typically is regulated by a low-dropout regulator internal to the controller. When Q1 turns off, the voltage across the capacitor to ground is $V_{OUT} + V_{CC}$, and the required voltage is available to turn on the high-side switch. The control circuitry also must be more complicated to ensure that there is enough delay before the rectifying switch turns on to avoid both switches turning on at the same time. If this occurs, the output voltage shorts to ground through both switches, causing high currents that can damage the switches.

Power loss of the rectifying switch

To compare the efficiencies of the two different rectifiers, the power dissipation should be calculated. In the nonsynchronous topology, the power dissipation in the rectifying power diode is estimated with Equation 1:

$$P_{D1} = I_{OUT} \times V_{FWD} \quad (1)$$

With a synchronous rectifier, there are two main sources of power dissipation—conduction and dead-time loss. When the low-side switch turns off, there is a time delay (t_{DELAY}) before the high-side switch turns on. During this delay, the body diode (V_{SD}) of the high-side switch conducts current. Typically this is referred to as dead time. When the high-side switch is turned on, there is also conduction loss due to the $R_{DS(ON)}$ of the MOSFET. Equation 2 calculates the duty cycle (D), and Equation 3 estimates the losses (P_{Q2}):

$$D = \frac{V_{OUT} - V_{IN}}{V_{OUT}} \quad (2)$$

$$P_{Q2} = \left(\frac{I_{OUT}^2}{1-D} \times R_{DS(ON)}\right) + \left(V_{SD} \times \frac{I_{OUT}}{1-D} \times 2 \times t_{DELAY} \times f_{SW}\right) \quad (3)$$

In an application requiring a low duty cycle, the rectifying switch conducts for a larger percentage of each switching period. However, the power loss in a nonsynchronous rectifier in a boost topology is independent of duty-cycle changes caused by variations in V_{IN}. This is because variations in V_{IN} also cause an equal but opposite change in the current the diode conducts. The rectifier loss is simply the forward voltage drop times output current per Equation 1. With a synchronous rectifier, there is some dependence on the duty cycle for power dissipation

because the conduction losses are caused by the resistance of the FET. This is unlike a diode, where the losses are caused by the forward voltage drop. A resistive conduction loss varies with current squared, leading to a dependence on duty cycle, with a higher duty cycle increasing the conduction power loss.

Efficiency of low-duty-cycle applications

To evaluate the power efficiency of low-duty-cycle applications, a synchronous design and a nonsynchronous design can be compared. The synchronous design uses the TPS43061 synchronous boost controller paired with TI's CSD86330Q3D power block. The power block integrates both the low-side and high-side MOSFETs. The nonsynchronous design uses the TPS40210 nonsynchronous boost controller and a CSD17505Q5A low-side switch, with specifications similar to those of the power block. This design has a Schottky diode for the rectifier that is rated for at least 15 V and 7 A. The smallest package size available for a Schottky diode with these ratings is a TO-277A (SMPC). A comparison of solution sizes based only on typical switch package sizes finds that the nonsynchronous switch and diode occupy an area of 65 mm^2, and the synchronous power-block switches occupy an area of 12 mm^2. The latter is a space savings of 53 mm^2. Both designs use the same LC filter and a 750-kHz switching frequency. Figure 3 shows the efficiency and power loss of both designs with a 12-V input and a 15-V output. The ideal duty cycle is 20%. The benefit of the synchronous rectifier is clear in this example. The full-load efficiency is improved by about 3%, whereas the power loss in the nonsynchronous design is almost double that in the synchronous design.

Figure 3. Measured efficiency and power loss in a low-duty-cycle application

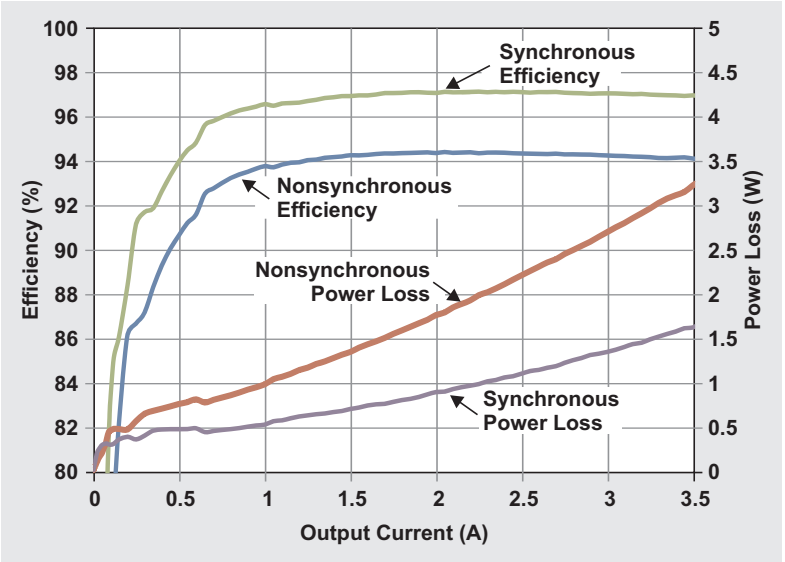
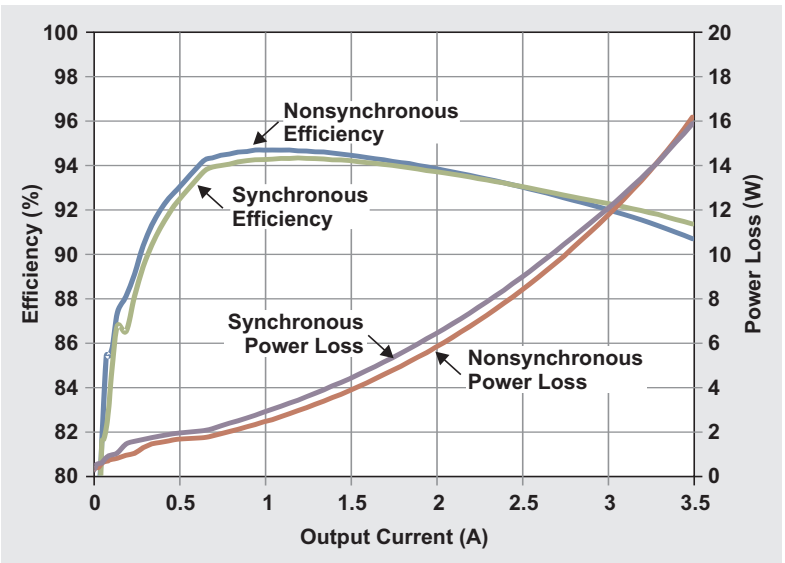


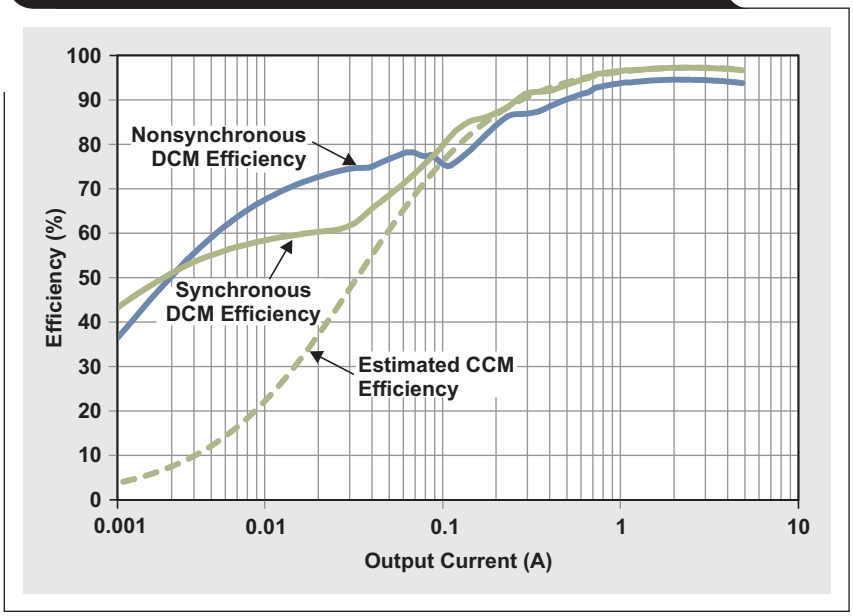
Figure 4. Measured efficiency and power loss in a high-duty-cycle application



Efficiency of high-duty-cycle applications

To evaluate the power efficiency of high-duty-cycle applications, a synchronous and a nonsynchronous design can again be compared. The synchronous design uses the TPS43060 synchronous boost controller with a pair of power MOSFETs for the low-side and high-side switches. The MOSFETs come in a 30-mm^2 typical 8-pin SON package. The nonsynchronous design uses the TPS40210 nonsynchronous boost controller and one of these same MOSFETs for the low-side switch. The Schottky diode for the rectifier is rated for at least 48 V and 16 A. The Schottky rectifier is in a D^2PAK package with a typical area of 155 mm^2. The synchronous solution saves 125 mm^2 of board space over the nonsynchronous design. Both designs use the same LC filter and a 300-kHz switching frequency. Figure 4 shows the efficiency and power loss of both designs with a 12-V input and 48-V output. The ideal duty cycle is 75%. The efficiency curves show that there is no benefit in using a synchronous rectifier in this application. From 2.5 to 3.5 A of load current, the synchronous solution begins to improve efficiency. However, the primary benefit of synchronous rectification is that less board space is required.

Figure 5. Light-load efficiency of DCM and CCM designs



Light-load efficiency

Both the TPS43060 and TPS43061 used in the synchronous designs feature reverse-current detection for discontinuous-conduction mode (DCM), improving efficiency at lighter loads. This reduces conduction losses in the switches, inductor, and sense resistor, enabling the light-load efficiency to be similar to that of the nonsynchronous solutions. For reference, Figure 5 shows a dashed curve for the estimated efficiency of a converter operating in forced continuous-conduction mode (CCM). This efficiency is determined by estimating losses in the switches, inductor, and sense resistor during CCM operation. The curves show the relative improvement in efficiency at light loads for converters operating in DCM. However, for some low-noise applications or applications requiring a fast transient response from light loads, it may be preferable to sacrifice improved light-load efficiency to keep CCM operation over the entire load range.

Conclusion

The benefits of synchronous rectification are evident, especially in low-duty-cycle applications as the load current increases. However, in high-duty-cycle applications with lower output current, a nonsynchronous design may have adequate efficiency. The lower losses with synchronous rectification can improve efficiency and reduce temperature rise and solution size.

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Designing a negative boost converter from a standard positive buck converter

By Mark Pieper
Analog Field Applications

Introduction

There are very few options for the designer when it comes to creating negative voltage rails in point-of-load applications. Integrated devices that are specifically designed for this are uncommon, and other available options typically have significant drawbacks, such as being too large, noisy, inefficient, etc. If a negative voltage is available, it is advantageous to use that as the input for the converter. This article describes a method using a standard positive buck converter to form a negative boost converter, which takes an existing negative voltage and creates an output voltage with a larger (more negative) amplitude. Using a boost regulator results in a smaller, more efficient, and more cost-effective design. A complete design example using an integrated FET buck converter is provided here. The basic theory of operation, high-level design trade-offs, and closed-loop compensation design of the resulting converter are discussed.

Negative boost topology

Implementing a negative boost converter takes advantage of some parallels between the power design and control of a positive buck converter and a negative boost converter. Figure 1 depicts the basic operation of a positive buck regulator. The buck consists of a half bridge that chops V_{IN} and a filter to extract the DC component. The filtered output voltage is regulated by varying the duty cycle (D) of the upper FET. When V_{OUT} is too low, the control loop reacts by causing D to increase. When V_{OUT} is too high, D is decreased. The buck input current is discontinuous (has a higher RMS current), and the output current is continuous and equal to the inductor current waveform. The current flow through the inductor is positive, flowing away from the half bridge.

Figure 2 depicts the negative boost topology in which a more negative voltage is generated from an existing negative voltage. During D, the inductor current is increased, storing energy ($dI = -V_{IN} \times D \times T/L$). During 1 – D, the energy is transferred to the output. When the upper FET is turned off and the lower FET is turned on, the inductor current flows into the output, supporting the load as the inductor current decreases. From Figures 1 and 2 it can be seen that the negative boost regulator resembles the positive buck regulator, except that it is level shifted below ground. Also, V_{IN} and V_{OUT} are transposed. Notice these common features:

- The upper FET is the controlled switch.
- The inductor current flows in the same direction through the inductor (away from the half bridge).
- Increasing V_{OUT} results from increasing D.

Figure 1. Simplified positive synchronous buck regulator

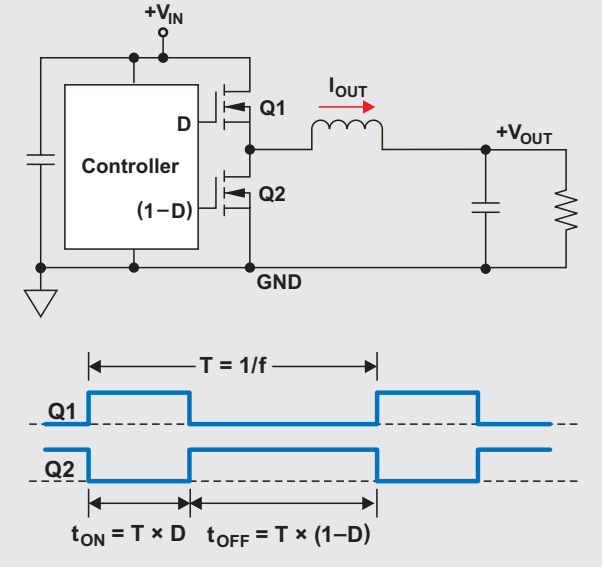


Figure 2. Simplified negative synchronous boost regulator

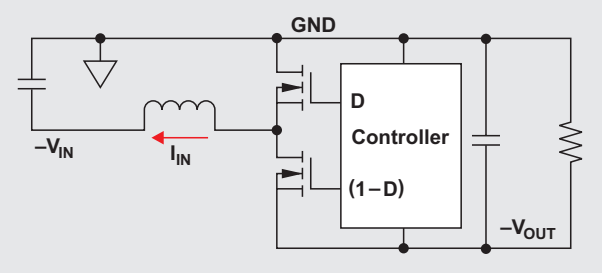
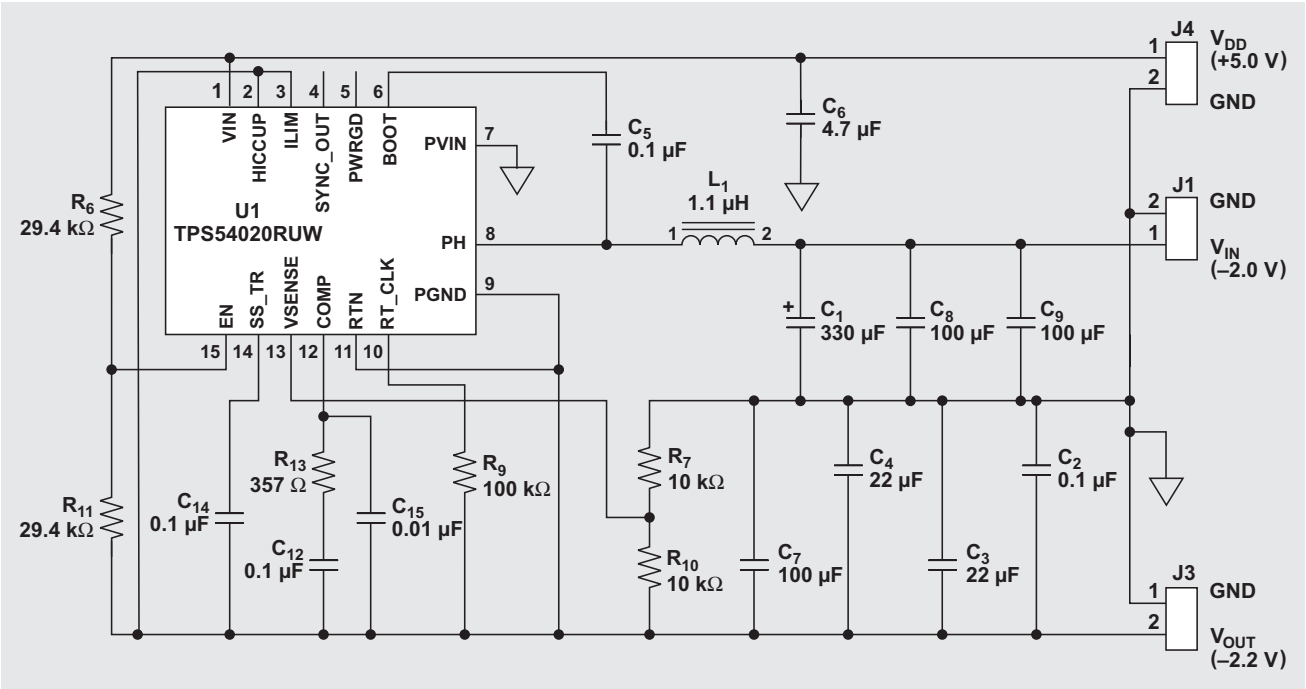


Figure 3. Complete schematic of the example negative boost regulator



The significance of these similarities is that the negative boost converter can be constructed by using a readily available positive buck converter. One difference in operation is that the boost converter has a discontinuous output current and a continuous input current, the opposite of the buck converter.

Converter selection

There are three additional things that need to be considered when selecting a converter:

1. The converter should have external compensation to accommodate the different control algorithm associated with the boost converter, which will be discussed later.
2. The converter is processing current equal to the input current, not the load current, so the current rating and current limit need to be sized accordingly. For instance, neglecting the effects of efficiency (η), a 12-W, –6-V to –12-V boost converter has an output current of 1 A (12 W) and an input current of 2 A (12 W). A converter with a current rating greater than 2 A is required for this design. The output-current rating of the converter selected must be greater than that in Equation 1:

$$I_{RATING} = \frac{P_{OUT}}{\eta V_{IN(min)}}. \quad (1)$$

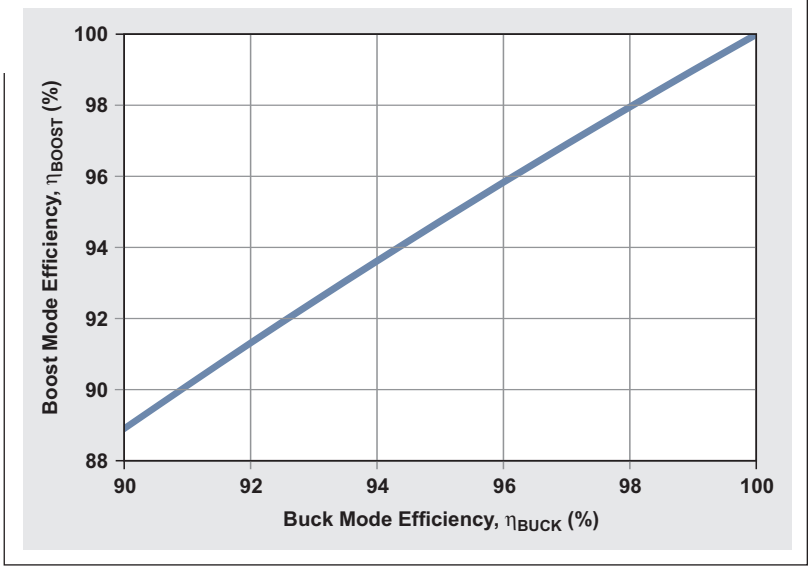
3. The converter's V_{DD} is biased by $-V_{OUT}$. When the converter is first powered on, V_{OUT} equals V_{IN}, and V_{OUT} is increased until it is in regulation. Therefore, the controller specification should allow the converter to start with $V_{DD} = |-V_{IN}|$, and the converter should be rated to operate with $V_{DD} = |-V_{OUT}|$. For instance, a design that converts a –6-V input to a –12-V output requires the controller to start with V_{DD} = 6 V and to continue running after start-up with V_{DD} = 12 V. This can be a problem when the negative input is a low voltage. A solution is to use a converter that has a V_{DD} separate from the power supply's V_{IN}. Figure 3 shows a negative boost regulator designed to convert –2.0 V to –2.2 V by using the TPS54020 from Texas Instruments (TI). Although this is a relatively low-voltage regulator, the principle is the same for any $-V_{IN}$ and $-V_{OUT}$ as long as the converter specifications support the voltages. Notice that the power to U1, pin VIN, is separate from the power ground to pin PVIN, allowing low-voltage operation.

As previously mentioned and defined in Equation 1, the current rating of the converter is driven by input current. Therefore, the power dissipation in the converter is dependent on input current.

The efficiency of the negative boost regulator (η_{BOOST}) is related to that of the positive buck regulator (η_{BUCK}) but is slightly lower. Figure 4 and Equation 2 show the relationship of the two efficiencies, which are about equal when the specified η_{BUCK} is above 90%:

$$\eta_{BOOST} = \frac{2\eta_{BUCK} - 1}{\eta_{BUCK}} \quad (2)$$

Figure 4. Efficiency of negative boost regulator



Component selection

The inductor can be chosen by using the same criteria as defined in the buck converter's datasheet. The boost converter's input and output capacitors should be chosen based on ripple voltages required by the application, keeping in mind that the output capacitor must be rated for the higher RMS current.

Control theory

Boost converters have a different, more complicated transfer function than buck converters. As with buck converters, the transfer function is different between voltage-mode control and current-mode control. This analysis uses a current-mode-controlled boost converter based on the TPS54020, a current-mode device. The Bode-plot method is used to evaluate the stability of this control-loop design. Points of interest for stability are the phase when the open-loop gain crosses unity, and the gain when the phase crosses –180°. The open-loop gain is equal to the forward transfer function multiplied by the control transfer function, including all gains around the control loop.

The current-mode power stage ("plant" in control jargon) has the forward transfer function given in Equation 3:[1]

$$G_{PS}(s) = \frac{g_M \times R_{LOAD} \times (1-D)}{2} \times \frac{\left(1+\frac{s}{2\pi \times f_{ESR}}\right)\left(1-\frac{s}{2\pi \times f_{RHPZ}}\right)}{1+\frac{s}{2\pi \times f_P}} \times H_e(s), \quad (3)$$

where s is the complex Laplace variable and $H_e(s)$ represents the higher-frequency dynamics. The continuous boost has two salient control features. First, the plant is a single-pole system, owing to the effect of current-mode control. Second, there is a right-half-plane zero (RHPZ).[1, 2] The RHPZ, plant pole, and C_{OUT} equivalent-series-resistance (ESR) zero frequencies are described respectively by the following equations:

$$f_P = \frac{2}{2\pi R_{LOAD} C_{OUT}} \quad (4a)$$

$$f_{ESR} = \frac{1}{2\pi R_{ESR} C_{OUT}} \quad (4b)$$

$$f_{RHPZ} = \frac{R_{LOAD}}{2\pi L} \times \left(\frac{V_{IN}}{V_{OUT}}\right)^2 \quad (4c)$$

The RHPZ requires that the unity-gain bandwidth of the loop be less than the minimum RHPZ frequency, usually by a factor of 5 to 10. If lower bandwidth is desired, the RHPZ can be ignored, and so can $H_e(s)$ in Equation 3. This design uses ceramic output capacitors, so the ESR zero also can be ignored. Now the control equations simplify to

$$G_{PS}(s) = \frac{g_M \times R_{LOAD} \times (1-D)}{2 \times \left(1+\frac{s}{2\pi \times f_P}\right)}. \quad (5)$$

Equations 3 and 5 are modified, using g_M (the compensation to output-current gain in A/V) instead of R_{SENSE}, with $g_M = 1/R_{SENSE}$.

Designing a negative boost regulator

It has been established that the forward transfer function simplifies to a single-pole system as described by Equation 5. A real control-loop example can be based on a design using TI's TPS54020EVM082, with V_{IN} = –2.0 V, V_{OUT} = –3.0 V, and I_{OUT} = 6 A. This electrical design can be reconfigured as a negative boost regulator consistent with the circuit in Figure 3, using many of the same components as in the EVM design. The terms "input" and "output" from here on refer to the boost mode input and output. Equation 4 can be used to calculate the minimum RHPZ as 32 kHz. The goal of the control-loop design is to have a unity-gain crossover at 1.0 kHz, so the effects of both the ESR zero and the RHPZ can be ignored.

Table 1 contains some specific parameters and values. Equation 6 uses these values to describe the forward transfer function:

$$G_{PS}(s) = \frac{R_{LOAD} \times 5.70}{1 + \frac{s \times R_{LOAD}}{13889}} \quad (6)$$

The Bode plot of $G_{PS}(s)$ is depicted in Figure 5 for four different load-resistance values. Note that the pole location and low-frequency gain are functions of load resistance. Also note that the gain slope does not vary after the pole (driven by C_{OUT}). Before the pole, the gain is dependent on the load, with the highest-frequency pole at the maximum load (minimum R_{LOAD}). A 0.5-Ω load (I_{LOAD} = 6.0 A) results in a pole at 4.4 kHz. It can also be seen that the RHPZ causes the gain to rise and the phase to fall, which makes compensation impossible and requires crossover to occur before the effect of the RHPZ becomes detrimental.

The plan for this design is to have unity gain in the open-loop transfer function at 1.0 kHz. The plant has a gain of approximately +9 dB at 1.0 kHz. This forward transfer function can be compensated easily with an integrator followed by a zero at the highest $G_{PS}(s)$ pole frequency, and with an overall gain that results in about –9 dB at the desired crossover of 1.0 kHz (+9 dB + –9 dB = 0 dB). This compensation approximates a single-pole rolloff characteristic through crossover and results in sufficient phase margin.

Bode stability criteria

A closed-loop system with negative feedback has a transfer function as in Equation 7:

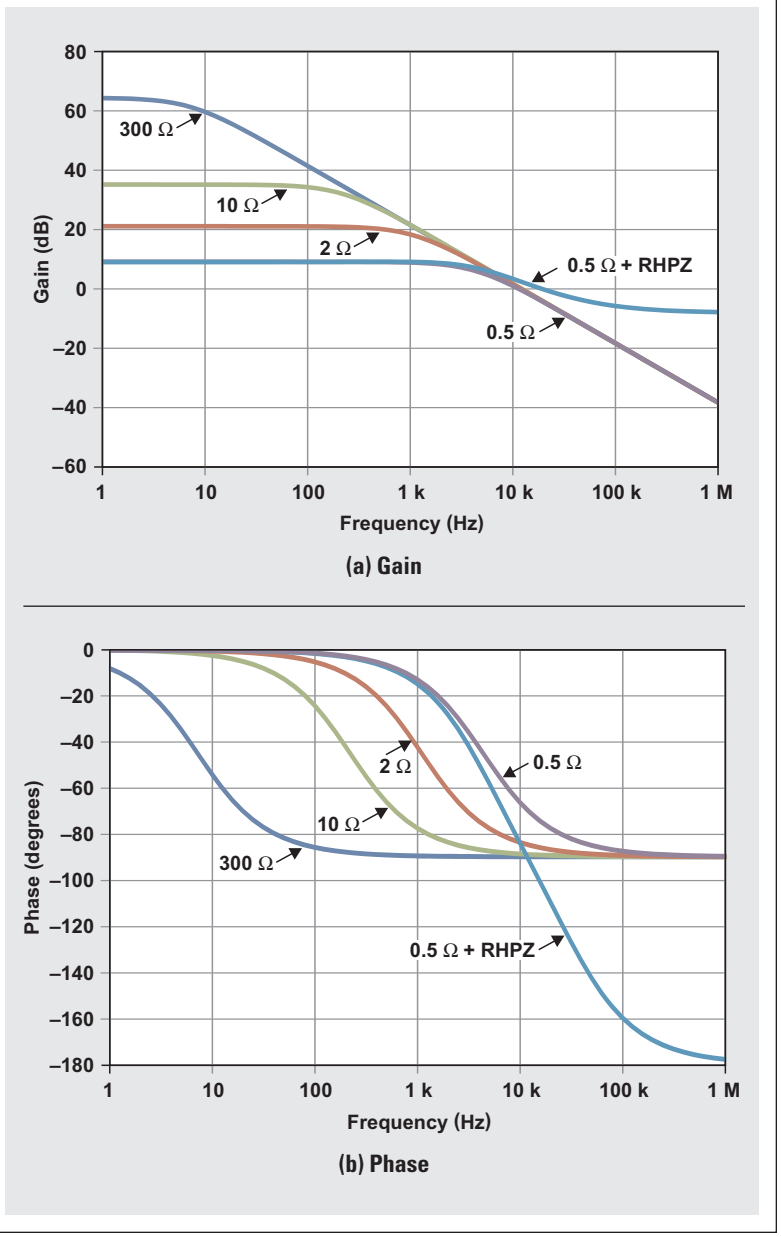
$$Y(s) = \frac{G(s)}{1 + G(s)H(s)}, \quad (7)$$

where G(s) is the forward (plant) transfer function, H(s) is the negative feedback control, and G(s)H(s) is the open-loop transfer function. The Bode stability criteria state that Y(s) is rational except where G(s)H(s) = –1. In the latter case, Y(s) is infinite and unstable. Two things have to happen at the same time for instability to occur. First, |G(s)H(s)| must equal 1 (gain = 0 dB); second, the phase of G(s)H(s) must equal –180°, corresponding to –1. Bode plots, including both the phase margin and the gain margin, are used to evaluate how near to this condition a control design approaches. Phase margin is defined as the phase difference between G(s)H(s) and –180° when the gain equals 0 dB, and gain margin refers to the negative gain when the phase equals –180°. A phase margin greater than 45° is generally considered good in power-supply design.

Table 1. Design values and TPS54020 datasheet[3] parameters for negative boost regulator

PARAMETER	COMMENTS
C_{OUT} = 144 µF	
L = 1.1 µH	
g_M = 17 A/V = 1/R_{SENSE}	g_M from datasheet = I_{SWITCH}/V_{COMP}
g_{EA} = 0.0013 A/V	From datasheet
D = (V_{OUT} – V_{IN})/V_{OUT} = 0.33	
V_{REF} = 0.600 V	From datasheet
R_{10} = 10.0 kΩ; R_7 = 40.2 kΩ	Feedback-divider gain = 0.2 V/V

Figure 5. Bode plots of $G_{PS}(s)$ for four different load resistances



Error-amplifier compensation

The error amplifier (EA) is depicted in Figure 6, and the circuit's transfer function is described by

$$G_{EA}(s) = \frac{g_{EA}R_{10}}{R_{10}+R_7} \times \frac{1}{C_1+C_{15}} \times \frac{1}{s} \times \frac{C_{15}R_1 s+1}{\frac{C_1C_{15}}{C_1+C_{15}} \times R_1 s+1}. \quad (8)$$

Note that the transfer function of the transconductance error amplifier includes the feedback-divider gain. If this was a voltage-feedback error amplifier, the divider would not be a gain term. Inspection of Equation 8 finds that $G_{EA}(s)$ has a pole at 0 Hz, a compensating zero at

$$f = \frac{1}{2\pi R_1 C_{15}},$$

and a higher-frequency pole at

$$f = \frac{1}{2\pi R_1 \left(\frac{C_1C_{15}}{C_1+C_{15}}\right)}.$$

Note that if the zero and pole are separated by a decade or more, then $C_{15} >> C_1$. The plan is to set the gain equal to –9 dB at 1.0 kHz, place the zero at the highest $G_{PS}(s)$ pole (4.4 kHz) to compensate the pole in the plant, and place the additional pole at some higher frequency.

Evaluating $|G_{EA}(s)|$ at f = 1.0 kHz and setting it equal to –9 dB yields $C_1 + C_{15} \approx C_{15} = 0.117$ µF. The nearest standard value of 0.10 µF is chosen. Given C_{15} and the desired zero location of 4.4 kHz, R_1 can be calculated as 360 Ω. The nearest standard value of 357 Ω is chosen. The higher-frequency pole is placed at 50 kHz. This is rather arbitrary, but this pole needs to be greater than 10 times the crossover frequency to ensure that it doesn't degrade the loop-phase margin. Adding this high-frequency pole is desirable because it keeps the loop gain decreasing at higher frequency. C_1 is calculated to be 0.01 µF. Figure 7 shows the Bode plot of the converter's final compensated loop. The predicted and measured open-loop gain and phase match closely near the 1.0-kHz unity-gain crossover.

Test data

Figure 7 also includes the measured Bode plot of the power supply with a 0.5-Ω load. There is good correlation near the 1.0-kHz crossover. The predicted waveforms in Figure 7 also include the effects of the RHPZ. The gain and phase disturbance between 1.0 kHz and 10 kHz is thought to result from a nonlinear characteristic in the controller and only begins to appear at load currents above 50%. Since this occurs above the crossover, it is inconsequential to the stability of the loop.

Figure 6. Error amplifier and compensation

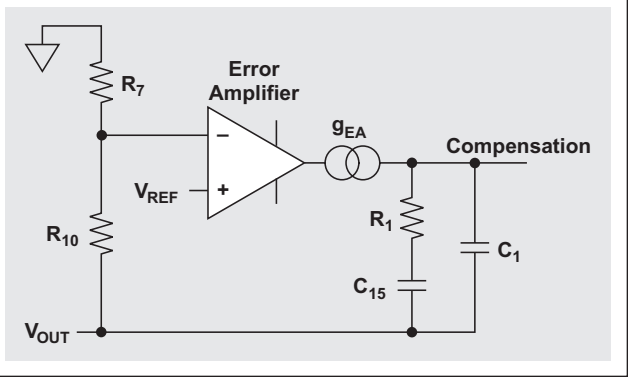


Figure 7. Bode plot of converter's final compensation loop

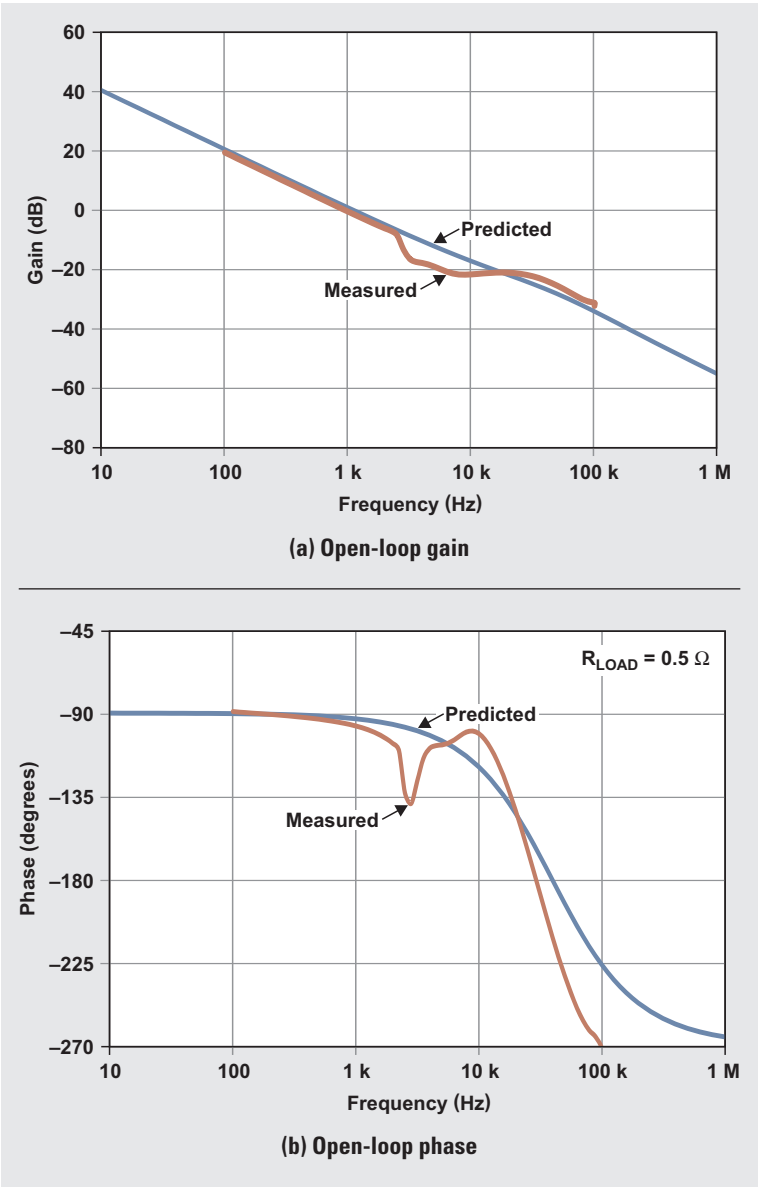
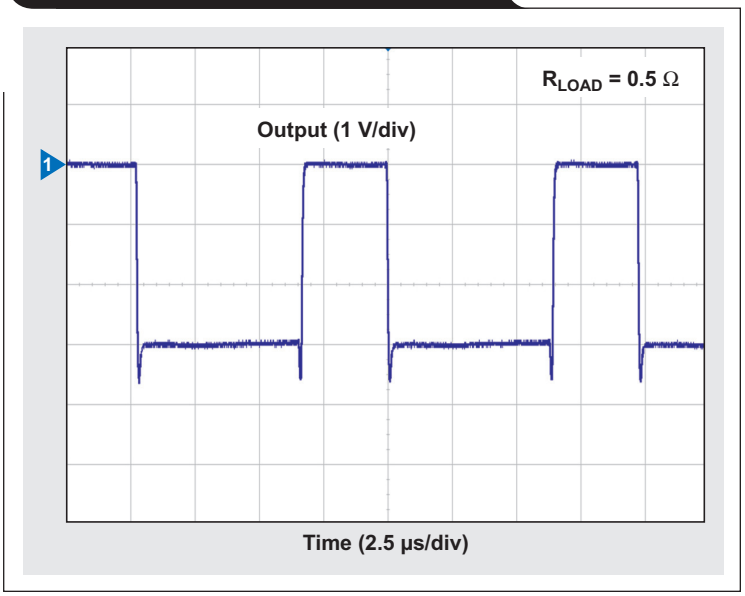


Figure 8 shows the switching waveform with a load of 0.5 Ω (6 A). As expected, it looks identical to a buck converter's switching waveform but is level shifted below ground, riding on the programmed V_{OUT} of –3.0 V.

Figure 8. Switching voltage waveform



Additional considerations

Three additional points about this type of converter should be noted. First, the TPS54020 has a separate V_{IN} and V_{DD}. This enables power conversion from a low voltage (2 V in this case), which would not be possible with many other converters. Second, this negative-boost design concept is extendable to higher voltages and is limited only by the ratings of the converter selected. Third and most important, before the boost converter starts but after voltage is applied to the PVIN pin, any load current on the boost output is conducted through the body diode of the lower FET. Although the TPS54020 functions well, starting up even with a DC current, not all devices may perform in the same way. Therefore, it might be necessary to add a Schottky diode in parallel with the lower internal FET to provide an external path for this current.

Conclusion

This article demonstrates that a positive buck regulator can be used to implement a negative boost regulator and obtain good performance. The actual performance very closely matches the expected behavior, both in real-time measurements and in the Bode plot of the control loop.

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Digital current balancing for an interleaved boost PFC

By Bosheng Sun
Systems Engineer

Introduction

A power-factor correction (PFC) converter lets the input current track the input voltage so that the load appears like a resistor to the voltage source that powers it. The most popular power topology used in active PFC is the non-isolated boost converter. For high power levels, two boost units can connect to the same bridge rectifier and operate at 180° out of phase (Figure 1). This is called two-phase interleaved PFC. By controlling two phases' inductor currents 180° out of phase, both input- and output-current ripple can be reduced. As a result, a smaller electromagnetic-interference filter can be used, which reduces material costs. Due to discrepancies between the two sets of components used in the two boost circuits, the two inductor currents inevitably will be different. This situation gets worse when PFC enters continuous-conduction mode (CCM). While the unbalanced current causes more thermal stress on one phase, it may also mistrigger over-current protection. Therefore, a current-balancing mechanism is necessary for the interleaved PFC design.[1–4]

This article discusses three different digital-control methods of balancing inductor currents. The first method senses the inductor current on each switching cycle, compares the current difference between the two phases, then adjusts the duty ratio of one phase cycle-by-cycle. The second method only adjusts the duty ratio in each half AC cycle. The third method uses two independent current loops to control each phase individually. Since these loops share the same current reference, the current is balanced automatically.

Method 1: Cycle-by-cycle duty-ratio adjustment

In this approach, a shunt is used to sense the total current. An average-current mode control is employed to force the input current to track input voltage. The pulse-width-modulation (PWM) controller generates two signals, each with the same duty ratio but shifted by 180° to drive the two boost stages. A current transformer (CT) is put right above the MOSFET in each phase to sense the switching current. The CT outputs are sampled and compared to each other; then the error is multiplied by a gain K, and the multiplier output is used to adjust the duty ratio of phase 2 accordingly. For example, if phase 1 has higher current than phase 2, the error is positive. The multiplier

Figure 1. A two-phase interleaved PFC

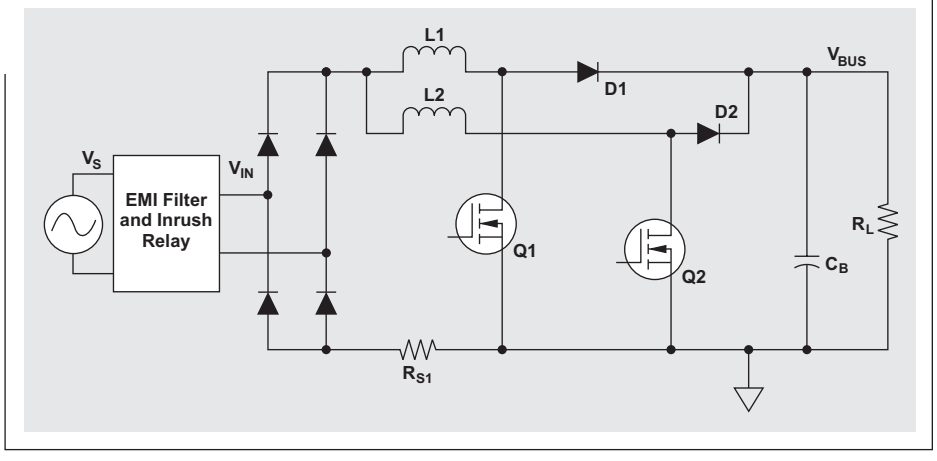
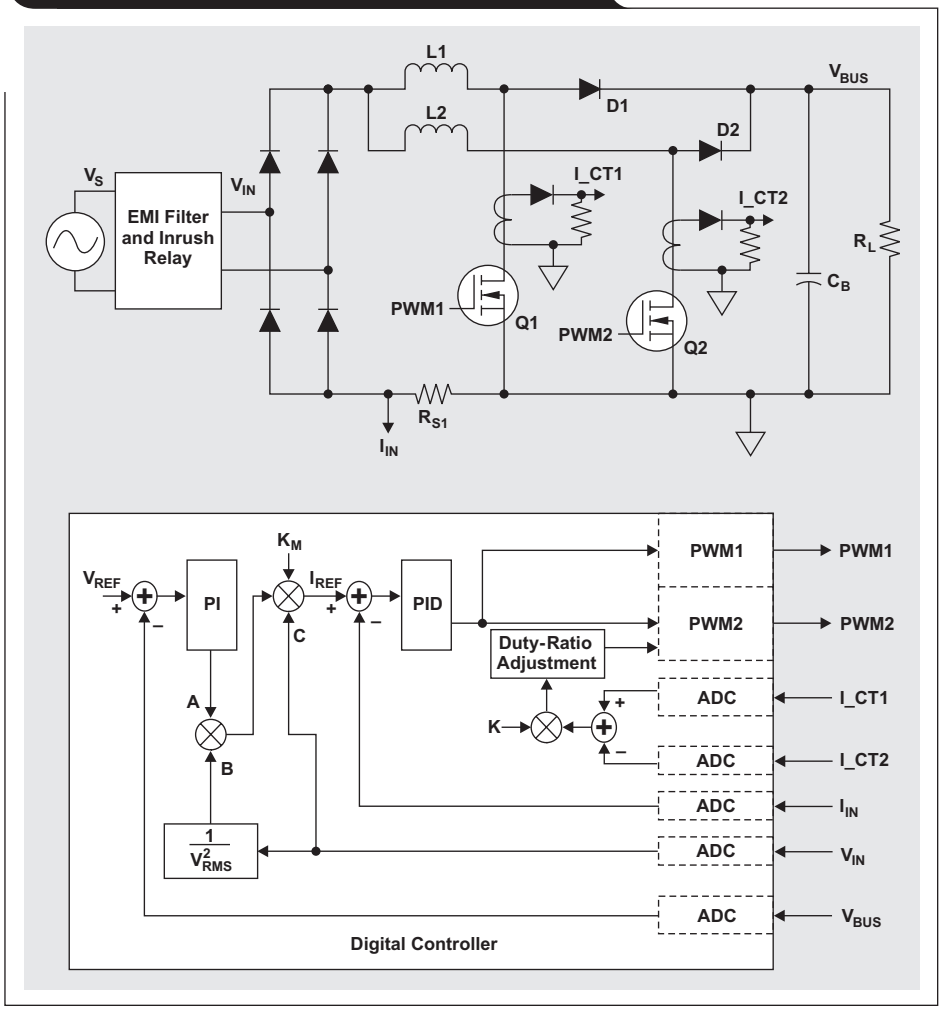


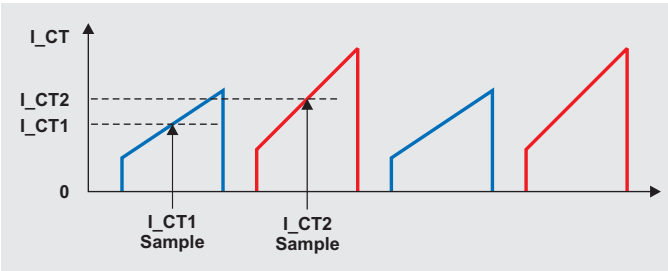
Figure 2. Cycle-by-cycle duty-ratio adjustment



output, which is also positive, increases the duty ratio of phase 2 and thus its current. This configuration is shown in Figure 2.

Properly sampling the CT currents is critical for this approach. Since the CT outputs are saw waves, both currents need to be sampled at the same point for a fair comparison. An example would be to sample both at the middle of the switch's ON time, as shown in Figure 3. Here the unbalanced current causes different magnitudes of CT output.

Figure 3. Sampling CT signal



With proper sampling of the CT currents, the cycle-by-cycle approach gives good current balancing. Figure 4 shows test results from a 360-W, digitally controlled interleaved PFC. As can be seen, there is a big difference between the inductor currents, but they almost overlap after being balanced.

Because the second-phase duty ratio is adjusted on each switching cycle, and the adjustment may be different for each cycle since the current difference may vary between cycles, this method inevitably brings high-frequency noise to the AC input current. Figure 5a shows that the waveform of the AC input current before current balancing is smooth and clean. Once current balancing is introduced, high-frequency noise appears (Figure 5b).

Method 2: Half-AC-cycle duty-ratio adjustment

Since adjusting the duty ratio on each switching cycle brings high-frequency noise to the total input current, it seems reasonable to try adjusting the duty ratio only once in each half AC cycle. Either average or peak inductor current in each half AC cycle can be used for current balancing. An example is to force the peak inductor currents to be equal in each half AC cycle by using a configuration similar to that in Figure 2. I_CT1 and I_CT2 are still sampled in each switching cycle, and the firmware finds out the peak value of I_CT1 and I_CT2 in each half AC cycle. These peak values are then compared, and the error is used to adjust the duty ratio. Since the current difference is calculated only once in each half AC cycle,

Figure 4. Inductor currents

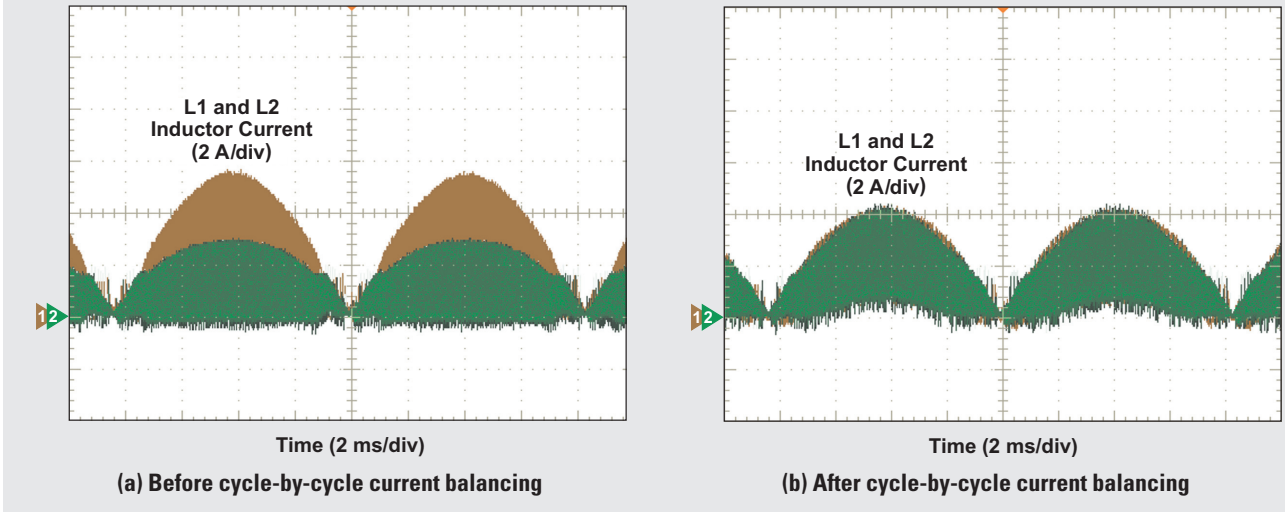
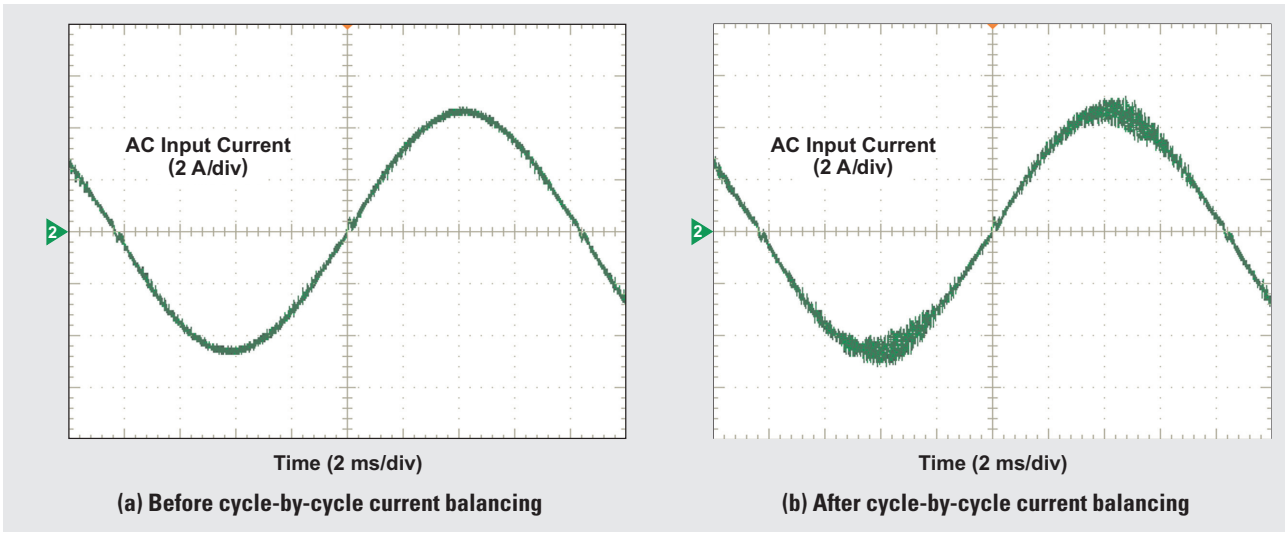


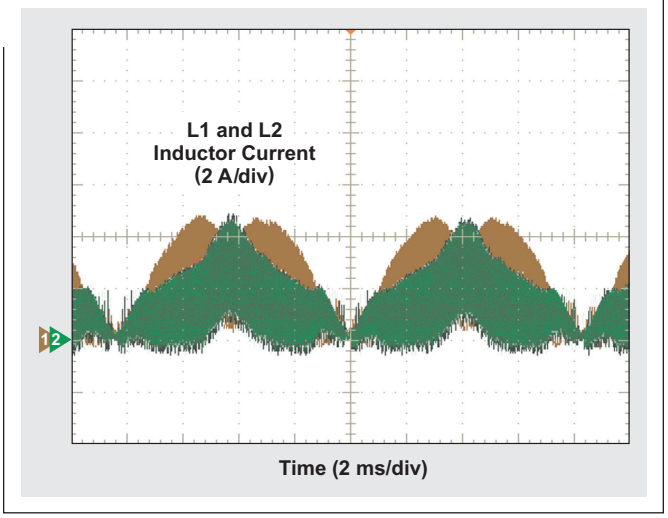
Figure 5. AC input current



the same duty-ratio adjustment is applied to the next half AC cycle. This essentially solves the issue of high-frequency noise. Test results showed that the AC current's waveform was almost the same as before current balancing was enabled; the high-frequency noise went away.

This approach also has a drawback. Because the relationship of the duty ratio to the input-current transfer function is different for continuous-conduction mode (CCM) and discontinuous-conduction mode (DCM),[5] the converter dynamics may change abruptly. Applying the same duty-ratio adjustment along the half AC cycle distorts the inductor current (Figure 6) even though the total input current is still sinusoidal. Moreover, because of discrepancies between the two component sets used in the two boost circuits, the circuits enter CCM at different points in each half AC cycle. Thus, the distortions of the two phases are also different. On the other hand, unlike the unbalanced currents in Figure 4a, this approach can force the peak values of inductor currents in each half AC cycle to be equal, so the current does get balanced to some level.

Figure 6. Inductor currents after half-AC-cycle current balancing



Method 3: Dual current-control loops

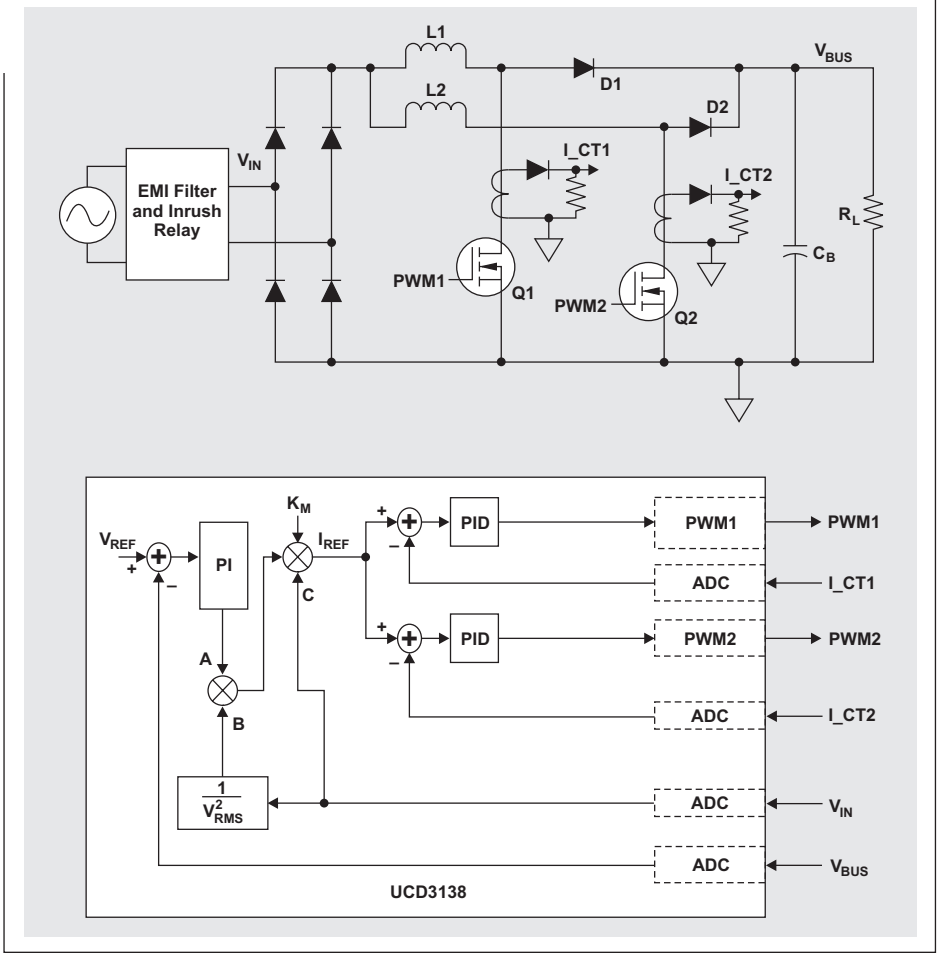
In the preceding approaches, there is only one current-control loop. The total current is used for current-loop control, and the two phases get the same duty ratio from the same control loop. If two current-control loops with the same current reference are used, with each controlling one phase individually, the closed-loop control will force the current to be balanced automatically, making duty-ratio adjustments unnecessary.

For analog controllers, adding one more loop means adding another compensation network and another feedback pin. Inevitably, this increases the cost and design effort. With a general digital controller, the current-control loop is implemented by firmware. Adding a second loop means adding extra code, which at first seems to be a good solution. However, the extra code takes extra CPU execution time. The CPU that used to do only one loop calculation now needs to do two. For this to happen without causing any interruption overflow, the CPU speed needs to be increased. This requires a higher-cost CPU with more power consumption. Another choice can be to reduce the control-loop speed—for example, from 50 kHz to 25 kHz. The CPU speed can then be kept the same, and the dual-loop calculation can be completed without causing any interruption overflow. However, the loop bandwidth suffers due to the reduced control-loop speed, and a reduced bandwidth deteriorates PFC performance.

Integrated control solution

A second-generation digital controller such as the Texas Instruments UCD3138 offers a different solution. This is a fully programmable digital controller, but the control loop is implemented by hardware. Based on the proportional integral derivative (PID), the control loop is a two-pole, two-zero digital compensator. All the loop calculations are done by hardware with a speed of up to 2 MHz. The firmware just needs to configure the PID coefficients. This allows a low-speed CPU to be used because it needs to do only the low-speed tasks, such as housekeeping and communication. Moreover, the UCD3138 has three independent loops inside the chip, so the dual current-control loops can be implemented without any extra hardware or a

Figure 7. Dual current-control loops with UCD3138



higher-speed CPU. Figure 7 shows the configuration of these dual control loops implemented with the UCD3138. The current-feedback signal from each phase needs to be measured. Normally, a CT placed above the MOSFET can be used. Since no current shunt is needed, this configuration also can improve efficiency.

Because the CT is placed right above each switch (Figure 7), it senses only the switching current. This is only the rising part of the inductor current, whereas each current loop controls the average inductor current. The CT current signal is still sampled at the middle of the PWM ON time (Figure 3). It is an instantaneous value, represented as I_{SENSE} in Figures 8 and 9. The sampled switching current (I_{SENSE}) is equal to the average PFC inductor current only when the current is continuous (Figure 8). When the current becomes discontinuous (Figure 9), I_{SENSE} is no longer equal to the average PFC inductor current. In order to control the average inductor current, the relationship between the middle point where I_{SENSE} is sampled and the average inductor current over a switching period needs to be derived and applicable to both CCM and DCM.

Figure 8. Sensed current waveform at CCM

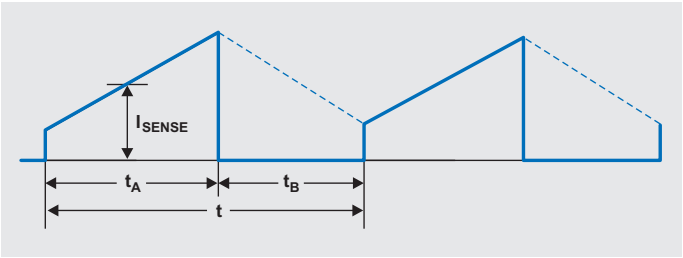
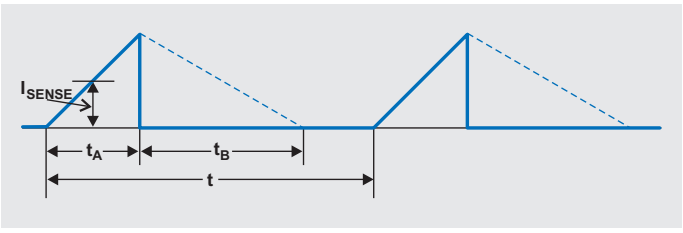


Figure 9. Sensed current waveform at DCM



For a boost-type converter in steady-state operation, the volt-second of the boost inductor maintains balance in each switching period:

$$t_{..} \times V \quad = t \quad \times \left(V \quad - V \quad \right), \tag{1}$$

where t_A is the current rising time (PWM ON time), t_B is the current falling time (PWM OFF time), V_{IN} is input voltage, and V_{OUT} is output voltage, assuming all power devices are ideal. From Figures 8 and 9, the average inductor current (I_{AVE}) can be calculated in terms of I_{SENSE}:

$$I_{AVE} = I_{SENSE} \times \frac{t_A + t_B}{t}, \tag{2}$$

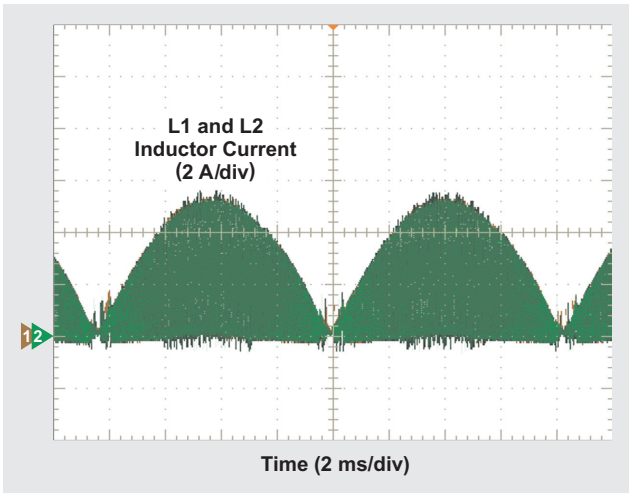
where t is the switching period. Combining Equations 1 and 2 results in

$$I_{SENSE} = \frac{I_{AVE} \times t \times \left(V_{OUT} - V_{IN} \right)}{t_A \times V_{OUT}}. \tag{3}$$

Through Equation 3, the average inductor current (I_{AVE}) is interpreted via instantaneous switching current (I_{SENSE}). I_{AVE} is the desired current, and I_{SENSE} is the current reference for the current-control loops. The real instantaneous switching currents are sensed and compared with this reference, and the error is sent to the current-control loops.

Figure 10 shows the test result of this approach. As shown in Figure 4, even though the two inductor currents have a wide variance, they almost overlap completely after current balancing is enabled. Meanwhile, the total AC current remains smooth and clean.

Figure 10. Inductor currents balanced with UCD3138 dual control loops



Conclusion

Three different digital-control methods of balancing inductor currents have been evaluated for an interleaved boost PFC. By comparing the current difference and adjusting the duty ratio cycle-by-cycle, the current can be balanced very well. However, this method also injects high-frequency noise into the total input current. Adjusting the duty ratio only once in each half AC cycle eliminates the high-frequency noise, but each individual inductor current gets distorted even though the total AC current is sinusoidal. A better approach is to use two current loops, with each controlling one phase individually. Since the two current loops share the same current reference, the current is balanced automatically. With a digital controller, the cost for a second loop is just a few extra codes. Test results show that the third approach gives the best performance.

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RS-485 failsafe biasing: Old versus new transceivers

By Thomas Kugelstadt
Senior Applications Engineer

It is incredible that an industrial interface standard such as RS-485, having been around for 30 years, still appears obscure to many industrial-network designers. While there should be plenty of literature available explaining the standard fundamentals, the Texas Instruments (TI) application team continues to receive basic questions on a weekly basis, such as how to apply failsafe biasing to an idle bus.

Failsafe biasing refers to the technique of providing a differential voltage to a terminated, idle bus in order to maintain the receiver output of a bus transceiver in a logic-high state. This technique is commonly required when legacy transceiver designs are used for designing bus networks.

Legacy designs such as transceiver X in Table 1 possess a wide input sensitivity of ±200 mV. This means that small input signals between +200 mV and –200 mV can turn the receiver output either high or low, thus making the output state indeterminate.

During a data transmission, the differential line voltage of a fully loaded bus is required to be higher than ±1.5 V, which is well above the transceiver's input sensitivity. However, during a handover of bus access from one node to another, or during a transmission pause, the bus idles. Then the low-impedance termination resistors, connecting the two conductors of the differential signal pair with each other, cause the differential bus voltage to be 0 V, right in the middle of the transceiver's input sensitivity, which produces an indeterminate output.

Therefore, to keep the receiver outputs at a logic high during bus idling, a positive, differential failsafe voltage higher than a receiver's positive input threshold (V_{IT+}) must be applied to the bus.

Table 1 shows that the theoretically required failsafe levels decrease with the receiver's positive input threshold from one generation to the next. While transceiver X requires a minimum of +200 mV of failsafe biasing, transceivers Y and Z can do without it as their positive input thresholds are below 0 V. Unfortunately, these values apply only in noise-free environments such as laboratories or the Earth's poles, and certainly not in the harsh environments of industrial factories where RS-485 networks are commonly installed.

Differential noise induced into the bus wires can falsely trigger a receiver input if the projected noise magnitude has not been included in the failsafe voltage calculation. Using a twisted-pair bus cable helps to convert noise induced along the cable run into common-mode noise. This noise is then rejected by the receiver's differential input. However, cable irregularities as well as noise induced at the bus node connectors might contribute to differential noise that cannot be rejected by a receiver.

Figure 1 on the next page shows that when a noise signal is superimposed onto the positive input threshold levels of transceivers X and Y, the minimum hysteresis voltage determines at which noise level the receiver output will assume the wrong logic state. Table 1, in which the receiver parameters have been extracted from different datasheets, gives a minimum hysteresis level only for transceiver Z. For the two older transceivers, X and Y, only typical hysteresis values are provided. In a situation such as determining the minimum failsafe value for a worst-case scenario, typical values are meaningless. In fact, the TI application team has measured minimum hysteresis voltages for both transceivers X and Y that were nearly half the specified typical values.

Furthermore, there is the possibility that for a given transceiver the hysteresis window might be located anywhere between the positive and negative input thresholds. Hence, for a worst-case calculation, one must assume that the hysteresis window is at the uppermost positive

Table 1. Receiver input sensitivities of first-, second-, and third-generation (X, Y, and Z) transceivers

	POSITIVE-GOING INPUT THRESHOLD VOLTAGE, V_{IT+} (mV)			NEGATIVE-GOING INPUT THRESHOLD VOLTAGE, $V_{IT–}$ (mV)			INPUT HYSTERESIS VOLTAGE, V_{HYS} (mV)			
TRANSCEIVER	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	RECEIVER OUTPUT IS INDETERMINATE WHEN
X (SN65LBC176)			200	–200				50		–0.2 V < V_{AB} < 0.2 V
Y (SN65HVD12)			–10	–200				35		–0.2 V < V_{AB} < 0.01 V
Z (SN65HVD72)		–70	–20	–200	–150		50	80		–0.2 V < V_{AB} < 0.07 V

threshold limit. Therefore, to determine a sufficiently high failsafe-biasing voltage, the projected peak-to-peak noise level must be added to the positive input threshold voltage: $V_{AB(min)} = V_{IT+} + V_{N(PP\_max)}$.

For a well-balanced bus with a noise level of $V_{N(PP\_max)}$ = 50 mV, using transceiver X requires a differential failsafe voltage of $V_{AB(min)}$ = 200 mV + 50 mV = 250 mV (Figure 1).

Operating transceiver Y at the same noise level without external biasing could be risky, particularly when considering a significantly smaller minimum hysteresis than the nominal value. Again, adding the noise level to the positive input threshold provides a minimum failsafe voltage of $V_{AB(min)}$ = –10 mV + 50 mV = 40 mV.

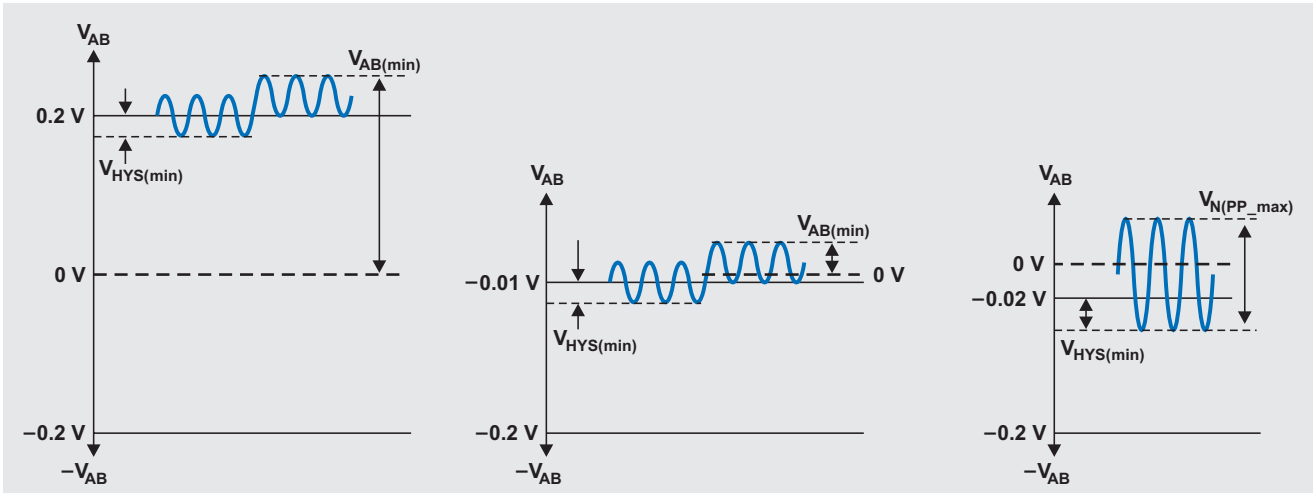
The more modern third-generation transceiver Z can maintain a stable output without failsafe biasing. Its positive input threshold of –20 mV and the specified minimum hysteresis of 50 mV allow for a maximum peak-to-peak noise level of 140 mV, which is almost three times the noise immunity of legacy devices with external biasing.

If it is not possible to use modern transceivers, the calculation methods presented in the following section can be used to optimize the failsafe-biasing networks required by legacy transceivers.

Failsafe biasing for legacy transceivers

Figure 2 shows a terminated RS-485 bus with its distributed network nodes and a failsafe-biasing network consisting of two biasing resistors (R_{FS}) and a termination resistor (R_{T1}). With the majority of RS-485 applications being master/slave systems, the failsafe-biasing network is

Figure 1. The need for failsafe biasing depends on the transceiver

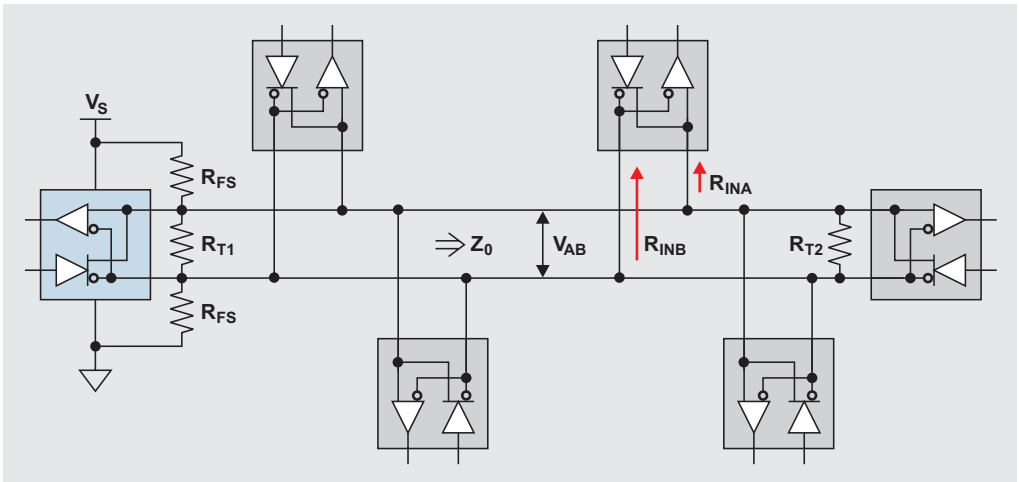


(a) Legacy transceiver X with failsafe biasing

(b) Legacy transceiver Y with failsafe biasing

(c) Modern transceiver Z does not require failsafe biasing

Figure 2. RS-485 bus with failsafe-biasing network for legacy transceivers



commonly installed at the master end of the bus, while the other cable end receives a termination resistor (R_{T2}) matching the characteristic line impedance (Z_0).

The major drawback of failsafe biasing is its common-mode loading. A common-mode load is the resistance between a signal conductor and the local transceiver ground. Transceivers have a high common-mode load, primarily because the receiver's input-voltage divider (Figure 3) reduces the input signal by a factor of 10 or more.

The internal resistor network, imposing a common-mode load on each of the A and B bus terminals, can be represented by a combined input resistance (R_{IN}). The total common-mode resistance of an entire transceiver network then can be expressed through an equivalent input resistance (R_{INEQ}) for both the A and the B line.

The RS-485 standard specifies a maximum common-mode load per bus line with 375 Ω. Initially this value is allocated for only the bus transceivers. Implementing a failsafe-biasing network can consume a significant amount of this loading, therefore allowing only a reduced number of transceivers to be connected to the bus.

Figure 4 presents a lumped equivalent circuit of an RS-485 bus. This circuit allows the failsafe resistor values to be determined as a function of the required failsafe bus voltage (V_{AB}), the supply voltage (V_S), the common-mode loading caused by R_{FS} and R_{INEQ}, and the characteristic line impedance (Z_0). Determining the currents into nodes A and B and solving for the respective line voltages (V_A and V_B) yields

$$\frac{V_S - V_A}{R_{FS}} = \frac{V_A - V_B}{R_{T1}} + \frac{V_A - V_B}{R_{T2}} + \frac{V_A}{R_{INEQ}} \Rightarrow$$

$$V_A = R_{INEQ} \times \left[\frac{V_S - V_A}{R_{FS}} - \left(V_A - V_B\right) \times \left(\frac{1}{R_{T1}} + \frac{1}{R_{T2}} \right) \right]$$

for Node A, and

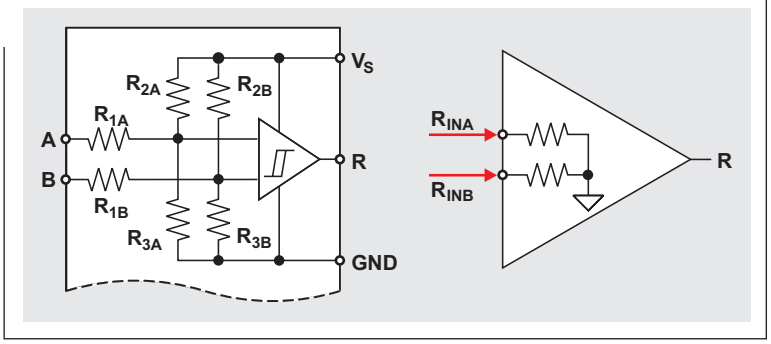
$$\frac{V_B}{R_{FS}} = \frac{V_A - V_B}{R_{T1}} + \frac{V_A - V_B}{R_{T2}} - \frac{V_B}{R_{INEQ}} \Rightarrow$$

$$V_B = R_{INEQ} \times \left[\left(V_A - V_B\right) \times \left(\frac{1}{R_{T1}} + \frac{1}{R_{T2}} \right) - \frac{V_B}{R_{FS}} \right]$$

for Node B. Allowing for the difference between the two line voltages and assuring failsafe biasing under minimum supply conditions permits the required minimum failsafe bus voltage to be determined:

$$V_{AB(min)} = \frac{V_{S(min)}}{R_{FS}} \times \frac{1}{\frac{1}{R_{INEQ}} + \frac{1}{R_{FS}} + 2\left(\frac{1}{R_{T1}} + \frac{1}{R_{T2}} \right)} \quad (1)$$

Figure 3. Common-mode input resistance of the receiver section



Because R_{FS} in combination with R_{INEQ} makes up the total common-mode load for a signal line, the parallel value of the two must not exceed the specified maximum of 375 Ω, which is expressed through

$$R_{FS} \parallel R_{INEQ} = 375\ \Omega \text{ or } \frac{1}{R_{INEQ}} + \frac{1}{R_{FS}} = \frac{1}{375\ \Omega}. \quad (2)$$

At the remote cable end, the termination resistor (R_{T2}) must match the characteristic line impedance (Z_0):

$$R_{T2} = Z_0 \text{ or } \frac{1}{R_{T2}} = \frac{1}{Z_0}. \quad (3)$$

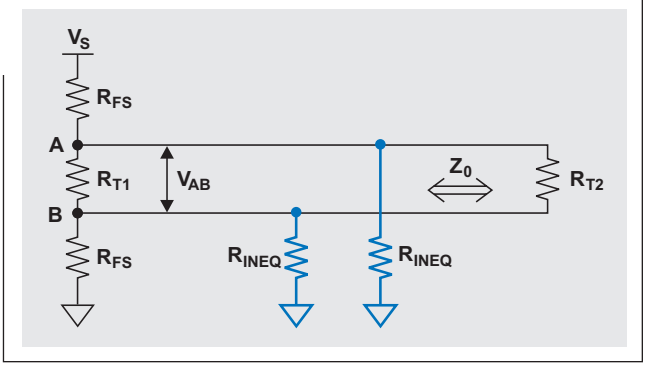
At the biasing network, the parallel combination of R_{T1} and the two failsafe resistors must also match Z_0:

$$R_{T1} \parallel 2R_{FS} = Z_0 \text{ or } \frac{1}{R_{T1}} = \frac{1}{Z_0} - \frac{1}{2R_{FS}}. \quad (4)$$

Inserting Equations 2, 3, and 4 into Equation 1 then yields the bus failsafe voltage:

$$V_{AB(min)} = \frac{V_{S(min)}}{R_{FS}\left(\frac{1}{375\ \Omega} + \frac{4}{Z_0} \right) - 1} \quad (5)$$

Figure 4. Lumped equivalent circuit



Solving Equation 5 for R_{FS} provides the value of each failsafe-biasing resistor:

$$R_{FS} = \left(\frac{V_{S(min)}}{V_{AB(min)}} + 1\right) \times \frac{1}{\frac{1}{375\ \Omega} + \frac{4}{Z_0}} \quad (6)$$

After R_{FS} is known, R_{T1} can be derived from Equation 4. Once the failsafe network has been established, the maximum number of transceivers that can be connected to the bus can be determined through

$$n \le \frac{12\ k\Omega}{UL_{XCVR}} \times \left(\frac{1}{375\ \Omega} - \frac{1}{R_{FS}}\right), \quad (7)$$

where UL_{XCVR} is the unit-load (UL) rating of the transceiver. A typical design procedure would be to calculate R_{FS} via Equation 6 first, then determine R_{T1} via Equation 4 while making $R_{T2} = Z_0$. Finally, Equation 7 would be used to calculate the maximum number of bus transceivers possible.

The design examples in Table 2 show the typical design procedure. This table also highlights the differences in failsafe biasing between a network using 1-UL, 5-V transceivers (X) and one using ⅛-UL, 3.3-V transceivers (Y).

Conclusion

Failsafe biasing with the high failsafe voltages required for first-generation transceivers causes heavy common-mode loading and necessitates a reduction in bus transceiver count. Using second-generation transceivers with less input sensitivity and lower unit loading improves the situation at low noise levels by allowing for a high transceiver count. The best of both worlds, however, can be accomplished only with modern third-generation transceivers, such as TI's 3-V SN65HVD7x family and 5-V SN65HVD8x family. These new transceivers have the following advantages:

- They don't require an external bias resistor network that can impose heavy common-mode loading on the bus, reducing the number of transceivers that can be connected to the bus.
- Therefore they allow for up to 256 transceivers on a bus.
- They tolerate high noise levels.
- They are robust against 12-kV IEC ESD and 4-kV IEC burst transients.
- They are less expensive than legacy transceivers, and some come in much smaller packages that provide cost and space savings.
- The designer doesn't have to spend time going through a mathematical treatise like the one in this article.

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2. "3.3V-supply RS-485 with IEC ESD protection," SN65HVD72/75/78 Datasheet. Available: www.ti.com/sllse11-aaj

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Table 2. Examples of how failsafe biasing affects bus transceiver count

TRANSCEIVER X	TRANSCEIVER Y
$V_{S(min)}$ = 4.75 V, V_{IT+} = 200 mV, UL_{XCVR} = 1 UL R_{T2} = 120 Ω ($R_{T2} = Z_0$)	$V_{S(min)}$ = 3.05 V, V_{IT+} = –10 mV, UL_{XCVR} = ⅛ UL R_{T2} = 120 Ω ($R_{T2} = Z_0$)
Assuming $V_{N(PP\_max)}$ = 50 mV yields: $V_{AB(min)} = V_{IT+} + V_{N(PP\_max)}$ = 250 mV	Assuming $V_{N(PP\_max)}$ = 50 mV yields: $V_{AB(min)} = V_{IT+} + V_{N(PP\_max)}$ = 40 mV
Applying Equation 6 yields: R_{FS} = 555.5 Ω. Choosing the closest E192 value makes R_{FS} = 556 Ω.	Applying Equation 6 yields: R_{FS} = 2.11 kΩ. Choosing the closest E192 value makes R_{FS} = 2.10 kΩ.
Applying Equation 4 yields: R_{T1} = 134.5 Ω. Choosing the closest E192 value makes R_{T1} = 135 Ω.	Applying Equation 4 yields: R_{T1} = 123.5 Ω. Choosing the closest E192 value makes R_{T1} = 124 Ω.
Applying Equation 7 yields: n = 10 transceivers	Applying Equation 7 yields: n = 210 transceivers

Introduction to capacitive touch-screen controllers

By Eric Siegel
Business Development Manager, Touch-Screen Controllers

Introduction

Resistive touch screens had their heyday, but their use has irrefutably declined. There are clear instances where they are no doubt better suited for low-cost designs whose users must wear gloves, such as in medical, industrial, and military environments. But capacitive touch screens have gained in popularity, and the leading smartphones and tablets on the market today incorporate capacitive touch-screen functionality.

Resistive versus capacitive touch screens

Both resistive and capacitive touch screens use indium tin oxide (ITO) sensors, but in vastly different ways. Unlike its resistive predecessor, which uses the mechanical action of human touch to connect two flexible layers of ITO together (Figure 1a), capacitive touch-screen control leverages the fact that humans are basically walking capacitors. Touching ITO changes the capacitive levels that the system can see (Figure 1b).

There are two things that give capacitive touch-screen control its edge to consumers:

1. A capacitive touch screen uses two layers, and in some cases one, of ITO. It uses a patterned sensor similar to a checkerboard (Figure 2), so it is possible to have only one full sheet covering the LCD, providing a clearer screen.
2. Since capacitive touch-screen control uses an electro-capacitive method of detection, a layer of safety glass can be placed on top of the structure to seal it, as opposed to using a flexible sheet of polyurethane for a resistive screen. This provides consumers with a more durable design.

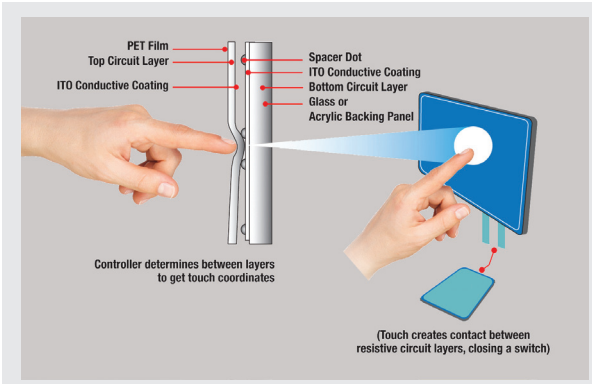
Design considerations for capacitive touch screens

There are three major issues facing designers of capacitive touch screens: power consumption, noise reduction, and gesture recognition. The remainder of this article takes a look at each of these.

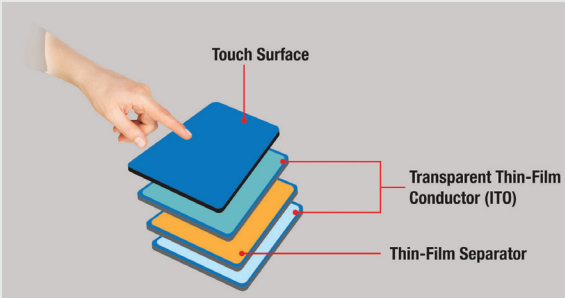
Power consumption

With so many battery-powered devices in existence today, power consumption is one of the more critical system components to consider. A device like the TSC3060 from Texas Instruments (TI) was designed with low power in mind. In typical operating conditions, it consumes less

Figure 1. Comparison of touch-screen designs

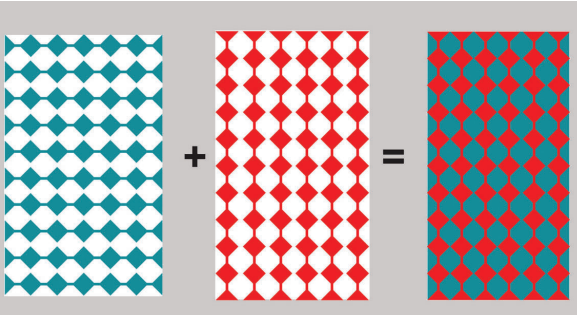


(a) Resistive touch screen



(b) Capacitive touch screen

Figure 2. ITO rows and columns are overlaid to make one full sensor sheet



than 60 mA. It can go as low as 11 µA while monitoring for a touch. This is at least one order of magnitude less than its competitors under similar operation.

Many solutions on the market were designed first as microcontrollers, then evolved into capacitive touch-screen controllers. Devices created solely as capacitive touch-screen controllers don't include the extra hardware of their predecessors that can consume extra current and clock cycles. Most systems already have a main central processor, be it a digital signal processor, a microprocessor, or a microcontroller unit (MCU). So why add another engine to a system that's finely tuned? The TSC3060 was purposely designed without a microcontroller.

Noise reduction

A superlong battery life won't matter much if the controller can't discern between actual touches and potential sources of crosstalk. A major source of noise in touch-screen designs typically comes from the LCD, which is subject to significant trade-offs in terms of quality versus cost. AC common-ground LCDs are usually cheaper but have a higher noise level. DC common-ground LCDs have a DC shield on them, thus reducing the noise generated but increasing the cost.

One typical technique to help reduce the amount of noise observed by the ITO sensor and in turn the touch-screen controller is to keep an air gap between the LCD and the ITO. This creates some distance between the two and reduces crosstalk interaction. Another way to deal with noise is to use filters. For example, the TSC3060 includes a set of programmable mixed-signal filters for noise reduction. These filters are implemented into the hardware via an integrated MCU. This means they will execute their task at hand faster than a filter in the software could. The faster response to real touch coordinates can also potentially reduce overall system resource consumption.

Gesture recognition

The final design concern is gesture recognition. Gestures don't have to be grand, complicated flourishes. A gesture is as simple as a single finger swipe. A system host MCU can easily recognize simple gestures like pinch, pull, zoom, rotate, and double and triple tap, and can do object rejection "in house." Adding a specialty engine for gesture recognition just increases power consumption in favor of what is potentially only a small reduction in system MCU bandwidth processing. In addition, the specialty engine may accomplish gesture recognition by running proprietary algorithms that designers aren't allowed to see. A device like the TSC3060 pushes this task to the host processor, which is already present in the system and allows designers the freedom to develop their own royalty-free algorithms to tweak as they see fit.

Conclusion

This article has compared some of the features and benefits of resistive and capacitive touch-screen controllers and has explained why the latter are gaining in popularity. It has also presented the three main considerations in designing touch-screen controllers—power consumption, noise reduction, and gesture recognition—and has offered some possible solutions.

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