High-Performance Analog Products

Analog Applications Journal

Fourth Quarter, 2012

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Introduction

Analog Applications Journal is a collection of analog application articles designed to give readers a basic understanding of TI products and to provide simple but practical examples for typical applications. Written not only for design engineers but also for engineering managers, technicians, system designers and marketing and sales personnel, the book emphasizes general application concepts over lengthy mathematical analyses.

These applications are not intended as "how-to" instructions for specific circuits but as examples of how devices could be used to solve specific design requirements. Readers will find tutorial information as well as practical engineering solutions on components from the following categories:

- Data Acquisition
- Power Management
- Interface (Data Transmission)
- Amplifiers: Audio
- Amplifiers: Op Amps
- Low-Power RF
- General Interest

Where applicable, readers will also find software routines and program structures. Finally, *Analog Applications Journal* includes helpful hints and rules of thumb to guide readers in preparing for their design.

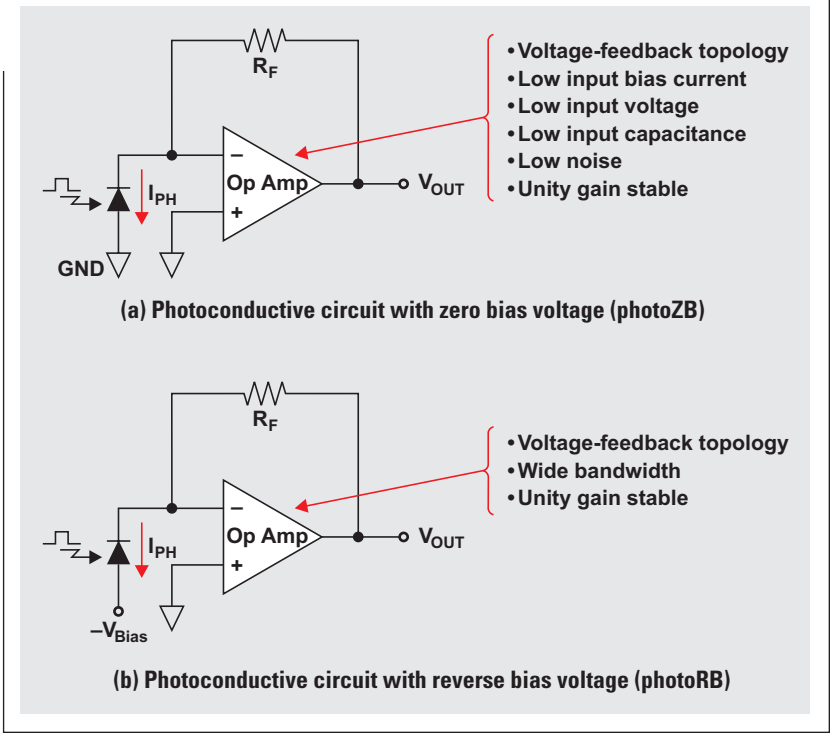
WEBENCH® tools and the photodetector's stability

By Bonnie C. Baker
WEBENCH Applications Engineer

The first priority for a photosensing application is to design good stability into the transimpedance amplifier circuit. The Texas Instruments developers of WEBENCH® designer tools have conscientiously provided photosensing designs with stable 60° phase margins, or an approximate 8.7% overshoot from a step-input signal.

WEBENCH Designer tools have powerful software algorithms and visual interfaces that deliver complete power, lighting, and sensing applications in seconds. This enables the user to make value-based comparisons at a system and supply-chain level before a design is committed. One tool among others embedded in the WEBENCH environment is the photodiode portion of Sensor Designer. This article is specifically about the WEBENCH Sensor Designer's built-in photodiode circuit stability.

Figure 1. Photodiode preamp configurations



The consequence of not paying attention to stability

A wide variety of light-sensing applications use photodiode preamplifier (preamp) circuits. These circuits convert the light information from an LED or light source into a useful voltage. With precision photoconductive circuits with zero bias voltage (photoZB) and high-speed photoconductive circuits with negative or reverse bias voltage (photoRB), the designed-in circuit phase margin can be critical. A few of the precision photoZB applications where photodiode preamps are used include CT scanners, blood analyzers, smoke detectors, and position sensors. These precision circuits require voltage-feedback amplifiers that have low input bias current, low offset voltage, and low noise. The less precise photoRB applications that depend on sensing digital light signals include bar-code scanners and fiber-optic receivers. These higher-speed application circuits require voltage-feedback amplifiers that have wider bandwidths.

The simplest way to design a photodiode preamp circuit is to put the photodiode across the amplifier inputs, ground the non-inverting input, and place a resistor in the feedback loop. One can then configure the light-sensing photodiode with or without a bias voltage. In the precision photoZB configuration (Figure 1a), the input amplifier needs to have a FET or CMOS input structure with low input bias current and low offset voltage. In this circuit, the photodiode cathode is connected to the amplifier's inverting input, and the photodiode anode is connected to ground. This circuit places a zero bias across the photodiode sensor. Notice the direction of current I_{PH} with respect to the photodiode's anode and cathode.

If digital speed and fast response times are important, the photoRB configuration (Figure 1b) uses the photodiode with a reverse bias voltage. This reverse bias voltage creates a leakage current across the photodiode. However, the parasitic capacitance across the photodiode is considerably lower compared to the photoZB configuration. This reduction in the photodiode capacitance increases the circuit's bandwidth. The amplifiers used for a reverse-biased photodiode preamp configuration can have FET, CMOS, or bipolar inputs; but the higher the amplifier's bandwidth is, the better.

In either configuration, incident light on the photodiode causes the current (I_{PH}) to flow through the diode from cathode to anode. That current also flows through the feedback resistor, R_F, causing a voltage drop across the

resistor. The amplifier's input stage keeps the amplifier's inverting input near virtual ground.

The simple solutions in Figures 1a and 1b are often destined for failure. Figure 2 shows how a step-input light signal can create a horrible ringing at the amplifier's output, V_{OUT}. With luck, it is possible that this photosensing circuit may not ring, but it is best to understand and compensate for this stability problem.

In Figure 3, the added capacitance, C_F, in the feedback loop changes the circuit's overall phase margin and removes oscillation from the output signal. However, this simple solution overcompensates by setting the value of C_F too high, causing the amplifier's output to move too slowly.

In photoZB applications, the overcompensation in Figure 3 may be acceptable, but this circuit consumes more power and has higher noise than a properly compensated circuit. With respect to photoRB applications, this circuit response is unacceptable because it does not produce a good square-wave response. Since photoRB circuits rely on clean digital square-wave signals, the configurations in Figures 2 and 3 both clearly require attention to create good compensation.

Figure 2. Uncompensated photoZB photodiode circuit

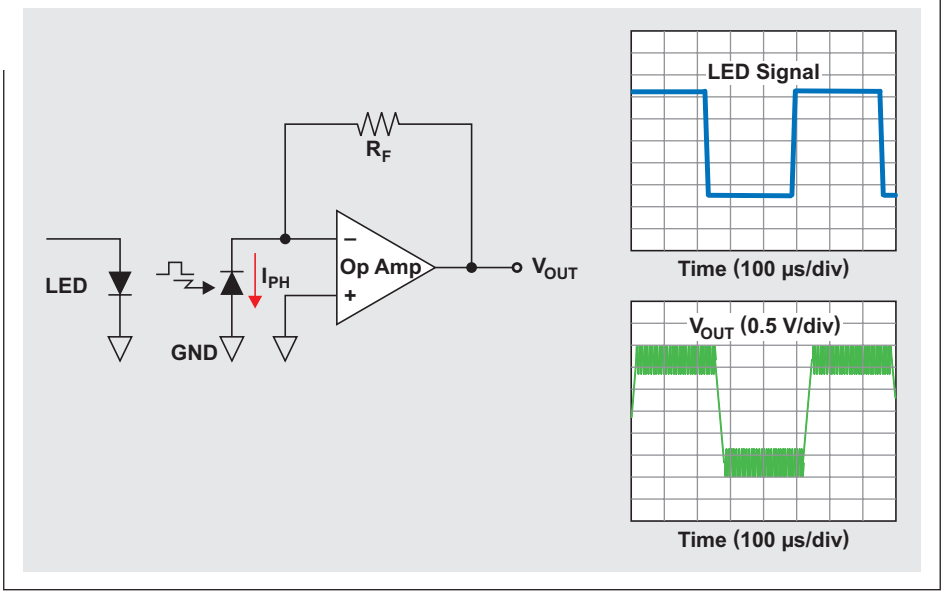
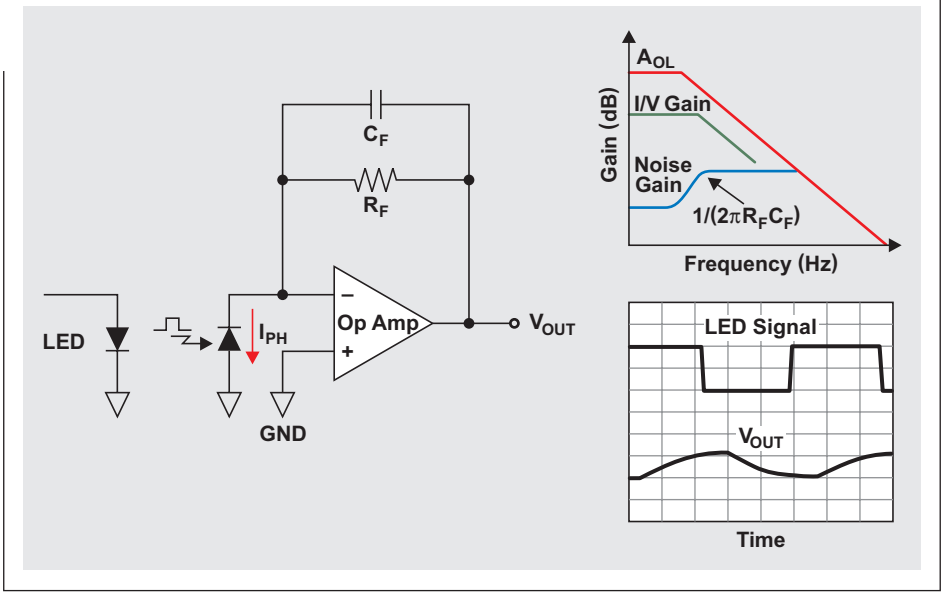


Figure 3. Overly compensated photodiode circuit

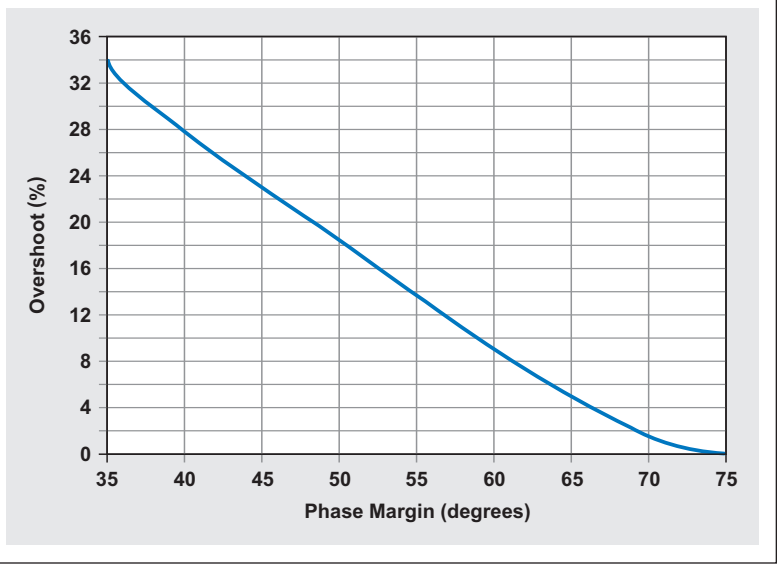


Elements at play in photodiode compensation

The target phase margin for this transimpedance amplifier is 60°. For a step response, this phase margin produces an 8.7% overshoot (Figure 4). Some designers will say that the proper phase margin for this two-pole system is 45°. As Figure 4 shows, the step response of a circuit with a 45° phase margin is 22.5%. Theoretically, both phase margins will produce stable circuits; however, they do not take into account the variations in amplifier bandwidth, resistance, capacitance, and stray capacitance. These kinds of variations can have a dramatically negative impact on the circuit with a 45° phase margin.

Proper compensation of the simple circuit in Figure 3 requires a clear understanding of the capacitive and resistive elements at play. Figure 5 shows a system model that includes a feedback network (R_F and C_F) and an operational amplifier. The following discussion will show how combining all the capacitive elements can directly impact this circuit's frequency response. WEBENCH Sensor Designer can be used to design for good system stability before the hardware is implemented, or manual precalculations can be performed.

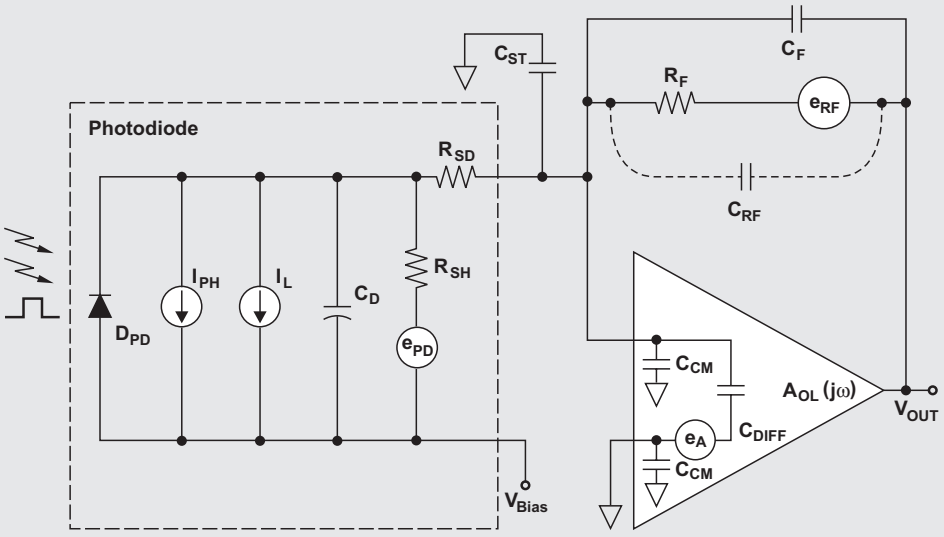
Figure 4. Overshoot response versus phase margin



The transfer function for the two-pole system circuit in Figure 5 is

$$V_{OUT} = \frac{I_{PD} \times R_F}{1 + 1/\left[A_{OL}(j\omega) \times \beta\right]},$$

Figure 5. System model of photodetector circuit



D_{PD} = Ideal photodiode
I_{PH} = Current generated by light
I_L = Leakage current
C_D = Device capacitance
e_{PD} = Device voltage noise
R_{SD} = Device lead resistance
R_{SH} = Device parallel resistance
C_{ST} = Stray capacitance
R_F = Feedback resistor
C_F = Feedback capacitor
e_{RF}, e_A = Resistor and amplifier voltage noise
C_{RF} = Parasitic capacitance of feedback resistor
C_{CM} = Common-mode amplifier capacitance
$A_{OL}(j\omega)$ = Amplifier open-loop gain
C_{DIFF} = Differential amplifier capacitance

where β is the inverse of the noise gain, or

$$\beta = \frac{1}{1 + Z_{IN}/Z_F}.$$

Z_{IN} is the input network impedance, or

$$Z_{IN} = R_{SH} \left\| j\omega\left(C_D + C_{CM} + C_{DIFF} + C_{ST}\right).\right.$$

Z_F is the feedback network impedance, or

$$Z_F = R_F \left\| j\omega\left(C_{RF} + C_F\right).\right.$$

Applying some algebra yields the following equations for system pole frequency, f_p, and system zero frequency, f_z, respectively:

$$f_p = \frac{1}{2\pi R_F C_F}$$

$$f_z = \frac{1}{2\pi \times \left(\frac{R_F \times R_{SH}}{R_F + R_{SH}}\right) \times \left(C_D + C_{CM} + C_{DIFF} + C_{ST} + C_F\right)}$$

Figure 6 graphically shows the system's frequency response. In this diagram, f_i is the intercept frequency between the feedback system (1/β) and the amplifier open-loop gain (A_{OL}). The frequency f_{BW} is the gain-bandwidth product of the amplifier. In this system, the DC gain, G1, is determined by resistors R_F and R_{SH}. Note that the feedback resistor (R_F) is in the second term's numerator and that the input resistor (R_{SH}) is in the denominator. The high-frequency gain, G2, in this system depends on the capacitors in the system. Note that the second term's numerator contains the summation of the input capacitors and that the denominator contains the circuit's feedback capacitor (C_F).

Coming to terms with stability

The placement of the pole frequency (f_p) and the intercept frequency (f_i) between 1/β and A_{OL} determines the stability of this circuit. The circuit's stability is determined at the point where the feedback curve and the amplifier's open gain curve intercept. Specifically, the phase margin at f_i dictates the type and amount of ringing or overshoot the circuit produces. For instance, the circuit's phase margin is 45° if f_p is equal to f_i. A 45° phase margin produces ~22.5% of overshoot on a square-wave input signal. If the circuit's phase margin is equal to ~60°, the pole's corner frequency occurs before the intercept of the amplifier's A_{OL} curve (Figure 6). If the corner frequency of f_p is below the A_{OL} intercept frequency, it is possible to implement a phase margin of 60° into the design. A 60° phase margin produces ~8.7% of overshoot on a square-wave input signal.

Figure 6. Frequency response of photodetector circuit

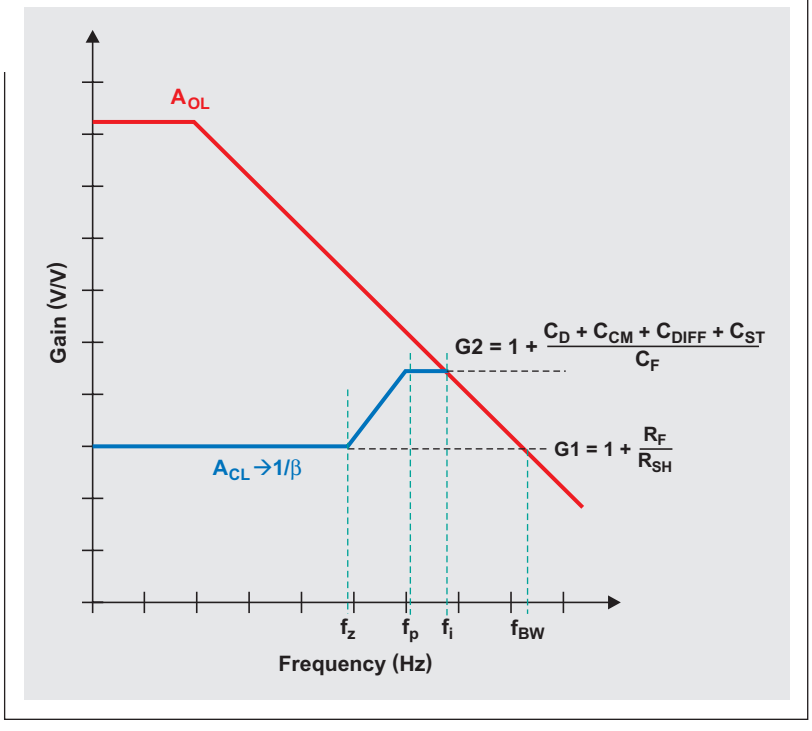
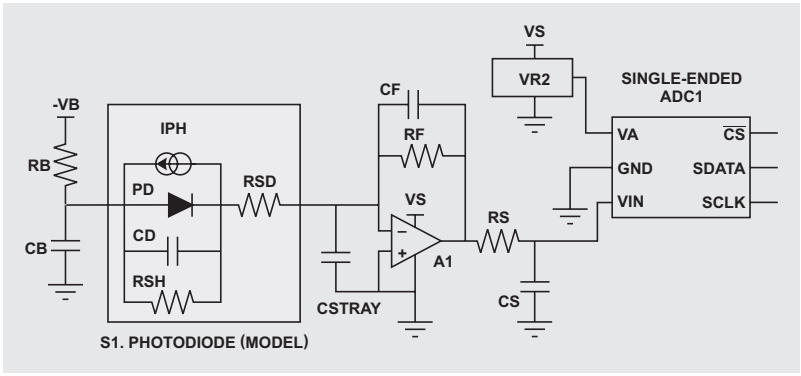


Figure 7. WEBENCH implementation of photoRB application circuit



The WEBENCH implementation

The WEBENCH implementation of the photoRB sensing network includes selecting an appropriate feedback capacitor (C_F) for the ideal 60° phase margin, selecting the proper amplifier, and following the ADC recommendations for the circuit. WEBENCH Sensor Designer provides a working circuit along with a purchasable, unpopulated printed circuit board. Figure 7 shows a block diagram of WEBENCH's photoRB system.

Conclusion

To design a photosensing circuit with good stability, there are several avenues that can be followed. WEBENCH Sensor Designer is fully equipped to provide circuits designed with stable 60° phase margins.

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Harnessing wasted energy in 4- to 20-mA current-loop systems

By Chris Glaser
Applications Engineer

A 4- to 20-mA current-loop signal is frequently used in industrial environments to transmit measurements across long distances, such as the temperature of a process or the pressure in a tank. This type of signaling is preferred because of its simplicity, noise immunity, safety, and ability to traverse great lengths without data corruption. These current loops are also low-power systems, since relatively low currents transmit the data. Previously, whatever power was not used or lost in the signal transmission was merely dissipated in the transmitter; but now, with modern integrated circuits, even this small amount of power can be harnessed to support necessary functions in these systems.

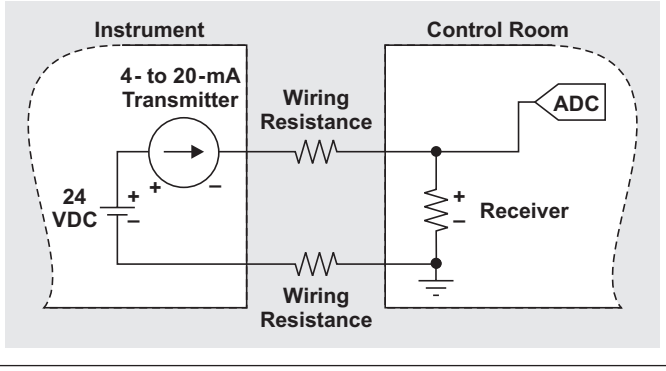
The basics of 4- to 20-mA current-loop systems

Figure 1 shows a typical 4- to 20-mA current-loop system. A semiregulated 24-VDC source provides power to the current loop and to the transmitter element. The transmitter measures the signal of interest (such as temperature, pressure, and many others) and outputs a 4- to 20-mA current that is proportional to that signal. This current passes through the wiring to a receiver system. There, the current develops a voltage across a resistor that is read by an analog-to-digital converter (ADC) and then further processed. The loop is completed with a connection back to the voltage source that powers the loop.

These current loops provide several benefits in industrial applications:

- The current loops are simple circuits requiring only a crude power supply; a transmitter to make the measurement and source the current; a wire; and a receiver circuit. The power supply needs to provide only enough voltage to overcome the various voltage drops in the system; any excess loop voltage is just dropped across the transmitter. Due to the low current, this is only a small amount of power, which creates little heat.
- The current loop contains only one loop for current flow. Therefore, from Kirchhoff's current law, the current through all the elements in the loop is equal. This provides high noise immunity, which is critical in industrial environments.
- Safety is provided since the lowest signal level is 4 mA. If something in the loop is broken or becomes disconnected, the receiver reads no current, which demonstrates a fault instead of the lowest signal level.
- As long as the power-supply voltage is high enough to overcome system voltage drops, the desired current representing the measured signal is maintained by the transmitter. Thus, smaller wire gauges with their higher voltage drops and lower cost are used for the interconnections, requiring only an increase to the supply voltage. Most importantly, the relatively large voltage drops permitted across the wiring allow a large amount of wire to be used. This allows physical separation of the instrument being measured and the control room that processes the measurement, providing safety to those in the control room.

Figure 1. Basic 4- to 20-mA current-loop system



Basic system improvement

The excess loop voltage that would otherwise be dropped across the transmitter can be harnessed and used to provide power to the receiver circuitry. Figure 2 shows a power supply inserted into the current loop. This power supply is located in the control room with the receiver circuitry it powers—efficiently converting the excess loop voltage to useful output power.

Since the receiver resistor is no longer ground-referenced, a level-shift circuit is likely necessary to interface with the data converter's input. This very simple circuit is provided by any high-side current-shunt monitor, such as the Texas Instruments (TI) INA138. These devices measure very small sense-resistor voltage drops at a common-mode voltage, thus lowering the necessary voltage drop across the receiver resistor. This allows more voltage for the power supply to harness, reducing the amount of wasted energy.

The power supply typically provides a regulated 3.3 V to power this level shifter, the data converter, and any other low-power devices in the control room. Examples of these devices are a microprocessor from TI's MSP430™ platform to review the incoming data and make decisions, and possibly a low-power RF device from TI's CC430 family to wirelessly transmit the data to other locations. A wireless transmitter is particularly useful if its cost is offset by savings from not having to buy and install the wire required for a particularly lengthy current loop. These devices must use very low power due to the limited amount of excess energy harnessed from the current loop.

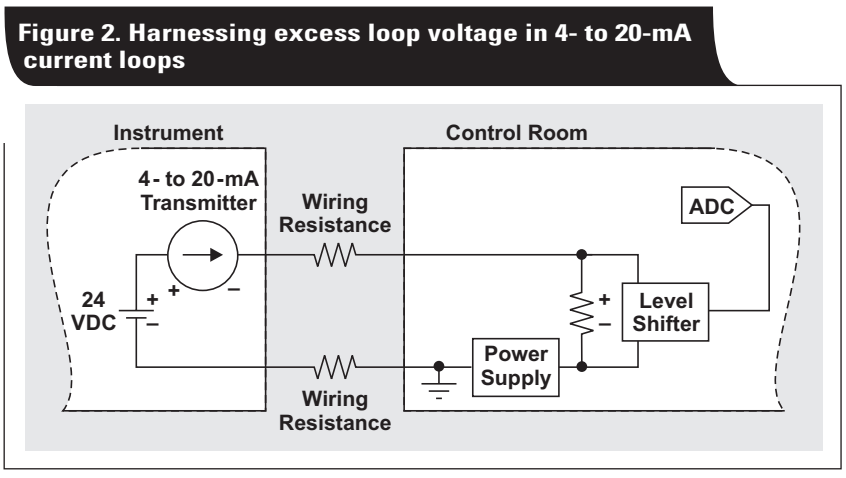
Finally, the power supply must be able to operate with such a low-power source—4 mA being the minimum current, and 20 mA being the most it ever gets. Since the voltage generated by this current is the excess voltage in the loop, the power supply must accept a wide input-voltage range and still provide a regulated output. What is more difficult for the power supply is starting up the system from such a current-limited source. Typically, a higher output power is required during start-up to charge up the output capacitors and provide the load with its start-up current. This can be much higher than what the system consumes in normal operation. If the power supply attempts to provide this higher power during start-up, its input power can exceed what the current loop provides. If this happens, the voltage into the power supply drops until the power supply turns off. Then, its input voltage rises again until it turns back on and repeats the process. Such start-up oscillations are a difficult challenge to be overcome when the power supply runs from such small amounts of input power.

Energy-harnessing solution

As just described, the energy-harnessing power supply must have a wide input-voltage range, be able to operate on a very small amount of input power, and avoid start-up oscillations when powered from current-limited sources. TI's TPS62125 is such a power supply, because it operates from a 3- to 17-V input, requires only 11 µA to operate, and has a programmable enable threshold voltage with adjustable hysteresis. The circuit recommended in the TPS62125 datasheet is used with three small modifications:

1. A 15-V Zener diode is added on the input to the device to protect it in cases where the excess loop voltage applied to it exceeds its 17-V rating. If a lower-voltage current-loop system is used, this diode may not be necessary. A Zener diode that clamps at a maximum of 15.6 V gives good results.
2. Bulk capacitance is added on the input to the device to store enough energy for start-up and load changes. Depending on the load's power demands during start-up, this capacitor may not be needed at all. A total of about 200 µF provides a smooth start-up for the example load, which draws 50 mA at 3.3 V for 30 ms at start-up, and 10 mA once started. The bulk capacitance also provides stored energy for periodic higher power demands that might occur, such as for measuring a temperature, taking a reading with the data converter, or transmitting the data via an antenna.

Figure 2. Harnessing excess loop voltage in 4- to 20-mA current loops



3. The device's enable threshold voltage is adjusted such that the device turns on when its voltage reaches 12 V. The device is programmed to turn off if its input drops down to 4 V. Once enabled, the device efficiently converts the harnessed energy to its 3.3-V output.

For an example power-supply solution, 4 V was chosen as the turn-off voltage in order to provide the required headroom of input voltage to output voltage, allowing the device to keep the 3.3-V output regulated. A turn-on voltage of 12 V was chosen for system considerations. It was assumed that the 24-V source varied between 18 and 30 V and that the voltage dropped in the current-loop sum to a maximum of 6 V, leaving a minimum of 12 V applied to the device under worst-case conditions. Thus, 12 V was chosen as the point at which to start the power supply, since it is the minimum voltage that would ever be applied to the device. Also, 12 V achieved sufficient separation between the turn-on and turn-off voltages such that the power supply started into its higher-powered load without start-up oscillations.

The described power-supply solution starts up from and runs off of TI's XTR111, a 4- to 20-mA current-loop transmitter delivering less than 4 mA at all times. Figure 3 shows this solution's start-up. Once the transmitter is enabled, it begins sourcing current, which raises the input voltage to the 12-V turn-on point of the power supply. The power supply's output voltage ramps up into regulation and immediately supplies the load's start-up current of 50 mA. This slightly reduces the input voltage of the power supply, but the supply keeps regulating the output voltage because of its wide voltage range and bulk input capacitor. After the 30-ms duration of the load's start-up power draw, the load current reduces to a steady-state, 10-mA level. The input voltage rises further and is clamped by the Zener diode at a safe 15-V level. As already noted, the current provided by the current loop remains below 4 mA at all times.

Figure 4 shows a close-up version of Figure 3. The power supply draws stored energy from the bulk capacitor to supply the start-up load current's demands, while the current loop provides less than 4 mA at all times. Drawing this energy reduces the input voltage by about 2 V, which is acceptable for this power supply.

Figure 3. Start-up of energy-harnessing power supply

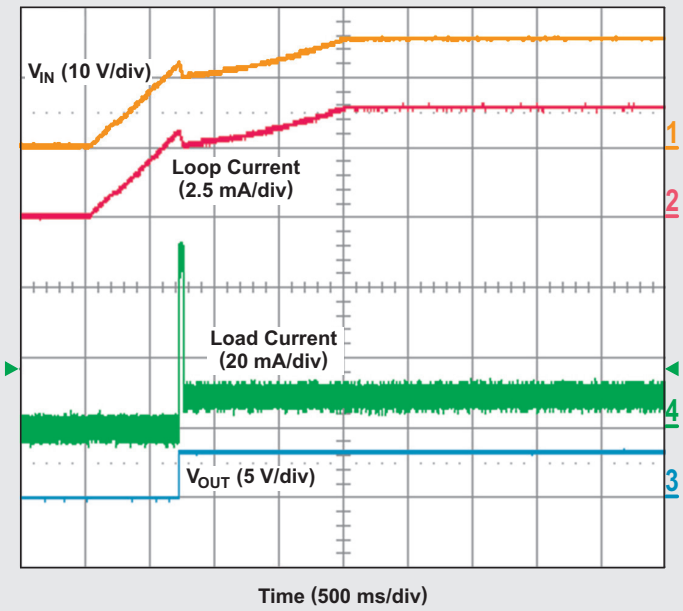
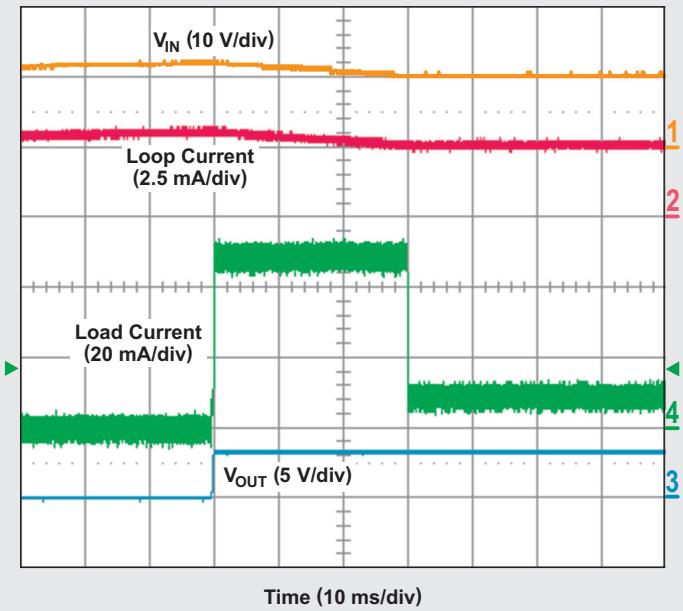


Figure 4. Energy-harnessing power supply providing load's start-up current



Finally, the energy-harnessing power supply stores enough energy in the bulk capacitor and operates over a wide enough input-voltage range to supply continuous pulses of power to the load. Figure 5 shows the supply providing 20 mA to the load for a duration of 100 ms every second, with the supply's output voltage remaining regulated.

Conclusion

In 4- to 20-mA current-loop systems, energy that otherwise would be wasted can be harnessed for useful purposes. This energy powers data converters and microprocessors that the control room needs to process the incoming data from the current loop, but it can also power low-power RF transmitters that extend the application possibilities of 4- to 20-mA current loops, as well as potentially save costs in such systems by reducing the amount of wire required. A power supply that has a wide input-voltage range, operates on very small amounts of power, and starts from current-limited sources without oscillations enables the energy to be harnessed and the continued usefulness of these systems.

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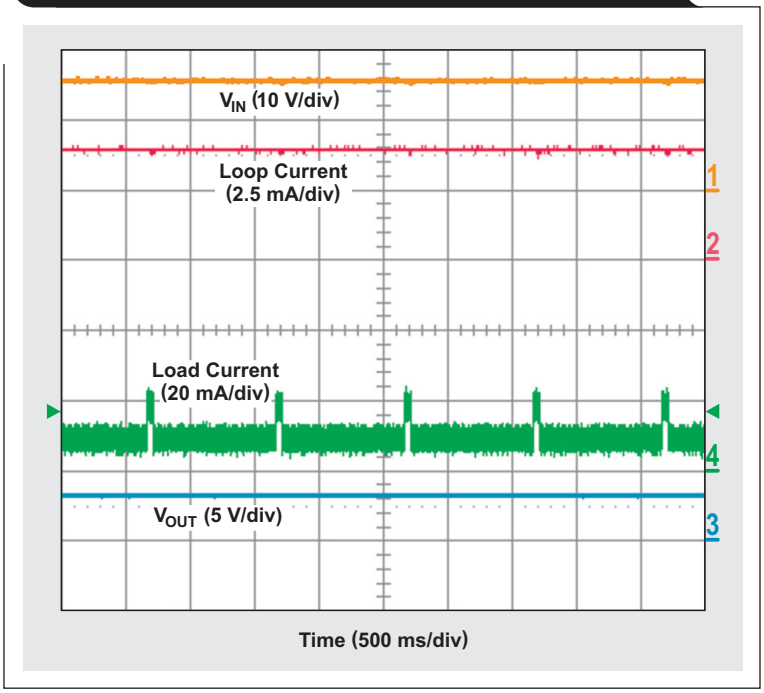
www.ti.com/msp430
www.ti.com/product/*partnumber*
Replace *partnumber* with INA138, TPS62125, or XTR111

Figure 5. Energy-harnessing power supply providing power pulses to the load



LDO noise examined in detail

By Masashi Nogawa
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Introduction

Requirements and expectations for telecommunication systems continue to evolve as complexity and reliability of the communication channels continue to increase. These communication systems rely heavily on high-performance, high-speed clocking and data-converter devices. The performance of these devices is highly dependent on the quality of system power rails. A clock or converter IC simply cannot achieve top performance when powered by a dirty power supply. Just a small amount of noise on the power supply can cause dramatic negative effects on the performance. This article examines a basic LDO topology to find its dominant noise sources and suggests ways to minimize its output noise.

A key parameter indicating the quality of a power supply is its noise output, which is commonly referred by the RMS noise measurement or by the spectral noise density. For the lowest RMS noise or the best spectral noise characteristics, a linear voltage regulator like a low-dropout voltage regulator (LDO) always has an advantage over a switching regulator. This makes it the power supply of choice for noise-critical applications.

Basic LDO topology

A simple linear voltage regulator consists of a basic control loop where a negative feedback is compared to an internal reference in order to provide a constant voltage—regardless of changes or perturbations in the input voltage, temperature, or load current.

Figure 1 shows a basic block diagram of an LDO regulator. The red arrow indicates the negative-feedback signal path. The output voltage, V_{OUT}, is divided by feedback resistors R1 and R2 to provide the feedback voltage, V_{FB}. V_{FB} is compared to the reference voltage, V_{REF}, at the negative input of the error amplifier to supply the gate-drive voltage, V_{GATE}. Finally, the error signal drives the output transistor, NFET, to regulate V_{OUT}.

A simplified analysis of noise begins with Figure 2. The blue arrow traces a subset of the loop represented by a common amplifier variation known as a voltage follower or power buffer. This voltage-follower circuit forces V_{OUT} to follow V_{REF}. V_{FB} is the error signal referring to V_{REF}. In steady state, V_{OUT} is bigger than V_{REF}, as described in Equation 1:

Figure 1. Negative-feedback loop of LDO

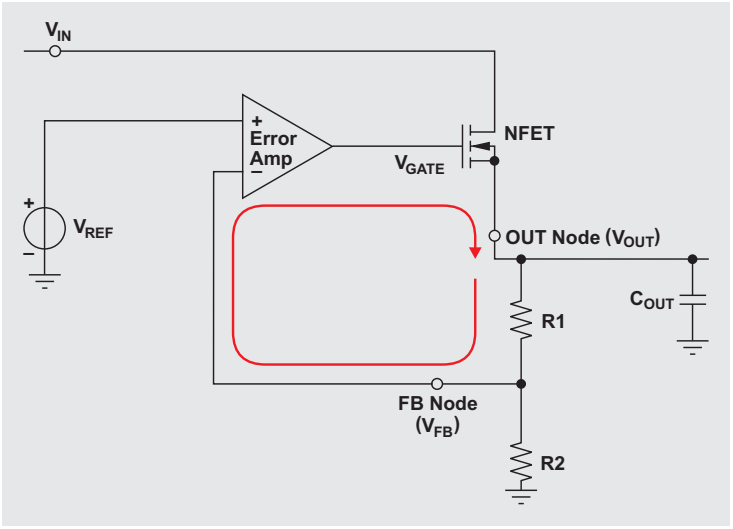
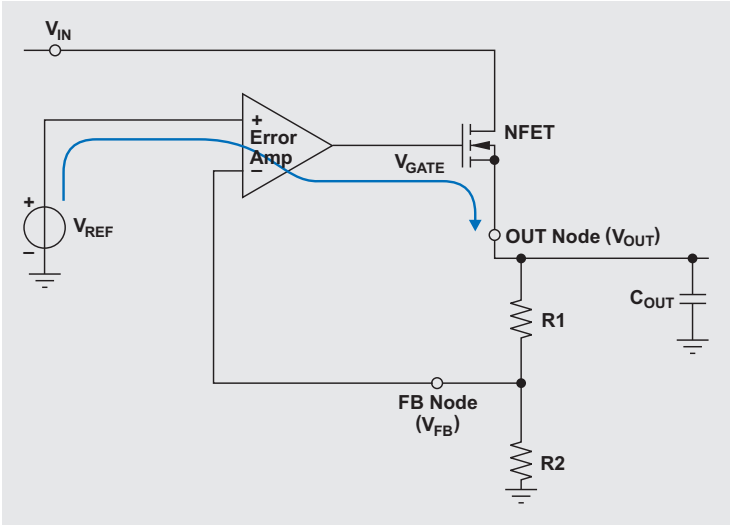


Figure 2. Reference-voltage buffering of LDO



$$V_{OUT} = \left(1 + \frac{R1}{R2}\right) \times V_{REF}, \quad (1)$$

where 1 + R1/R2 is the gain that the error amplifier must have to obtain the steady-state output voltage (V_{OUT}).

Suppose the voltage reference is not ideal and has an effective noise factor, $V_{N(REF)}$, on its DC output voltage (V_{REF}). Assuming all circuit blocks in Figure 2 are ideal, V_{OUT} becomes a function of the noise source. Equation 1 can be easily modified to account for the noise source, as described in Equation 2:

$$V_{OUT} + V_{N(OUT)} = \left(1 + \frac{R1}{R2}\right) \times (V_{REF} + V_{N(REF)}), \quad (2)$$

where $V_{N(OUT)}$ is the independent noise contribution to the output, expressed by Equation 3:

$$V_{N(OUT)} = \left(1 + \frac{R1}{R2}\right) \times V_{N(REF)} \quad (3)$$

From Equations 2 and 3, it's clear that a higher output voltage generates higher output noise. The feedback resistors, R1 and R2, set (or adjust) the output voltage, thereby setting the output noise voltage. For this reason, many LDO devices characterize the noise performance as a function of output voltage. For example, $V_N = 16\ \mu V_{RMS} \times V_{OUT}$ illustrates a standard form describing the output noise.

Dominant sources of LDO output-voltage noise

For most typical LDO devices, a dominant source of output noise is the amplified reference noise in Equation 3. This is generally true even though the total output noise is device-dependent. Figure 3 is a complete block diagram showing each equivalent-noise source corresponding to its respective circuit element. Since any device with current flowing through it is a potential noise source, every single component in Figure 1 and Figure 2 is a noise source.

Figure 4 is redrawn from Figure 3 to include all equivalent-noise sources referenced at the OUT node. The complete noise equation is

$$V_{N(OUT)} = V_{N(AMP)} + V_{N(FET)} + \left(1 + \frac{R1}{R2}\right) \times (V_{N(REF)} + V_{N(R1)} + V_{N(R2)}). \quad (4)$$

In most cases, because the reference-voltage block, or bandgap circuit, consists of many resistors, transistors, and capacitors, $V_{N(REF)}$ tends to dominate the last three noise sources in this equation where $V_{N(REF)} >> V_{N(R1)}$ or $V_{N(REF)} >> V_{N(R2)}$. Thus, Equation 4 can be simplified to

$$V_{N(OUT)} = V_{N(AMP)} + V_{N(FET)} + \left(1 + \frac{R1}{R2}\right) \times V_{N(REF)}. \quad (5)$$

Figure 3. LDO topology with equivalent-noise sources

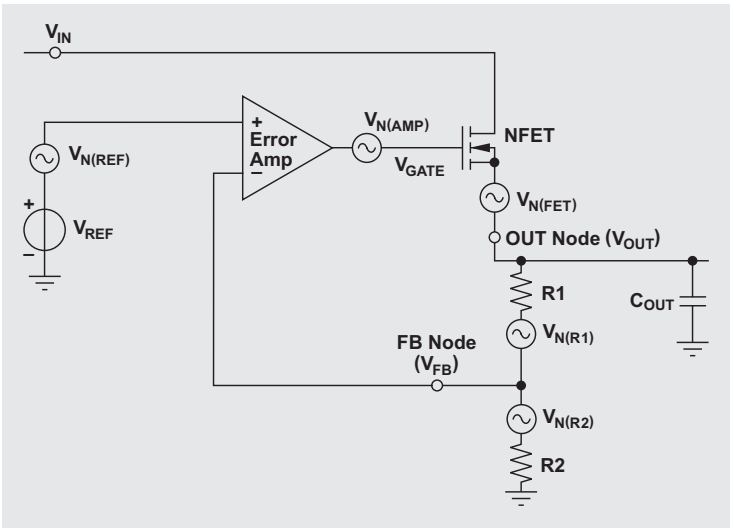
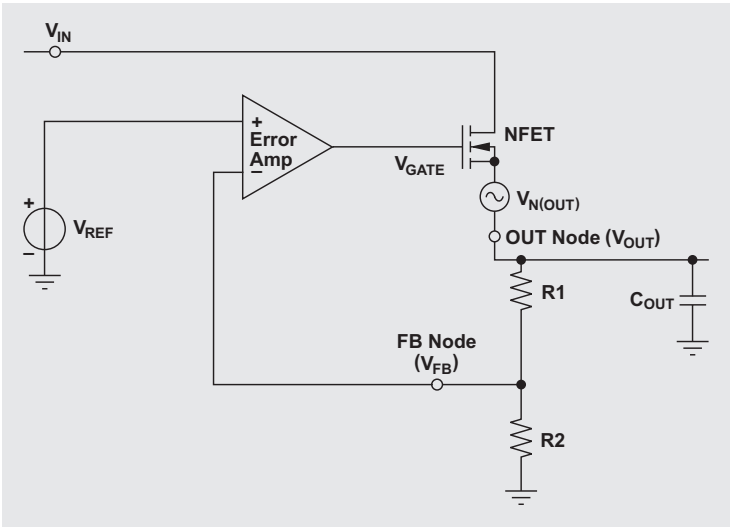


Figure 4. LDO topology with a consolidated noise source



For higher-performance LDO devices, it is common to add a noise-reduction (NR) pin to shunt reference noise to ground. Figure 5 illustrates how the NR pin works to reduce noise. Since it is known that $V_{N(REF)}$ is the dominant output-noise source, an RC filter capacitor, C_{NR}, is inserted between the reference-voltage block (V_{REF}) and the error amplifier to reduce this noise. This RC filter reduces the noise by an attenuation function of

$$G_{RC}(f) = \frac{1}{\sqrt{1+\left(f/f_p\right)^2}} < 1, \quad (6)$$

where

$$f_p = \frac{1}{2\pi \times R_{NR} \times C_{NR}}.$$

The amplified reference noise is therefore reduced to $(1 + R1/R2) \times V_{N(REF)} \times G_{RC}$, and Equation 5 then becomes

$$V_{N(OUT)} = V_{N(AMP)} + V_{N(FET)} + \left(1+\frac{R1}{R2}\right) \times V_{N(REF)} \times G_{RC}. \quad (7)$$

In the real world, all control signal levels are frequency-dependent, including the noise signal. If the error amplifier has limited bandwidth, the high-frequency reference noise ($V_{N(REF)}$) is filtered by the error amplifier in a way similar to using an RC filter. But in reality an error amplifier tends to have a very wide bandwidth, so the LDO device has very good power-supply ripple rejection (PSRR), which is another key performance parameter of high-performance LDOs. To satisfy this conflicting requirement, IC vendors settle on having a wide-bandwidth error amplifier for the best PSRR over less noise. This decision leads to using an NR pin function if low noise is also mandatory.

Figure 5. LDO topology with reference-noise filter

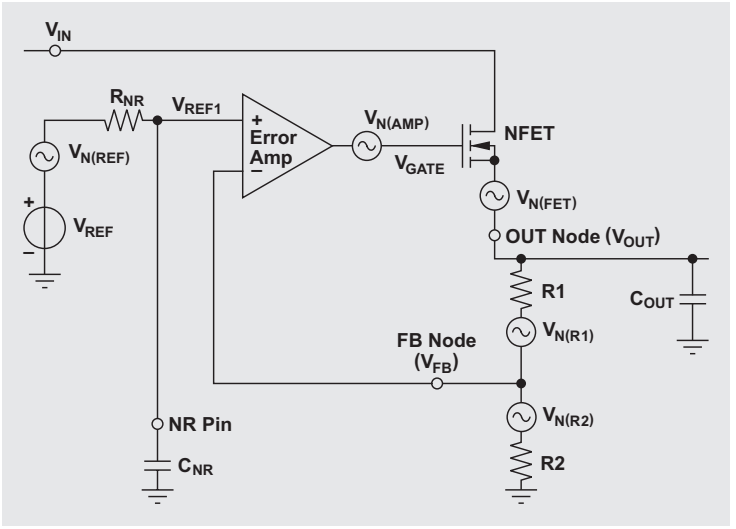
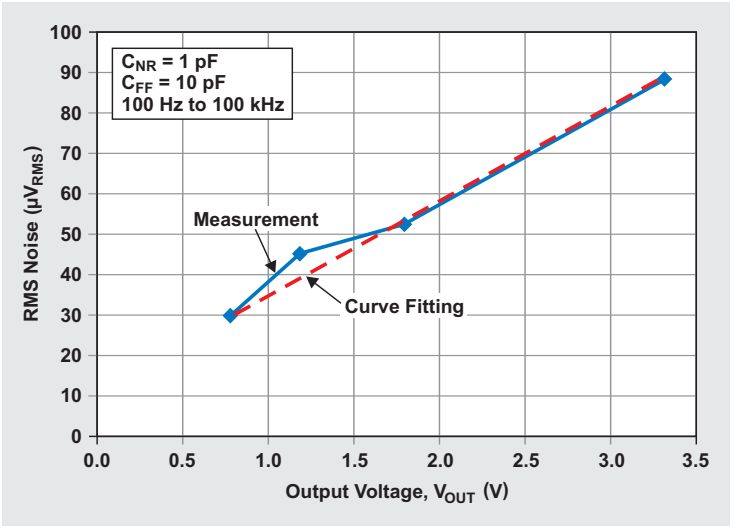


Figure 6. RMS noise versus output voltage



Controlling reference noise in a typical circuit

Amplified reference noise

The Texas Instruments (TI) TPS74401 LDO was used for testing and measurements. The common setup parameters are shown in Table 1. Please note that a soft-start capacitor, C_{SS}, in the TPS74401 datasheet[1] is referred to as a noise-reduction capacitor, C_{NR}, in this article for easier reading.

First, the effect of the amplifier gain was examined with a negligibly small C_{NR}. Figure 6 shows RMS noise versus output-voltage settings. As discussed earlier, the dominant noise source, $V_{N(REF)}$, is amplified by the ratio of the feedback resistors R1 and R2. Equation 7 can be modified into the form of Equation 8:

$$V_{N(OUT)} = V_{N(Other)} + \left(1+\frac{R1}{R2}\right) \times V_{N(REF)} \times G_{RC}, \quad (8)$$

where $V_{N(Other)}$ is the sum of all other noise sources.

Table 1. Setup parameters

$V_{IN} = V_{OUT(Target)} + 0.3$ V	$I_{OUT} = 0.5$ A		$C_{OUT} = 10$ µF
$V_{OUT(Target)}$	R1	R2	1 + R1/R2
3.3 V	31.25 kΩ	10 kΩ	4.125
1.8 V	12.5 kΩ	10 kΩ	2.25
1.2 V	5 kΩ	10 kΩ	1.5
0.8 V	0 Ω (short OUT node to FB node)	Open circuit	1

If Equation 8 is fitted to a linear curve of the form y = ax + b as shown by the red dotted line in Figure 6, $V_{N(REF)}$ (the slope term) can be estimated as 19 μV_{RMS}, and $V_{N(Other)}$ (the y-intercept term) as 10.5 μV_{RMS}. As explained

later under "Effect of the noise-reduction (NR) pin," the value of C_{NR} was chosen as 1 pF to minimize the RC-filter effect to a negligible level, and G_{RC} is treated as being equal to 1. In this situation, the basic assumption is that $V_{N(REF)}$ is the dominant noise source.

Note that the minimum noise occurs when the OUT node is shorted to the FB node, making the amplifier gain (1 + R1/R2) equal to 1 (R1 = 0) in Equation 8. Figure 6 shows this minimum-noise point to be approximately 30 μV_{RMS}.

Canceling amplified reference noise

This section explains a very effective technique for achieving a configuration with minimum output noise. A feedforward capacitor, C_{FF}, forwards (bypasses) output noise around R1 as illustrated in Figure 7. This bypass or shorting action prevents the reference noise from being increased by the gain of the error amplifier at frequencies higher than the resonant frequency, $f_{Resonant}$, of R1 and C_{FF}, where

$$f_{Resonant} = \frac{1}{2\pi \times R1 \times C_{FF}}.$$

The output noise becomes

$$V_{N(OUT)} = V_{N(Other)} + \left[1 + \frac{R1 \parallel \frac{1}{2\pi \times f \times C_{FF}}}{R2}\right] \times G_{RC} \times V_{N(REF)}. \quad (9)$$

Figure 8 shows the changes in RMS noise relative to feedforward capacitance (C_{FF}) and different output-voltage settings. Note that each point along each RMS plot represents the statistical mean of the integrated noise across the entire given bandwidth of interest for the circuit conditions described. As expected, all curves converge toward the minimum output noise of approximately 30 μV_{RMS}; in other words, the noise converges to $V_{N(REF)} + V_{N(Other)}$ due to the effect of C_{FF}.

Figure 8 illustrates that, for a C_{FF} value greater than 100 nF, the amplifier gain of 1 + R1/R2 in Equation 8 is canceled. This is true only because the low-frequency noise does not contribute significantly to the overall statistical mean of the RMS calculation, even though that low-frequency noise is not completely canceled by C_{FF}. In order to see the actual effect of C_{FF}, it is necessary to look

Figure 7. LDO topology with feedforward capacitor (C_{FF}) for minimizing noise

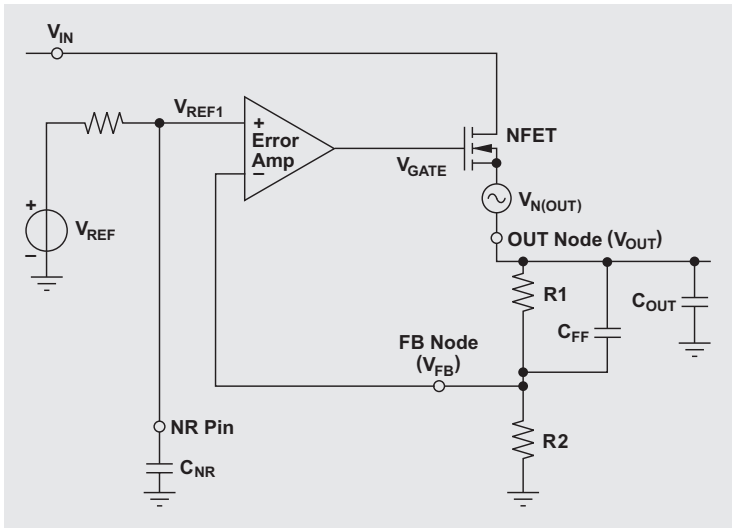
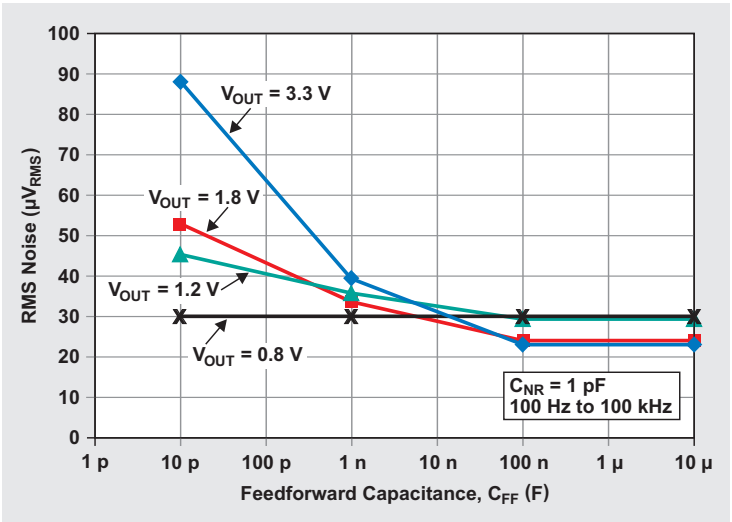


Figure 8. Effects of feedforward capacitance on noise



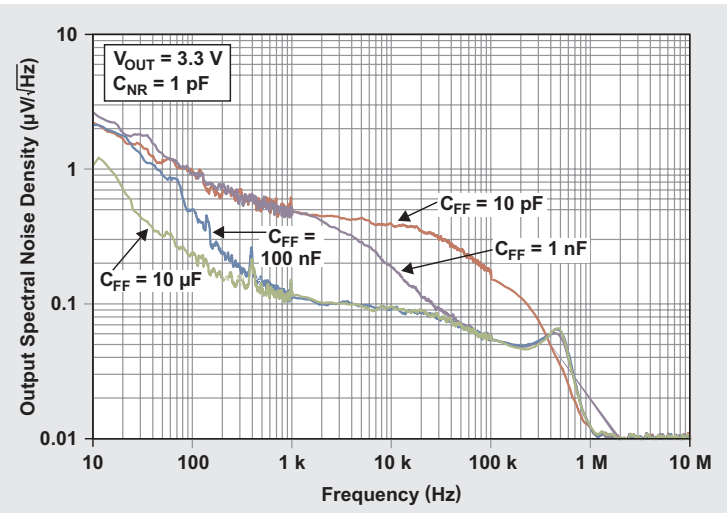
at the actual spectral-density plot of the noise voltage (Figure 9). Figure 9 shows that there is minimum noise at the curve of C_{FF} = 10 µF but that all curves approach this minimum noise curve above certain frequencies. Those certain frequencies correspond to the resonant pole frequencies determined by the R1 and C_{FF} values. See Table 2 for the calculated C_{FF} values with an R1 value of 31.6 kΩ.

Table 2. Calculated resonant frequencies

	C_{FF} = 10 pF	C_{FF} = 1 nF	C_{FF} = 100 nF	C_{FF} = 10 µF
$f_{Resonant}$	504 kHz	5.04 kHz	50.4 Hz	0.504 Hz

Figure 9 shows that the curve of C_{FF} = 100 nF rolls off around 50 Hz. The curve for C_{FF} = 1 nF rolls off around 5 kHz, but the resonant frequency for when C_{FF} = 10 pF is obscured by the overall internal effects on the LDO noise. Given these observations of Figure 9, it is assumed for the rest of this discussion that C_{FF} = 10 µF to minimize noise.

Figure 9. Output spectral noise density for various C_{FF} values



Effect of the noise-reduction (NR) pin

G_{RC} decreases when the RC filter capacitor (C_{NR}) is used between the NR pin and ground. Figure 10 shows RMS noise as a function of C_{NR} (see Figure 5). The difference between the two curves is examined later in the third paragraph under "Other technical considerations."

A wider integration range of 10 Hz to 100 kHz is used in Figure 10 to capture the performance difference in the low-frequency region. With C_{NR} = 1 pF, both curves show very high RMS noise values. Although not shown in Figure 10, there is no RMS noise difference whether C_{NR} = 1 pF or not. This is why G_{RC} is treated as being equal to 1 in the earlier section, "Amplified reference noise."

As expected, RMS noise gets lower as C_{NR} increases, and converges toward the minimum output noise of approximately 12.5 μV_{RMS} when C_{NR} = 1 µF.

For a C_{FF} of 10 µF, the amplifier gain (1 + R1/R2) can be ignored. Thus, Equation 8 can be simplified to

$$V_{N(OUT)} = V_{N(Other)} + V_{N(REF)} \times G_{RC}. \quad \textbf{(10)}$$

As seen, $V_{N(Other)}$ is not affected by C_{NR}. Therefore C_{NR} remains 10.5 μV_{RMS} as was determined by the data-curve fit in Figure 6. Equation 10 can be expressed as

$$V_{N(OUT)} = V_{N(REF)} \times G_{RC} + 10.5\,\mu V.$$

Next, it is important to determine the effect of noise-reduction capacitance on G_{RC}. The minimum measured noise along the curve in Figure 10 allows Equation 10 to be rewritten as

$$V_{N(OUT)} = 12.5\,\mu V = V_{N(REF)} \times G_{RC} + 10.5\,\mu V, \quad \textbf{(11)}$$

where $V_{N(REF)} \times G_{RC}$ is solved to equal 2 μV_{RMS}. Adding C_{NR} decreases the reference noise from 19.5 μV_{RMS} to 2 μV_{RMS}, which is to say that G_{RC} has decreased from unity to an average of 0.1 (2/19.5) over the frequency range of 10 Hz to 100 kHz.

Figure 10. RMS noise versus noise-reduction capacitance

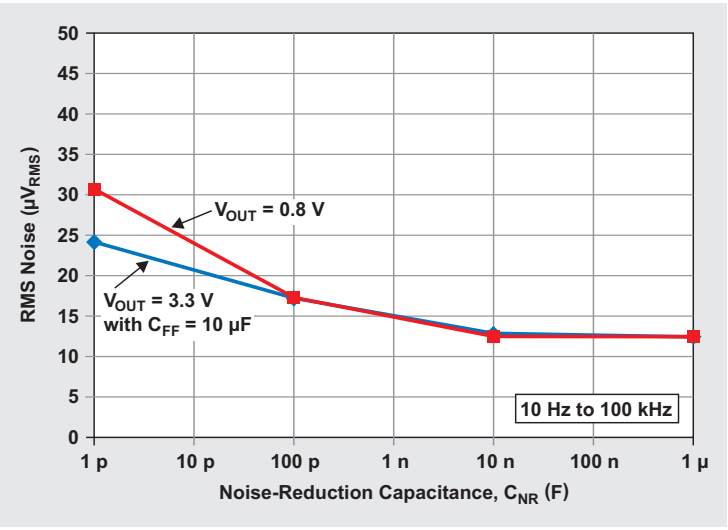


Figure 11 shows how C_{NR} reduces noise in the frequency domain. Just like the smaller C_{FF} values in Figure 9, a smaller C_{NR} starts working at a higher frequency. Note that the biggest C_{NR} value, 1 µF, shows the lowest noise. Though the curve for C_{NR} = 10 nF shows almost minimum noise close to the curve for C_{NR} = 1 µF, the 10-nF curve shows a small hump between 30 and 100 Hz.

The curves in Figure 8, where C_{NR} = 1 pF, can be improved to those in Figure 12, where C_{NR} = 1 µF. Figure 8 shows little difference in RMS noise between C_{FF} = 100 nF and C_{FF} = 10 µF, but Figure 12 clearly shows a difference.

In Figure 12, regardless of the output voltage, values of C_{FF} = 10 µF and C_{NR} = 1 µF bring the lowest noise, 12.5 μV_{RMS}, which is to say that the minimum G_{RC} value (in other words, the maximum effect of the RC filter) is 0.1. This value of 12.5 μV_{RMS} is the noise floor of the TI device TPS74401.

When a new LDO device is used for noise-sensitive applications, it is good practice to figure out a noise floor unique to the device by using large C_{FF} and C_{NR} capacitors. Figure 12 indicates that an RMS-noise curve converges at the noise-floor value.

Figure 11. Output spectral noise density versus frequency for various C_{NR} values

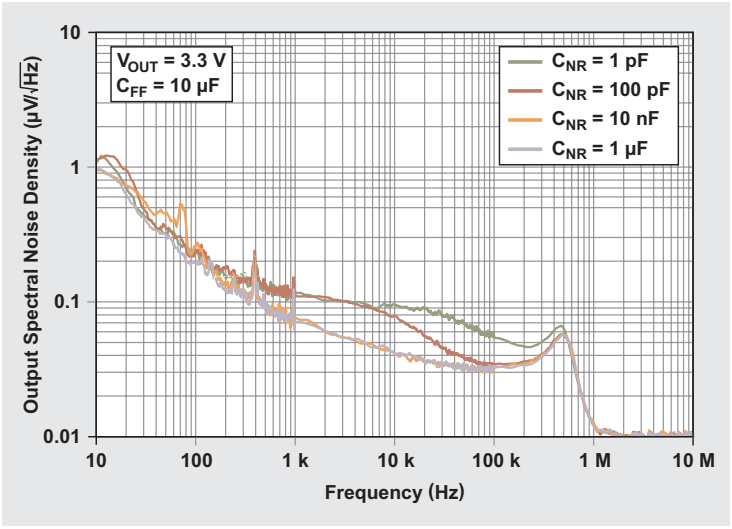
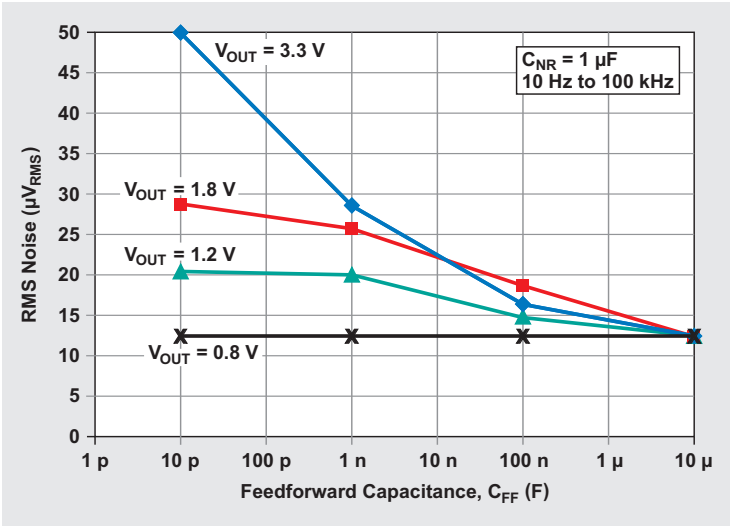


Figure 12. RMS noise versus feedforward capacitance after noise optimization



Other technical considerations

Slow-start effect of noise-reduction capacitor

Besides its ability to reduce noise, an RC filter is also known to work as an RC delay circuit. Therefore, a big C_{NR} value causes a big delay of the regulator's reference voltage.

Slow-start effect of feedforward capacitor

The same mechanism whereby C_{FF} bypasses the AC signal across the R1 feedback resistor also bypasses the output-voltage feedback information when V_{OUT} is ramping up after an enable event. Until C_{FF} is fully charged, an error amplifier takes a bigger negative feedback signal, resulting in a slow start.

Why a higher V_{OUT} value results in less RMS noise

In Figures 8 and 10, the curve for V_{OUT} = 3.3 V shows less noise than that for V_{OUT} = 0.8 V. Since it is known that a higher voltage setting can increase the reference noise, this looks odd. The explanation is that, because C_{FF} is connected to the OUT node, C_{FF} has the effect of increasing the output-capacitor value in addition to bypassing the noise signal across resistor R1. Figure 12 shows that, as the reference noise gets minimized, this phenomenon can't be observed.

RMS-noise value

Because the noise floor of the TPS74401 is 12.5 μV_{RMS}, this device is one of the lowest-noise LDOs on the market. This absolute value of 12.5 μV_{RMS} can be a good reference to use in designing a regulator with very low noise.

Conclusion

The basic noise of an LDO device and how to minimize it have been examined, including:

- How each circuit block contributes to output noise
- How the reference voltage is the dominant source of noise, amplified by an error amplifier
- How to cancel the amplified reference noise
- How an NR function works

Careful selection of a noise-reduction capacitor (C_{NR}) and a feedforward capacitor (C_{FF}) can minimize LDO output noise to a noise-floor level unique to the device. With this noise-minimized configuration, an LDO device keeps the noise-floor value regardless of the parameters that usually affect noise in non-optimized configurations.

Due to the expected side effect of a slow start when C_{NR} and C_{FF} are added to the circuit, values for these capacitors must be chosen that will provide a fast enough ramp-up.

The method described in this article is already being used to optimize the noise of TI's TPS7A8101 LDO. On page 10 of the TPS7A8101 datasheet,[2] the device shows a constant noise value no matter what parameter is changed.

References

For more information related to this article, you can download an Acrobat® Reader® file at www.ti.com/lit/*litnumber* and replace "*litnumber*" with the **TI Lit. #** for the materials listed below.

Document Title	TI Lit. #
1. "3.0A ultra-LDO with programmable soft-start," TPS74xx Datasheet	SBVS066M
2. "Low-noise, wide-bandwidth, high PSRR, low-dropout 1-A linear regulator," TPS7A8101 Datasheet	SBVS179A

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www.ti.com/product/TPS7A8101
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Simple open-circuit protection for boost converters in LED driver applications

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Introduction

One method for driving high-brightness LEDs is to modify the standard boost-converter topology to drive a constant current through the load. However, there is a major problem with this implementation in that an open-circuit fault in the LED string removes the pathway for the load current. This creates the potential to damage the circuit due to a high-output voltage from the converter, which operates without feedback in this condition. This article presents a simple method of robust open-circuit fault protection that uses a Zener diode and a resistor with negligible changes in overall efficiency. The functionality of the topology is demonstrated by configuring a high-voltage boost converter as a constant-current driver for a string of three high-brightness white LEDs and producing a simulated fault condition at the output. The presented circuit clamps the output voltage to a safe level and reduces the output current in the protected state.

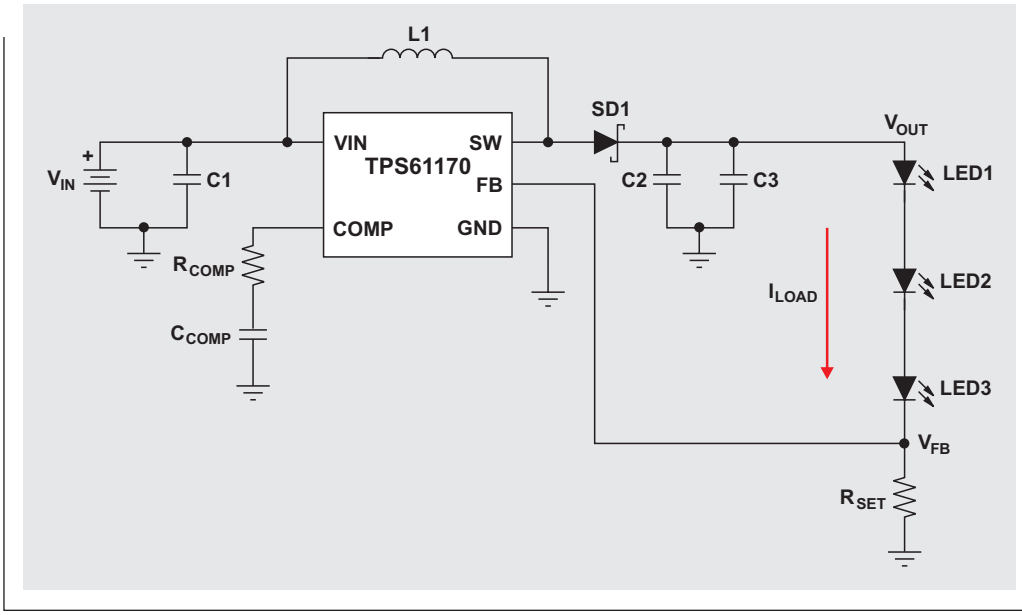
Typical boost converter for high-brightness LEDs

Boost converters are commonly modified for driving high-brightness LEDs in single-cell lithium-ion (Li-Ion), alkaline, and other applications where the voltage of the LED string exceeds the battery or rail voltage. In the standard boost configuration, the output voltage, V_{OUT}, is monitored by using a voltage divider to produce a feedback voltage, V_{FB}, for the circuit. The converter regulates the output voltage to keep V_{FB} equal to the on-chip reference voltage, V_{REF}. This topology can be adapted to maintain a constant current rather than a constant voltage by replacing the upper resistor in the feedback-voltage divider with the load, as represented by the LED string in Figure 1. The load current is dependent on the boost converter's on-chip reference voltage and is determined by

$$I_{LOAD} = \frac{V_{REF}}{R_{SET}}. \quad (1)$$

A major problem with this simple implementation is that an open-circuit fault in the LED string removes the pathway for the load current. Without the load current flowing across the feedback resistor, R_{SET}, V_{FB} is pulled to ground. In response, the boost converter increases its operating duty cycle to the maximum duty cycle possible in an effort to maintain the correct voltage on the feedback (FB) pin. Using the idealized transfer function of a boost converter reveals that a high-output voltage (V_{OUT}) can be produced when the converter approaches its maximum duty cycle. Consider a boost converter with a typical maximum duty

Figure 1. High-voltage boost converter configured as an LED driver without open-circuit protection



cycle of 90% (a common value) and a 5-V input:

$$V_{OUT} = \frac{1}{1-D} \times V_{IN} = \frac{1}{1-0.9} \times 5 = 50\ V \quad (2)$$

The high voltage at the converter's output creates the potential for multiple failures. This voltage may exceed the rating of internal or external switching devices or passive components. It may also represent a potential hazard to the user and could damage a load upon connection if the circuit is being operated without one.

Protection circuit

An alternate pathway for the load current must exist in the event of an open-circuit condition. While placing a resistor in parallel with the LED string provides a pathway, it is not ideal because it causes a significant efficiency loss. An alternative configuration (Figure 2) consists of a Zener diode and a resistor and offers suitable system protection with negligible losses in efficiency.

When the load-current pathway is removed, the output voltage increases until the Zener diode, ZD1, turns on and current flows through R_{PRO} and R_{SET} to ground. The output current is determined by the series combination of R_{PRO} and R_{SET} because V_{FB} is driven to equal the internal bandgap reference, V_{REF}. Therefore, the output protection current defaults to

$$I_{PRO} = \frac{V_{REF}}{R_{SET} + R_{PRO}}. \quad (3)$$

A voltage is chosen for the Zener diode such that no current flows through it during normal circuit operation. To ensure that the diode is completely off during normal operation, the voltage chosen should be at least 2 V higher than the maximum load voltage but still less than the maximum output voltage specified for the boost converter. This also decreases the chance that the circuit designer will have to increase the voltage rating of the output capacitors, C2 and C3, and the catch diode, SD1. The output voltage is clamped to the sum of the Zener diode's voltage and the reference voltage:

$$V_{OUT} = V_{ZD1} + V_{REF} \quad (4)$$

R_{PRO} is selected by balancing the error induced to the LED current and the power dissipated during circuit protection. In practice, the value selected for R_{PRO} should be as large as possible in order to minimize power dissipation in the Zener diode:

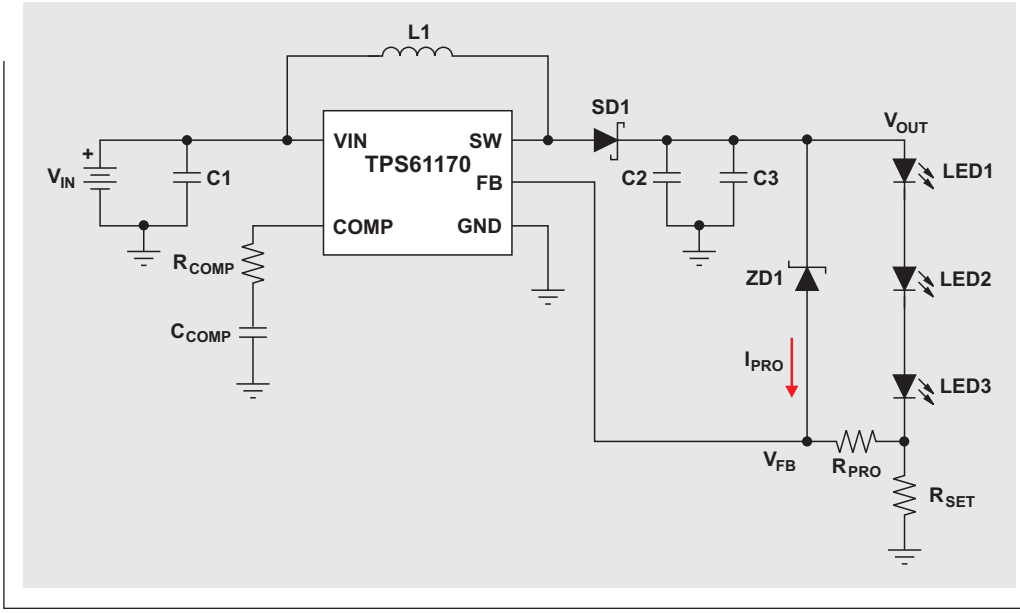
$$P_{ZD1} = I_{PRO} \times V_{ZD1} \quad (5)$$

The error introduced into the circuit is due to the leakage current through the Zener diode, I_{ZL}, as well as the bias current, I_{FB}, of the error amplifier internal to the boost converter. Equation 6 is a revised transfer function that includes these errors:

$$I_{LOAD} = \frac{V_{REF} - I_{ZL}(R_{PRO} + R_{SET}) - I_{FB}(R_{PRO} + R_{SET})}{R_{SET}} \quad (6)$$

Because these two currents are normally less than 1 µA, the error introduced is very small and can be ignored in most implementations.

Figure 2. LED driver circuit with open-circuit protection

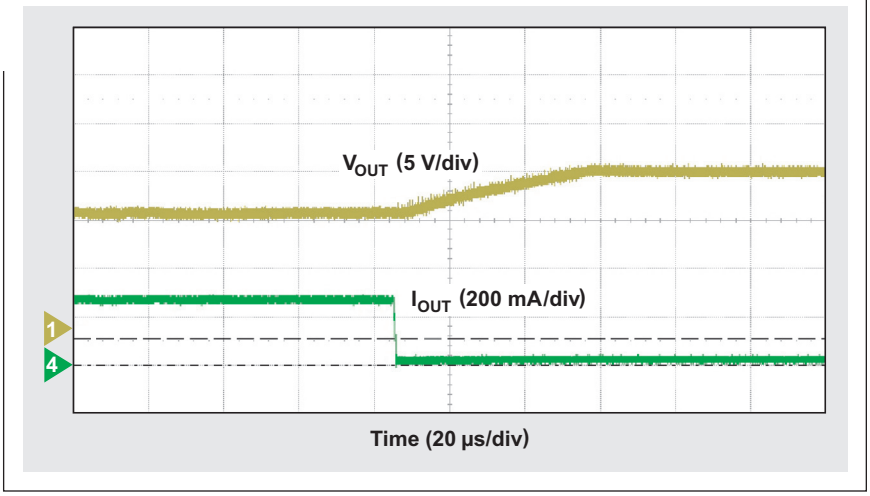


Demonstration

As an application example, the Texas Instruments TPS61170 boost converter IC was configured as a constant-current LED driver. This is an ideal boost converter for driving a string of high-brightness LEDs in applications such as backlighting or flashlights. The 3- to 18-V input range allows a wide range of power sources, such as 2S-to-4S Li-Ion or 3S-to-12S alkaline battery packs, USB, or 12-V rail power.

The boost converter was configured to drive three high-brightness white LEDs with a current of 260 mA. With a typical reference voltage of 1.229 V, R_{SET} was calculated by using the simplified version of the load current in Equation 7:

Figure 3. Oscilloscope screen shot of protection-circuit activation



$$R_{SET} = \frac{V_{REF}}{I_{LOAD}} = \frac{1.229\ V}{260\ mA} = 4.73\ \Omega \quad (7)$$

A value of 1 mA was chosen as a reasonable protection current (I_{PRO}) to calculate the value of R_{PRO}:

$$R_{PRO} = \frac{V_{REF}}{I_{PRO}} - R_{SET} = \frac{1.229\ V}{1\ mA} - 4.7\ \Omega = 1224.3\ \Omega \rightarrow 1.2\ k\Omega \quad (8)$$

A 15-V Zener diode was chosen for ZD1 in order to exhibit minimal leakage at the expected load voltage of approximately 10 V, while also clamping the output to a value far below the maximum allowable output voltage of the boost converter, 40 V. The output voltage was clamped to the Zener diode's voltage (V_{ZD1}), which was summed with the converter's reference voltage:

$$V_{OUT} = V_{ZD1} + V_{REF} = 15\ V + 1.229\ V = 16.229\ V \quad (9)$$

With the load current and protection resistors selected, the deviation from the expected load current was calculated (see Equation 10 below). The datasheet value of 200 nA was used for the feedback bias current (I_{FB}), and a value of 1 µA was used for the expected leakage current through the Zener diode, with a V_{OUT} of approximately 10 V.

Recall that the intended load current for the circuit was 260 mA. As can be seen, once the theoretical values for components are replaced by available values in Equation 10, they contribute far more error than does the protection circuit itself.

To test the protection circuit's operation, the LED string was replaced with a resistor decade box set to 38 Ω to mimic the voltage across the LED string at the designed load current. An open-circuit fault was simulated by rapidly changing the load resistance from 38 Ω to 1038 Ω. As illustrated in Figure 3, the change in the output current (green trace) signaled the sudden change in load impedance. To compensate, the output voltage of the TPS61170 (yellow trace) rose to re-establish the designed load current. However, rather than continuing this trend until reaching its maximum duty cycle, the output voltage stabilized to the clamp voltage of approximately 16 V.

Conclusion

A simple method to provide open-circuit protection to a boost converter configured as a constant-current LED driver was presented. Consisting of a Zener diode and an additional resistor, this circuit limits the output voltage to a safe level while simultaneously reducing the output current when an open-circuit fault occurs at the load. Furthermore, this approach contributes negligible error to the load-current calculations and negligible loss of efficiency during normal circuit operation. The functionality of the protection circuit was demonstrated by configuring a boost converter as an LED driver and adding a 15-V Zener diode and a 1.2-kΩ resistor for output protection. The demonstration circuit exhibited the expected output behavior in a simulated load fault condition.

Related Web sites

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$$I_{LOAD} = \frac{1.229\ V - 1\ \mu A(1.2\ k\Omega + 4.7\ \Omega) - 200\ nA(1.2\ k\Omega + 4.7\ \Omega)}{4.7\ \Omega} = 261\ mA \quad (10)$$

How to design an inexpensive HART transmitter

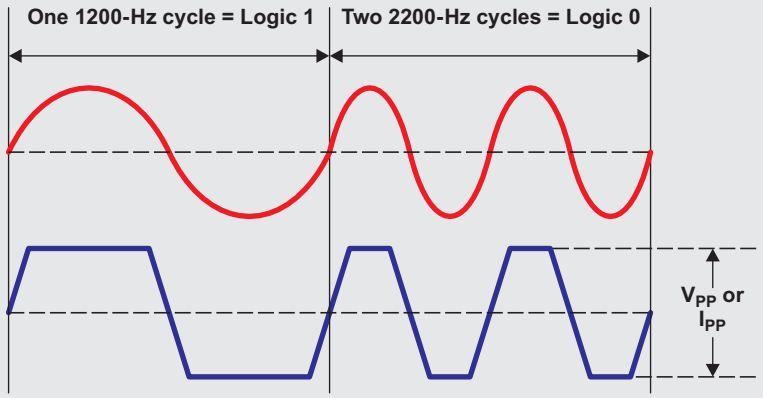
By Thomas Kugelstadt
Applications Manager

Process measurement and control devices can communicate via the conventional 4- to 20-mA current loop by utilizing the highway addressable remote transducer (HART) protocol. This protocol uses frequency-shift keying (FSK) with the frequencies of 1200 Hz and 2200 Hz. Here one 1200-Hz cycle represents a logic 1, while two 2200-Hz cycles represent a logic 0. Because the average value of the FSK waveform is always zero, the analog 4- to 20-mA signal is not affected.

Ideally, the FSK signal consists of sine waves of the two frequencies superimposed onto the DC measurement signal. However, generating phase-continuous FSK sine waves is a rather complex matter. Therefore, in order to simplify the generation of HART signal waveforms, the physical layer of the HART specification defines parametric limits into which the amplitude, shape, and slew rate of a more generalized waveform must fall. In this case, a trapezoidal waveform, with the limiting values detailed in Figure 1, suits this application well.

Figure 1. Minimum and maximum values of trapezoidal HART current waveform

PARAMETER	MINIMUM	MAXIMUM
V_{PP}	0.4 V	0.6 V
I_{PP}	0.8 mA	1.2 mA
Slew Rate at 1200 Hz	1 V/ms 2 mA/ms	4 V/ms 8 mA/ms
Slew Rate at 2200 Hz	2 V/ms 4 mA/ms	



The HART transmitter in Figure 2 provides a simple and inexpensive solution that generates a trapezoidal HART waveform, superimposes it onto a variable DC level, and subsequently converts the resulting output voltage into the loop current.

The HART FSK signal, commonly generated by a local microcontroller unit (MCU), is applied to the input of a first NAND gate, G1. A second output of the MCU's general-purpose I/O port serves as an active-high ENABLE signal. G1 controls two further NAND gates, G2 and G3, whose outputs connect together via high-impedance voltage dividers, R_1 and R_2.

A second voltage divider, consisting of R_4 and R_5, splits the 5-V supply into a reference voltage of $V_{REF} = V_{CC}/2$, or 2.5 V. As long as ENABLE is low, G2's output is low and G3's output is high. Due to high-impedance loading, the NAND outputs provide rail-to-rail capability; and, with $R_1 = R_2$, the input voltage at A1's non-inverting input, V_{IN}, is also 2.5 V.

When ENABLE is taken high, the outputs of G2 and G3 toggle in phase with each other, thus creating a small square wave at V_{IN} that swings symmetrically about V_{REF}. The peak-to-peak amplitude of V_{IN} is given by

$$V_{IN(PP)} = V_S \times \frac{R_3}{R_3 + R_1 \| R_2},$$

where V_S is the positive 5-V supply, and $R_1 \| R_2$ is the parallel combination of R_1 and R_2.

Inserting the resistor values from Figure 2 into the preceding equation yields an input-voltage swing of $V_{IN(PP)}$ = 200 mV, making V_{IN} swing between 2.4 and 2.6 V. When V_{IN} rises to 2.6 V, A1's output goes immediately into positive saturation and charges C_3 via R_6 and R_7. The actual HART voltage on C_3 (V_{HART}) rises linearly until it reaches 2.6 V. At this point, amplifier A1 rapidly exits saturation and acts as a voltage follower, thus holding V_{HART} at 2.6 V. When V_{IN} decreases to 2.4 V, A1's output goes into negative saturation and discharges C_3 via R_6 and R_7. V_{HART} then ramps down linearly until it reaches 2.4 V, at which point A1 comes out of saturation and again acts as a voltage follower, holding V_{HART} at 2.4 V.

The resulting trapezoidal waveform is equal in amplitude to V_{IN} and swings symmetrically about V_{REF}. Its slew rate is determined by

$$\frac{dV}{dt} = \frac{I}{C_3} = \frac{(V_{SAT} - V_{HART})/(R_6 + R_7)}{C_3},$$

where V_{SAT} is the positive or negative output-saturation voltage of A1.

Because the AC content of V_{HART} is small compared to V_{SAT}, V_{HART} can be approximated by its quiescent level, V_{REF}. Also, A1's rail-to-rail-output capability in combination with the high-impedance loading through R_6 yields output-saturation levels of 5 V and 0 V. Given that R_7 is much smaller than R_6, the preceding expression simplifies to

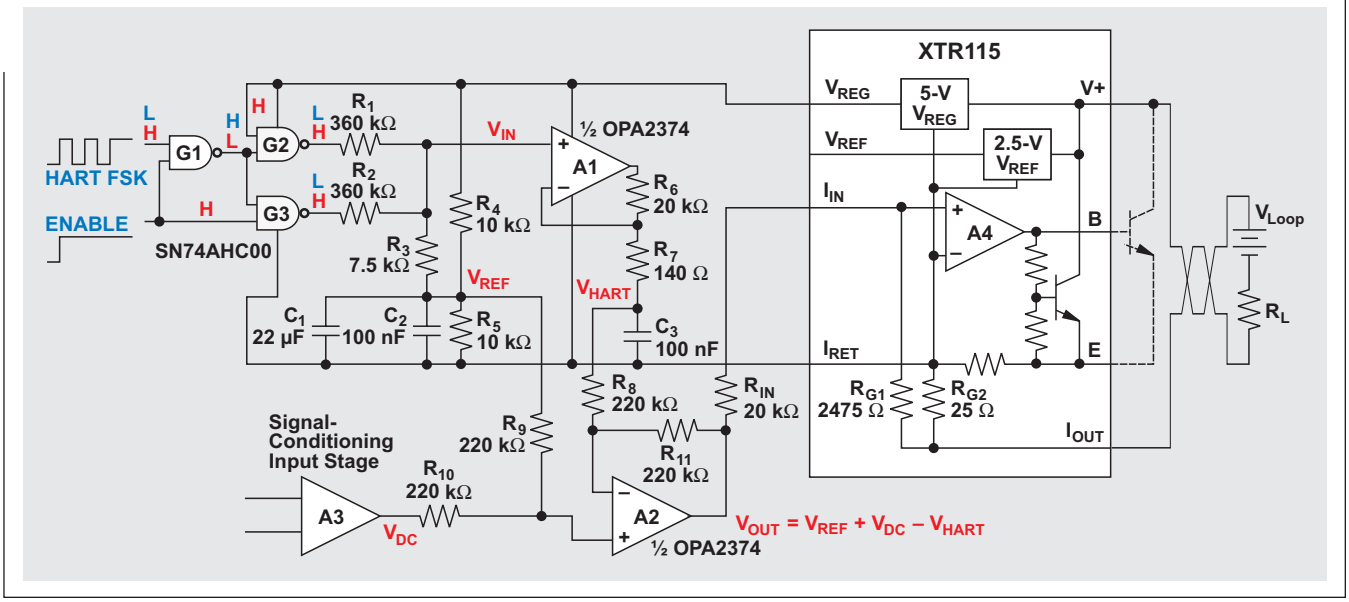
$$\frac{dV}{dt} = \frac{\pm V_{REF}}{R_6 \times C_3}.$$

If the component values for R_6 and C_3 from Figure 2 are inserted, the trapezoid's slew rate results in ±1.25 V/ms.

Scaling the peak-to-peak amplitude of V_{HART} (200 mV) to a HART peak-to-peak current signal of 1 mA makes the voltage slew rate of 1.25-V/ms equivalent to a current slew rate of 6.25 mA/ms in the HART current signal, which perfectly fits within the given limits of Figure 1.

R_7 is required to isolate A1's output from the large capacitive load, C_3, in order to maintain closed-loop stability. The required value depends on A1's unity-gain bandwidth, f_T,

Figure 2. Low-cost HART transmitter



and the values of R_6 and C_3. A good approximation for R_7 is accomplished with

$$R_7 \approx \frac{1+\sqrt{1+8\pi \times f_T \times R_6 \times C_3}}{2\pi \times f_T \times C_3}.$$

A1 must have a reasonably wide frequency response and be able to slew significantly faster than the HART trapezoid. The OPA2374, a low-cost dual operational amplifier from Texas Instruments (TI), provides a sufficiently fast slew rate of 5 V/µs and a unity-gain bandwidth of f_T = 6.5 MHz. In addition, the amplifier outputs have rail-to-rail drive capability with a typical quiescent current of 585 µA per amplifier.

The second amplifier, A2, superimposes the HART signal onto a variable DC voltage, V_{DC}. The voltage at A2's output, V_{OUT}, becomes

$$V_{OUT} = \left(V_{REF} \times \frac{R_{10}}{R_9 + R_{10}} + V_{DC} \times \frac{R_9}{R_9 + R_{10}} \right) \times \left(1 + \frac{R_{11}}{R_8} \right) - V_{HART} \times \frac{R_{11}}{R_8}.$$

Making R_8 to R_{11} equal in value simplifies this equation to

$$V_{OUT} = V_{REF} + V_{DC} - V_{HART}.$$

Because V_{HART} consists of a 200-mV trapezoid swinging symmetrically about V_{REF}, the output of A2 contains only the small HART waveform riding on the variable DC level. Feeding V_{OUT} into TI's XTR115 voltage-to-current converter makes each 200 mV of V_{DC} equivalent to 1 mA of current. Thus, varying V_{DC} from 0.8 V to 4.0 V is equivalent to a 4- to 20-mA current range.

Resistors R_8 to R_{11} should be large enough to minimize the loading effects on C_3's charging current but not so large as to introduce errors through A2's input-offset current. Well-matched resistor values remove V_{REF} entirely from V_{OUT} so that $V_{OUT} = V_{DC} \pm 100$ mV. Therefore a mismatch in R_4 and R_5 or variations in the voltage supply have little effect on V_{OUT}'s DC content.

The XTR115 is a two-wire, precision, current-output converter that transmits analog 4- to 20-mA signals over an industry-standard current loop. The device provides accurate current scaling as well as functions for limiting output current. Its on-chip 5-V voltage regulator is used to power the external circuitry. To ensure control of the output current, I_{OUT}, the current-return pin, I_{RET}, serves as a local ground and senses any current used in the external circuitry. Its input stage has a current gain of 100, which is set by the two laser-trimmed gain resistors, R_{G1} and R_{G2}:

$$\text{Gain} = 1 + \frac{R_{G1}}{R_{G2}}$$

Therefore, an input current, I_{IN}, produces an output current, I_{OUT}, equal to $I_{IN} \times 100$. With the voltage potential at I_{IN} being 0 (referenced to I_{RET}), the resistor value required to convert an input voltage into a defined output current is calculated with

$$R_{IN} = \frac{V_{IN}}{I_{IN}} = \frac{V_{IN}}{I_{OUT}} \times \text{Gain}.$$

Converting the 200-mV_{PP} HART voltage into a 1-mA current thus requires an input resistance of

$$R_{IN} = \frac{200\ \text{mV}}{1\ \text{mA}} \times 100 = 20\ \text{k}\Omega.$$

In addition, R_{IN} defines the input-voltage range for a 4- to 20-mA current range with

$$V_{DC\_min} = \frac{R_{IN} \times I_{OUT\_min}}{\text{Gain}} = \frac{20\ \text{k}\Omega \times 4\ \text{mA}}{100} = 0.8\ \text{V}$$

and

$$V_{DC\_max} = \frac{R_{IN} \times I_{OUT\_max}}{\text{Gain}} = \frac{20\ \text{k}\Omega \times 20\ \text{mA}}{100} = 4\ \text{V}.$$

Conclusion

Simple operational-amplifier circuits can be used to design a low-cost HART transmitter for the conventional 4- to 20-mA current loop.

Figure 3 shows the signal voltages at various test points during a HART transmission for a DC input of 2 V. Resistor matching in the difference amplifier, A2, removes the V_{REF} component in the output signal. Thus, deviations in the reference voltage have no impact on V_{OUT}. The output signal therefore swings symmetrically around the 2-V DC input.

References

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Related Web sites

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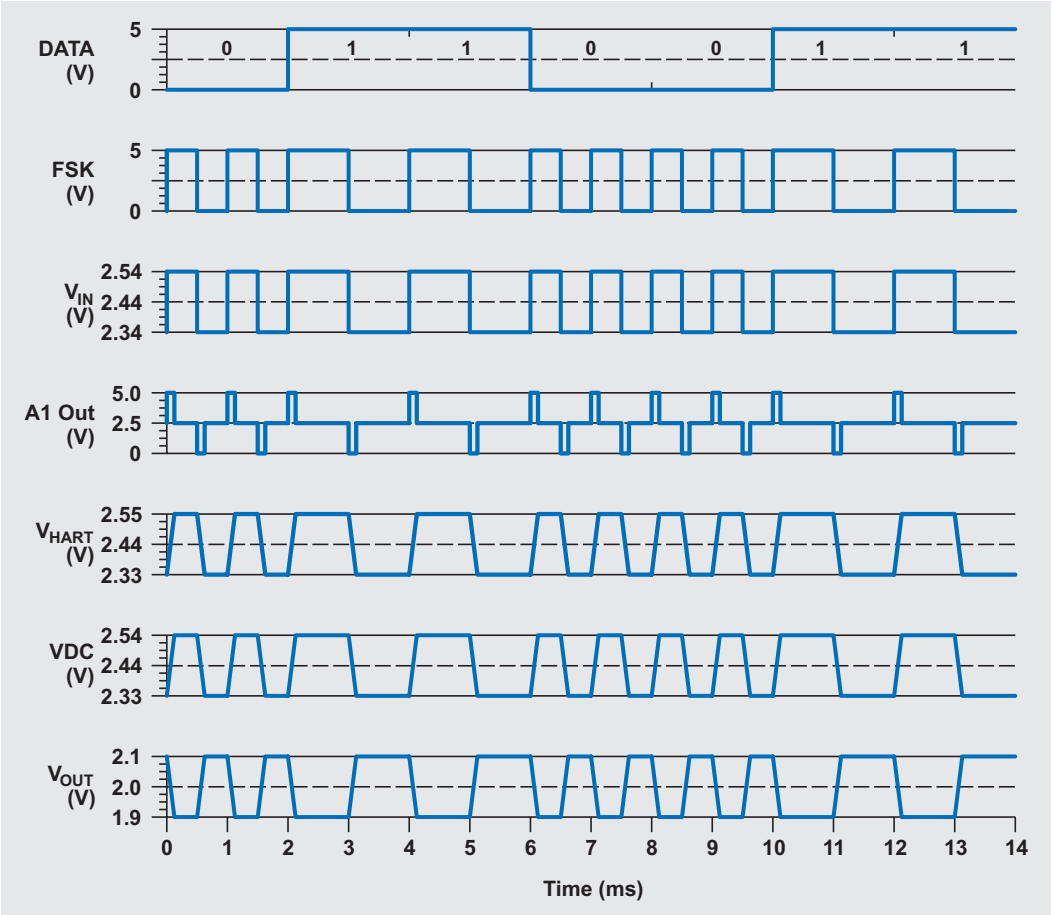
www.ti.com/product/*partnumber*

Replace *partnumber* with OPA2374, SN74AHC00, or XTR115

Figure 3. Signal voltages of the HART transmitter's signal path



Design considerations for system-level ESD circuit protection

By Roger Liang
Systems Engineer

Introduction

As technology has evolved, mobile electronic devices have also evolved to become an integral part of people's lives and cultures. The advent of haptics for tablets and smartphones has encouraged increasing interaction with these devices. This creates the perfect environment for electrostatic discharge (ESD) hazards, or the discharge of static electricity from a body surface to a device. In the case of consumer electronics, for example, ESD can occur between a user's finger and a tablet's USB or HDMI connector and cause irreversible damage to the tablet, such as spiked standby current or permanent system failure.

This article explains the difference between system-level and device-level ESD phenomena and offers system-level design techniques that are targeted to protect against everyday ESD events.

System-level versus device-level ESD protection

ESD damage to ICs can occur at any time, from assembly to board-level soldering to end-user interactions. The incidence of ESD-related damage dates back to the dawn of semiconductors, but it didn't become a prevalent problem until the 1970s with the introduction of the microchip and thin-gate-oxide FETs for highly integrated ICs. All ICs have built-in device-level ESD structures that protect the IC against ESD events during the manufacturing phase. These events are simulated by three different device-level models: the human-body model (HBM), the machine model (MM), and the charged-device model (CDM). The HBM is intended to emulate ESD events caused by human handling, the MM to emulate ESD events caused by automated handling, and the CDM to emulate ESD events caused by product charging/discharging. These models are used for testing in the manufacturing environment, where assembly, final testing, and board-level soldering are performed in controlled ESD environments that limit the level of ESD stress to which the device is exposed. In the manufacturing environment, ICs are usually specified to survive ESD strikes only to a 2-kV HBM, while lower-geometry devices have recently been specified to as low as 500 V.

While device-level models are usually sufficient for the controlled ESD environment of the factory floor, they are completely inad equate for system-level testing. The levels of ESD strikes from both voltages and currents can be much greater in the end-user environment. For this reason, the industry uses a different method for system-level ESD testing, defined by the IEC 61000-4-2 standard. Device-level HBM, MM, and CDM tests are intended to ensure only that ICs survive the manufacturing process; system-level tests specified by IEC 61000-4-2 are intended to simulate end-user ESD events in the real world.

There are two types of system-level tests specified by the IEC: contact discharge and air-gap discharge. In the contact-discharge method, the test-simulator electrode is held in contact with the device under test (DUT). In air-gap discharge, the charged electrode of the simulator approaches the DUT, and a spark to the DUT actuates the discharge.

The range of test levels specified in the IEC 61000-4-2 standard for each method is given in Table 1. It is important to note that the severity of each test level is not equivalent between the two methods. Stress levels are usually incrementally tested above level 4 (the highest official level for each method) until the point of failure.

Table 1. Test levels for contact-discharge and air-gap-discharge methods

CONTACT-DISCHARGE LEVEL	TEST VOLTAGE (± kV)	AIR-GAP-DISCHARGE LEVEL	TEST VOLTAGE (± kV)
1	2	1	2
2	4	2	4
3	6	3	8
4	8	4	15

Table 2. Comparison of device-level models and IEC system-level model

	HUMAN-BODY MODEL (HBM)	MACHINE MODEL (MM)	CHARGED-DEVICE MODEL (CDM)	IEC 61000-4-2 MODEL
Definition	Human body discharging accumulated static	Robotic arm discharging accumulated static	Charged device being grounded	Real-world ESD events
Test Levels (V)	500 to 2000	100 to 200	250 to 2000	2000 to 15000
Pulse Width (ns)	~150	~80	~1	~150
Peak Current at Applied 2 kV (A_{PK})	1.33	—	~5	7.5
Rise Time	25 ns	—	< 400 ps	< 1 ns
Number of Voltage Strikes	2	2	2	20

Device-level models and system-level models have some distinct differences, as highlighted in Table 2. The last three parameters in Table 2—current, rise time, and number of voltage strikes—are of particular concern:

- The difference in current is critical to whether the ESD-sensitive device survives an ESD strike. Because high current levels can cause junction damage and gate-oxide damage, it is possible that a chip protected by an 8-kV HBM (with a peak current of 5.33 A) can be destroyed by a strike to a 2-kV IEC model (with a peak current of 7.5 A). Thus, it is extremely important that system designers do not confuse HBM ratings with ratings for the IEC model.
- Another difference lies within the rise time of the voltage strikes. The rise time specified for an HBM is 25 ns. The pulse of the IEC model has a rise time of less than 1 ns and dissipates most of its energy in the first 30 ns. If an HBM-rated device takes 25 ns to respond, the device can be destroyed before its protection circuits are even activated.
- The number of strikes used during testing is different between the models. The HBM requires only a single positive and single negative strike to be tested, whereas the IEC model requires ten positive strikes and ten negative strikes. It is possible for a device to survive the first strike but fail on subsequent strikes due to damage sustained during the initial strike. Figure 1 shows example ESD waveforms for a CDM, an HBM, and the IEC model. It is apparent that the IEC model's pulse carries much more energy than the pulse of each device-level model.

Figure 1. ESD waveforms for device-level and IEC models

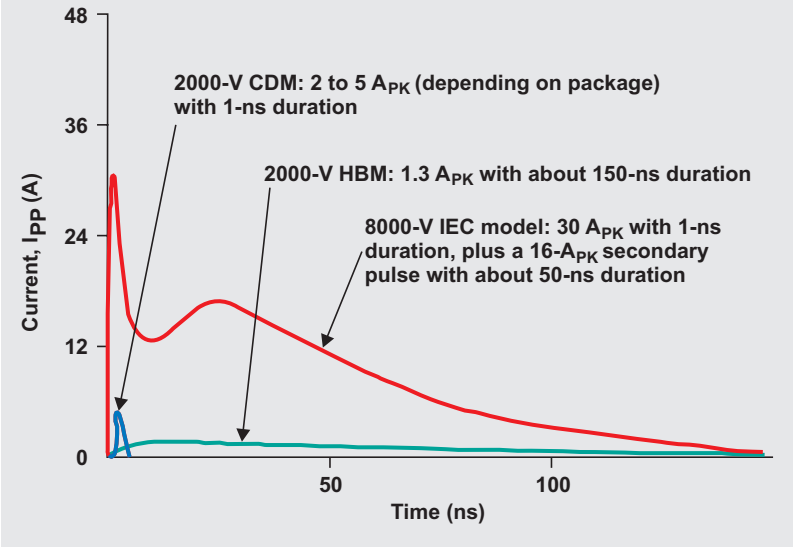
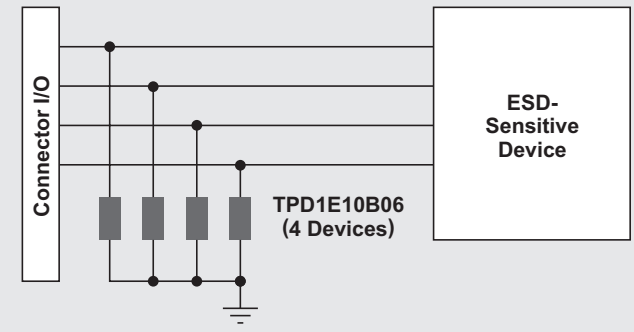


Figure 2. System-level TVS placement



How a TVS protects a system against ESD events

Instead of integrated structures for ESD protection, the model specified by the IEC 61000-4-2 standard usually uses discrete stand-alone transient-voltage-suppressant diodes, or transient-voltage suppressors (TVSs). Compared to ESD-protection structures integrated into a power-management or microcontroller unit, stand-alone TVSs are low in cost and can be placed close to the system's I/O connector, as shown in Figure 2.

There are two types of TVSs: bidirectional and unidirectional (see Figure 3). The Texas Instruments TPD1E10B06 is an example of a bidirectional TVS that can be placed on a general-purpose data line for system-level ESD protection. Both bidirectional and unidirectional TVSs are designed to be an open circuit during normal operating conditions, and a short to ground during an ESD event. In the case of a bidirectional TVS, a voltage signal on the I/O line can swing above and below ground as long as neither D1 nor D2 enters its breakdown region. When an ESD strike (positive or negative) hits the I/O line, one diode becomes forward-biased and the other breaks down, creating a path in which ESD energy is immediately dumped to ground. In the case of a unidirectional TVS, a voltage signal can swing above ground as long as neither D2 nor Z1 enters its breakdown region. When a positive ESD strike hits the I/O line, D1 becomes forward-biased and Z1 enters its breakdown region before D2 does; a path to ground is created through D1 and Z1 in which ESD energy is dissipated. When a negative ESD strike hits, D2 becomes forward-biased and ESD energy is dissipated through D2 to ground. Unidirectional diodes are implemented for high-speed applications because D1 and D2 can be sized smaller with less parasitic capacitance; D1 and D2 in turn "hide" the bigger Zener diode, Z1, which is sized bigger in order to handle more current in its breakdown region.

Figure 3. Bidirectional and unidirectional TVSs

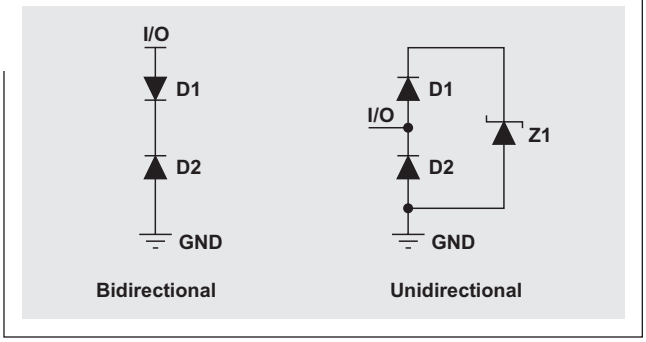
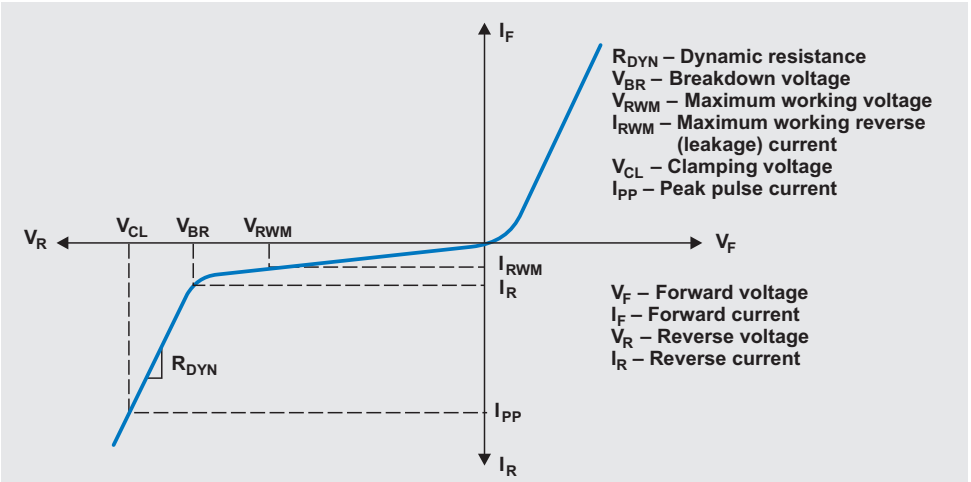


Figure 4. TVS diode's current versus voltage



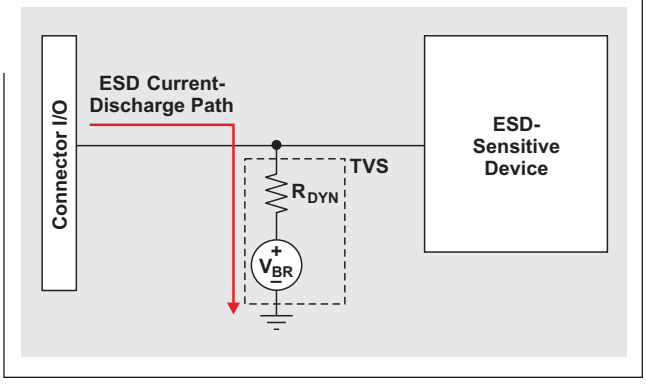
Key device parameters for system-level ESD protection

Figure 4 shows the characteristics of a TVS diode's current versus voltage. Even though a TVS is a simple structure, several important parameters should be considered in the design of system-level ESD protection. These include breakdown voltage, V_{BR}; dynamic resistance, R_{DYN}; clamping voltage, V_{CL}; and capacitance.

Breakdown voltage

The first step in selecting the appropriate TVS is looking at the breakdown voltage (V_{BR}). For example, if the maximum working voltage, V_{RWM}, on the protected I/O line is 5 V, the TVS should not enter into its breakdown region before reaching this maximum. More often than not, a TVS datasheet includes V_{RWM} at a specific leakage current, which makes choosing the right TVS easy. If that is not the case, a TVS can be selected whose $V_{BR(min)}$ is a couple of volts higher than the V_{RWM} of the protected I/O line.

Figure 5. ESD current-discharge path



Dynamic resistance

An ESD is an ultrafast event in the range of nanoseconds. During such a short amount of time, the TVS conduction path to ground is not established instantaneously and there is some resistance in this path. This resistance, known as dynamic resistance (R_{DYN}), is shown in Figure 5.

Ideally, R_{DYN} should be zero so that voltage on the I/O line can be clamped as close to the V_{BR} as possible; however, that is never the case. The industry's current standard value for R_{DYN} is 1 Ω or less. R_{DYN} can be captured by using transmission-line pulse-measurement techniques, where a charged voltage is discharged through the TVS and a corresponding current is measured. After many data points with different charged voltages have been taken, an IV curve like the one in Figure 6 can be drawn, and the slope is R_{DYN}. Figure 6 shows the TPD1E10B06's R_{DYN}, which has a typical value of ~0.3 Ω.

Clamping voltage

Since an ESD is an ultrafast transient event, the voltage on the I/O line is not clamped instantaneously. As shown in Figure 7, thousands of volts are clamped to tens of volts according to the IEC 61000-4-2 standard. As indicated by Equation 1, the lower R_{DYN} is, the better the clamping performance will be:

$$V_{CL} \approx V_{BR} + I_{PP} \times R_{DYN} + I_{Parasitic} \times \frac{dI_{PP}}{dt}, \quad (1)$$

where I_{PP} is the peak pulse current during an ESD event, and $I_{Parasitic}$ is the parasitic inductance of the trace from the connector through the TVS to ground.

Imagine the area under the clamping-voltage waveform as energy. The better the clamping performance is, the less likely it is that an ESD-sensitive device under protection will be damaged during an ESD event. Due to poor clamping voltage, some TVSs survive an IEC model's 8-kV contact discharge, but the "protected" device is destroyed.

Capacitance

During normal operating conditions, the TVS acts as an open circuit and has a parasitic-capacitance shunt to ground. It is important for the designer to take this capacitance into account in the signal chain's bandwidth budget.

Conclusion

As IC process-technology nodes continue to become smaller, they become increasingly more susceptible to ESD damage, both during the manufacturing process and in the end-user environment. Device-level ESD protection is not enough to protect ICs on a system level. Standalone TVSs should be used in a system-level design. When selecting a TVS, the designer should pay careful attention to parameters such as V_{BR}, R_{DYN}, V_{CL}, and capacitance.

Reference

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Document Title	TI Lit. #
1. "System-level ESD/EMI protection guide". . .	SSZB130B

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Figure 6. IV characteristic of TPD1E10B06

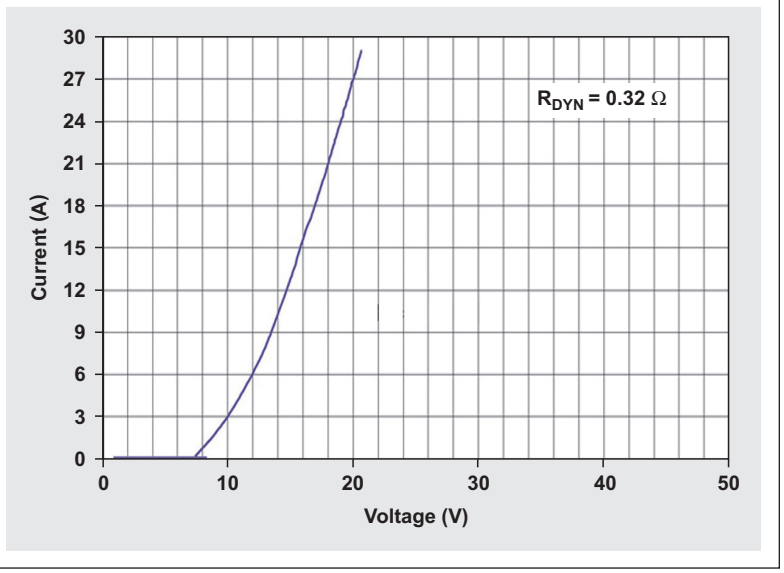
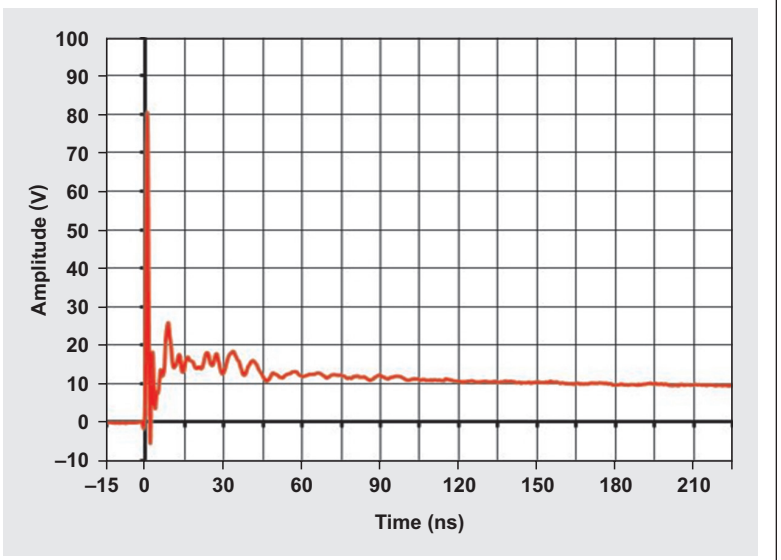


Figure 7. ESD-event clamping with 8-kV contact discharge



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Note: The European Free Call (Toll Free) number is not active in all countries. If you have technical difficulty calling the free call number, please use the international number above.

Fax +(49) (0) 8161 80 2045
Internet www.ti.com/asktexas
Direct Email asktexas@ti.com

Japan

Phone Domestic 0120-92-3326
Fax International +81-3-3344-5317
Domestic 0120-81-0036
Internet/Email International support.ti.com/sc/pic/japan.htm
Domestic www.tij.co.jp/pic

Asia

Phone
International +91-80-41381665
Domestic Toll-Free Number

Note: Toll-free numbers do not support mobile and IP phones.

Australia 1-800-999-084
China 800-820-8682
Hong Kong 800-96-5941
India 1-800-425-7888
Indonesia 001-803-8861-1006
Korea 080-551-2804
Malaysia 1-800-80-3973
New Zealand 0800-446-934
Philippines 1-800-765-7404
Singapore 800-886-1028
Taiwan 0800-006800
Thailand 001-800-886-0010

Fax +8621-23073686
Email tiasia@ti.com or ti-china@ti.com
Internet support.ti.com/sc/pic/asia.htm

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