The IBIS model, Part 3: Using IBIS models to investigate signal-integrity issues

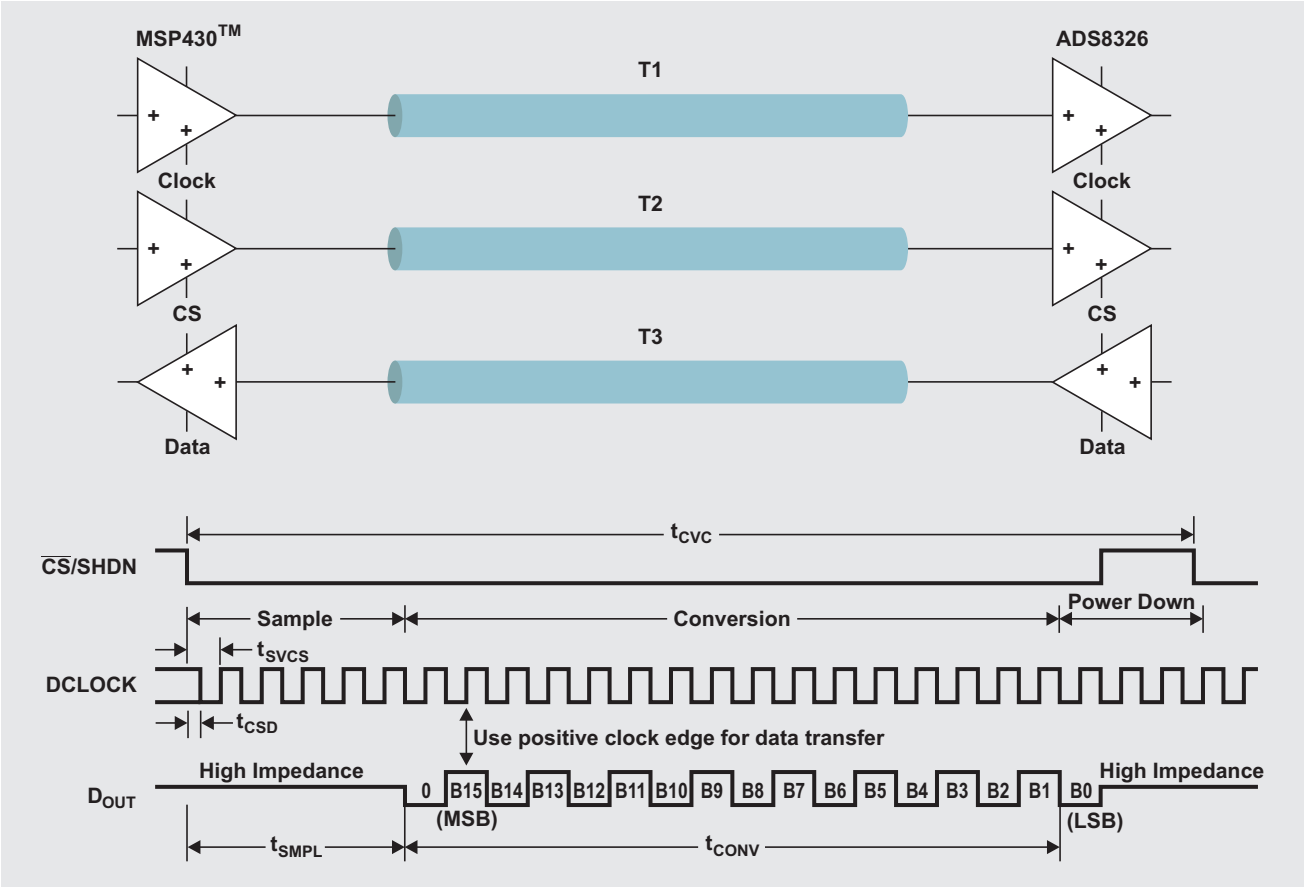
By Bonnie C. Baker
Senior Applications Engineer

This article is the third of a three-part series on using a digital input/output buffer information specification (IBIS) simulation model during the development phase of a printed circuit board (PCB). Part 1 discussed the fundamental elements of IBIS simulation models and how they are generated in the SPICE environment.[1] Part 2 discussed IBIS model validation.[2] The IBIS model brings a simple solution to many of the signal-integrity problems that may be encountered during the design phase. This article, Part 3, shows how to use an IBIS model to extract important variables for signal-integrity calculations and PCB design solutions. Please note that the extracted values are an integral part of the IBIS model.

Signal-integrity problems

When looking at a digital signal at both ends of a transmission line, the designer may be surprised at the result of driving the signal into a PCB trace. Over relatively long distances, electric signals act more like traveling waves than instantaneous, changing signals. A good analogy that describes electric-wave behavior on a circuit board is waves in a pool. A ripple travels smoothly across the pool because one volume of water has the same "impedance" as the next. However, the pool wall presents a very different impedance and reflects the wave in the opposite direction. Electric signals injected into a PCB trace experience the same phenomena, reflecting in a similar manner when impedances are mismatched. Figure 1 shows a PCB setup with mismatched termination impedances. A microcontroller,

Figure 1. PCB setup with mismatched termination impedances



the Texas Instruments (TI) MSP430™, transmits a clock signal to the TI ADS8326 ADC, which sends the conversion data back to the MSP430. Figure 2 shows the reflections created by the impedance mismatches in this setup. These reflections cause signal-integrity problems on the transmission lines. Matching the electrical impedance of the PCB trace at one or both ends can reduce reflections dramatically.

To tackle the issue of matching a system's electrical impedances, the designer needs to understand the impedance characteristics of the integrated circuits (ICs) and the PCB traces that function as a transmission line. Knowing these characteristics allows the designer to model the connecting elements as distributed transmission lines.

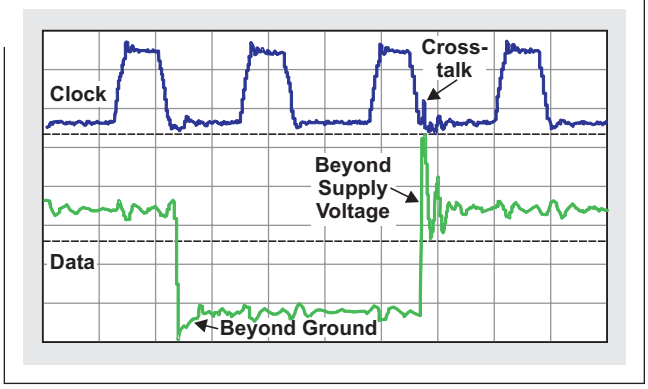
Transmission lines service a variety of circuits, from single-ended and differential-ended to open-drain output devices, etc. This article focuses on a single-ended transmission line where the driver has a totem-pole design. Figure 3 shows the elements to use to design this example transmission line.

The following IC pin specifications are also needed:

- Transmitter's output resistance, Z_T (Ω)
- Transmitter's rise time, t_{Rise}, and fall time, t_{Fall} (seconds)
- Receiver's input resistance, Z_R (Ω)
- Receiver pin's capacitive value, C_{R_Pin} (F)

These specifications are usually not available in the IC manufacturer's product datasheets. As this article will demonstrate, all of these values can be pulled from the IC's IBIS model in the process of designing the PCB and using the model to simulate the PCB's transmission lines.

Figure 2. Induced reflections from mismatched termination impedances in Figure 1

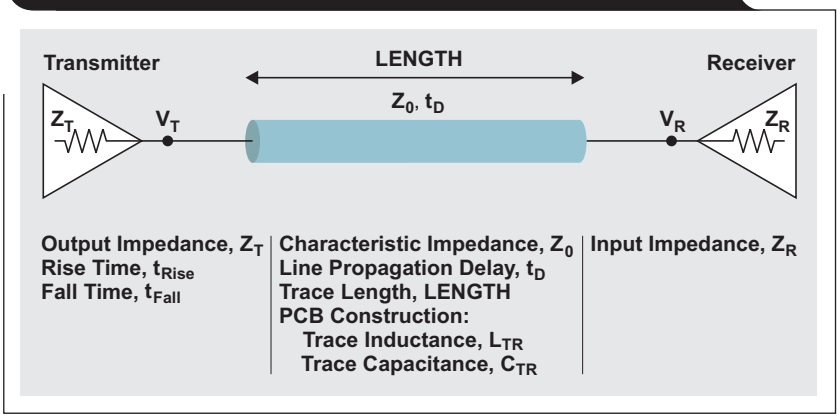


The transmission lines are defined with the following parameters:

- Characteristic impedance, Z_0 (Ω)
- Propagation delay, D (ps/inch)
- Line propagation delay, t_D (ps)
- Trace length, LENGTH (inches)

This list of variables can expand, depending on the PCB design. For instance, a PCB design can have a backplane with multiple transmission/receiver points.[3] All of the transmission-line values depend on the particular PCB. Typically, an FR-4 board's Z_0 ranges from 50 to 75 Ω, and D ranges from 140 to 180 ps/inch. The actual values of Z_0 and D depend on the actual transmission line's material

Figure 3. Example single-ended transmission-line circuit



and physical dimensions.[4] The line propagation delay on a particular board is calculated as

$$t_D = D \times LENGTH. \quad (1)$$

For FR-4 boards, a reasonable propagation delay for a stripline (see Figure 4) is 178 ps/inch, with a characteristic impedance of 50 Ω. This can be verified on the board by measuring the line inductance and capacitance of the trace and inserting those values into the following equations:

$$D = 10^{12} \times \sqrt{C_{TR} \times L_{TR}} \quad (2)$$

or

$$D = 85 \text{ ps/inch} \times \sqrt{e_r}, \quad (3)$$

and

$$Z_0 = \sqrt{\frac{L_{TR}}{C_{TR}}}. \quad (4)$$

C_{TR} is the trace line capacitance in farads/inch; L_{TR} is the trace line inductance in henrys/inch; 85 ps/inch is the dielectric constant for air; and e_r is the material dielectric constant. For instance, if the microstrip-board line capacitance is 2.6 pF/inch, and the line inductance is 6.4 nH/inch, then D = 129 ps/inch and Z_0 = 49.4 Ω.

Lumped versus distributed circuits

Once the transmission lines have been defined, the next step is to determine whether the circuit layout represents a lumped or a distributed system. Generally, a lumped circuit is small, and a distributed circuit requires much more space on the board. A small circuit is one that has an effective length (LENGTH) that is smaller than the fastest electrical feature in the signal. To qualify as a lumped system, the circuit on the PCB must meet the following requirement:

$$LENGTH < \frac{t_{Rise}}{6 \times \sqrt{L_{TR} \times C_{TR}}}, \quad (5)$$

where t_{Rise} is the rise time in seconds.

With a lumped-circuit implementation on the PCB, termination strategies become a non-issue. Fundamentally, it is assumed that the driver signals transmitted into the transmission lines arrive at the receiver instantaneously.

Data organization in an IBIS model

An IBIS model includes data for three, six, or nine corners, depending on the IC's power-supply voltage range. The variables governing these corners are the silicon process,[1] the power-supply voltage, and the junction temperature. The specific process/voltage/temperature (PVT) SPICE corners of a device's models are critical for creating an accurate IBIS model. The silicon process varies from nominal to weak to strong models. The designer defines the voltage settings from the component's power-supply requirements and varies them between nominal, minimum, and maximum values. Finally, the temperature settings at the component's silicon junction are determined from the component's specified temperature range, the nominal power dissipation, and the package's junction-to-ambient thermal resistance, or θ_{JA}.

Figure 4. Basic cross sections of microstrip and stripline boards

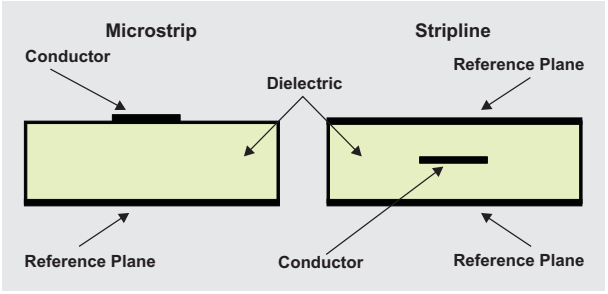


Table 1 shows an example of the three PVT variables and their relationships for a CMOS process with TI's ADS129x family of 24-bit biopotential-measurement ADCs. These variables are used to perform the SPICE simulation six times. The first and fourth simulations use the nominal process models, the nominal power-supply voltage, and the junction at room temperature. The second and fifth simulations use the weak process models, a low power-supply voltage, and a high junction temperature. The third and sixth simulations use the strong process models, a higher power-supply voltage, and a lower junction temperature. The relationships between the PVT values map the optimum corners for a CMOS process.

Table 1. PVT simulation corners for ADS1296 IBIS model

CORNER NUMBER	SILICON PROCESS*	POWER-SUPPLY VOLTAGE (V)	TEMPERATURE (°C)
1	Nominal	1.8	27
2	Weak	1.65	85
3	Strong	2.0	–40
4	Nominal	3.3	27
5	Weak	3.0	85
6	Strong	3.6	–40

*The standard for TI's IBIS models is nominal = typical, weak = minimum, and strong = maximum.

Finding and/or calculating transmitter specifications

The required transmitter specifications for a signal-integrity evaluation are the output impedance (Z_T) and the rise and fall times (t_{Rise} and t_{Fall}, respectively). Figure 5 shows the package listing from the IBIS model file, ads129x.ibs,[5] for TI's ADS1296. The values that are used to produce the impedance are shown under the "[Pin]" keyword and are also within the buffer models (not shown). The rise and fall times are located in the transient portions of the IBIS model's data listing.

Figure 5. IBIS model's package listing for ADS1296, including L_pin and C_pin values

```
ads1296zxg :: PBGA, 64 pin package

[Component]    ads1296zxg
[Manufacturer] TI
|
[Package]    |ZXG (PBGA) - 64 pin
| variable   typ           min           max
R_pkg        0.084959      0.084959      0.084959
L_pkg        1.726943nH    1.173300nH    2.802300nH
C_pkg        0.203317pF    0.155540pF    0.299270pF
|
[Pin]  signal_name  model_name  R_pin         L_pin         C_pin
|
1A      IN8P        TERM        0.080388      1.4891nH      0.16542pF
1B      IN7P        TERM        0.078742      1.4385nH      0.15797pF
1C      IN6P        TERM        0.077541      1.4231nH      0.16358pF
                      ⋮           ⋮             ⋮
5E      GPIO4       DIO         0.106300      2.5339nH      0.28001pF
                      ⋮           ⋮             ⋮
```

Impedances of input and output pins

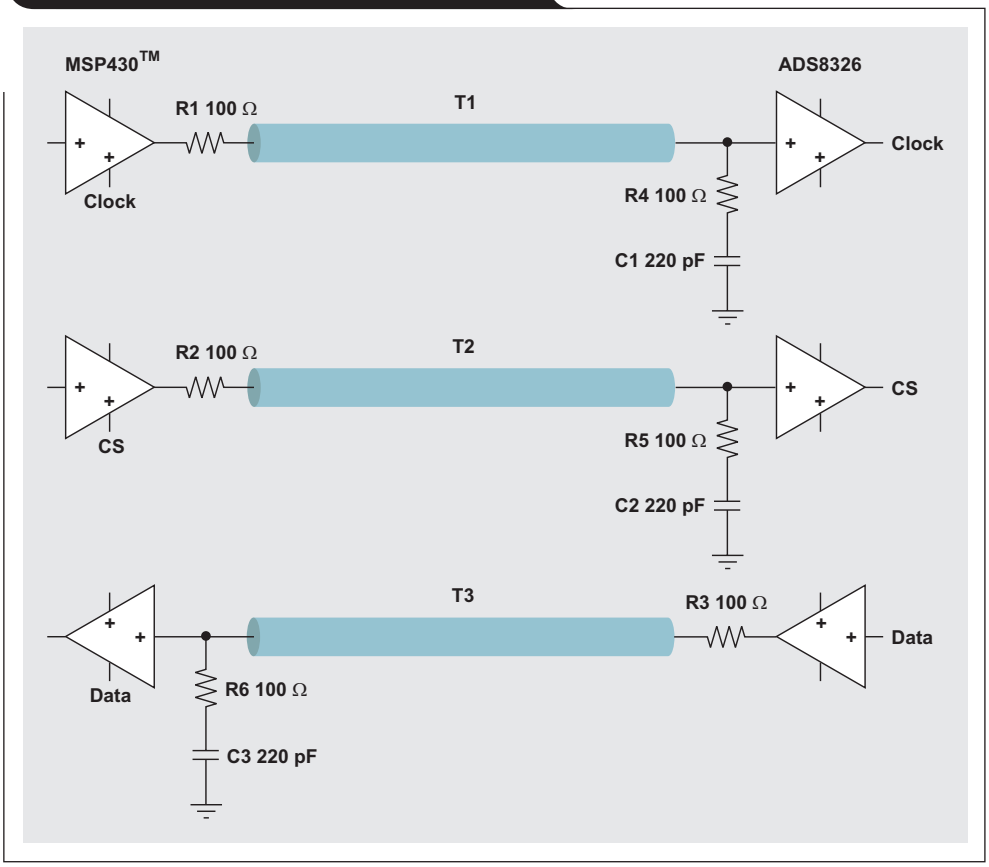
The pin impedance of any signal consists of the package inductance and capacitance added to the model's impedance. In Figure 5, the keywords "[Component]," "[Manufacturer]," and "[Package]" describe a specific package, a 64-pin PBGA (ZXG). The package inductance and capacitance for specific pins can be found under the "[Pin]" keyword. For instance, at pin 5E for the signal GPIO4, the L_pin and C_pin values are given. The L_pin (pin inductance) and C_pin (pin capacitance) values for this signal and package are 1.4891 nH and 0.28001 pF, inclusive.

The second capacitance value of interest is the silicon capacitance, C_comp. The C_comp values can be found under the "[Model]" keyword in the model DIO_33 listing from the ads129x.ibs file (see Figure 6). C_comp in this model is the capacitance of the DIO buffer with 3.3 V applied to the power-supply pin. The "|" symbol indicates a comment; so the active C_comp values in this listing are 3.0727220e-12 F (typical), 2.3187130e-12 F (minimum), and 3.8529520e-12 F (maximum), from which the PCB designer can choose. During the design stage of the PCB transmission lines, the typical value of 3.072722 pF is an appropriate choice.

Figure 6. Model DIO_33 listing of C_comp values from ads129x.ibs file

```
[Model]      DIO_33
Model_type   I/O
|Signals     SCLK, DAISY_IN
|
Vinl = 0.66
Vinh = 2.64
Vmeas = 1.65
Vref = 1.65
Cref = 15pF
Rref = 50
|
|                     typ             min             max
|                     (nom PVT)       (fast PVT)      (slow PVT)
|
C_comp                3.0727220e-12   2.3187130e-12   3.8529520e-12
|C_comp (ON state)    5.2856500e-12   4.3183460e-12   6.0694320e-12
|C_comp (OFF state)   6.2160260e-12   5.1916700e-12   7.4675830e-12
|
|
| Where nom PVT is Nominal Process, 3.3V, 27C
|       Fast PVT is Strong Process, 3.6V, -40C
|       Slow PVT is Weak Process, 3V, 85C
```

Figure 7. Termination-correction strategy



The input and output impedances can be critical to signal transmission. The following equation defines the characteristic impedance of the IBIS model pins:

$$Z_T = Z_R = \sqrt{\frac{L_{pin}}{C\_pin + C\_comp}} \quad (6)$$

Output rise and fall times

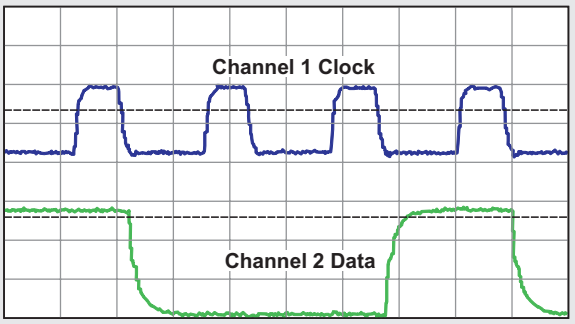
Across the industry, the convention for rise- and fall-time specifications is to use the time needed for the output signal to swing between 10% and 90% of the rail-to-rail signal, which is usually 0 to DV_{DD}. The IBIS Open Forum's definition for rise time is the same and was adopted because of the long tails on CMOS switching waveforms.

Output, I/O, and three-state models within the IBIS model have specifications embedded under the "[Ramp]" keyword for R_load (test load), dV/dt_r (rise time), and dV/dt_f (fall time). The range of the rise- and fall-time data is from 20 to 80% of the voltage-output signal. If the denominator of the typical dV/dt_r values is multiplied by 0.8/0.6, the rise-time value will change from a 20-to-80% swing to a 10-to-90% swing. Please note that the data represents a buffer with the resistive load, R_load. In the ads129x.ibs file, DIO_33 data assumes a 50-Ω load, so the data does not extend to DV_{DD}. The resulting number from this calculation will provide an appropriate value for t_{Rise} for the various transmission-line calculations such as f_{Knee}, f_{3dB}, and rising-edge lengths.

Using IBIS to design transmission lines

This article started out by discussing a PCB with mismatched termination impedances. The IBIS model was then used to understand and find the critical elements for this transmission problem. At this point, it is only fair to show that there is a solution to this problem. Figure 7 shows the termination-correction strategy, and Figure 8 shows the corrected waveforms.

Figure 8. Stable signals from termination correction



To design PCB transmission lines, the first step is to gather information from the product datasheet. The second step is to examine the IBIS model to find the parameters that cannot be gleaned from the datasheet—input/output impedance, rise time, and input/output capacitance. It makes sense to use the IBIS model to find key product specifications and to simulate the final design before going to the hardware stage.

References

For more information related to this article, you can download an Acrobat® Reader® file at www.ti.com/lit/*litnumber* and replace "*litnumber*" with the **TI Lit. #** for the materials listed below.

Document Title	TI Lit. #
1. Bonnie Baker, "The IBIS model: A conduit into signal-integrity analysis, Part 1," *Analog Applications Journal* (4Q 2010)	slyt390
2. Bonnie C. Baker, "The IBIS model, Part 2: Determining the total quality of an IBIS model," *Analog Applications Journal* (1Q 2011)	slyt400
3. Shankar Balasubramaniam, Ramzi Ammar, Ernest Cox, Steve Blozis, and Jose M. Soltero, "Basic design considerations for backplanes," Application Report	szza016
4. Howard W. Johnson and Martin Graham, *High-Speed Digital Design: A Handbook of Black Magic.* Englewood Cliffs, NJ: Prentice Hall, 1993.	—
5. ads129x.ibs IBIS Model [Online]. Available: http://www.ti.com/litv/zip/sbam021b	—
6. "Using IBIS models for timing analysis," Application Report	spra839
7. Roy Leventhal and Lynne Green, *Semiconductor Modeling for Simulating Signal, Power, and Electromagnetic Integrity.* New York: Springer Science+ Business Media, LLC, 2006.	—

Related Web sites

dataconverter.ti.com
www.ti.com/sc/device/ADS1296
www.ti.com/sc/device/ADS8326

TI Worldwide Technical Support

Internet

TI Semiconductor Product Information Center Home Page
support.ti.com

TI E2E™ Community Home Page
e2e.ti.com

Product Information Centers

Americas	Phone	+1(972) 644-5580
Brazil	Phone	0800-891-2616
Mexico	Phone	0800-670-7544
	Fax	+1(972) 927-6377
	Internet/Email	support.ti.com/sc/pic/americas.htm

Europe, Middle East, and Africa

Phone	
European Free Call	00800-ASK-TEXAS (00800 275 83927)
International	+49 (0) 8161 80 2121
Russian Support	+7 (4) 95 98 10 701

Note: The European Free Call (Toll Free) number is not active in all countries. If you have technical difficulty calling the free call number, please use the international number above.

Fax	+(49) (0) 8161 80 2045
Internet	support.ti.com/sc/pic/euro.htm
Direct Email	asktexas@ti.com

Japan

Phone	Domestic	0120-92-3326
Fax	International	+81-3-3344-5317
	Domestic	0120-81-0036
Internet/Email	International	support.ti.com/sc/pic/japan.htm
	Domestic	www.tij.co.jp/pic

Asia

Phone	
International	+91-80-41381665
Domestic	Toll-Free Number

Note: Toll-free numbers do not support mobile and IP phones.

Australia	1-800-999-084
China	800-820-8682
Hong Kong	800-96-5941
India	1-800-425-7888
Indonesia	001-803-8861-1006
Korea	080-551-2804
Malaysia	1-800-80-3973
New Zealand	0800-446-934
Philippines	1-800-765-7404
Singapore	800-886-1028
Taiwan	0800-006800
Thailand	001-800-886-0010
Fax	+8621-23073686
Email	tiasia@ti.com or ti-china@ti.com
Internet	support.ti.com/sc/pic/asia.htm

A122010

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Audio	www.ti.com/audio	Communications and Telecom	www.ti.com/communications
Amplifiers	amplifier.ti.com	Computers and Peripherals	www.ti.com/computers
Data Converters	dataconverter.ti.com	Consumer Electronics	www.ti.com/consumer-apps
DLP® Products	www.dlp.com	Energy and Lighting	www.ti.com/energy
DSP	dsp.ti.com	Industrial	www.ti.com/industrial
Clocks and Timers	www.ti.com/clocks	Medical	www.ti.com/medical
Interface	interface.ti.com	Security	www.ti.com/security
Logic	logic.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Power Mgmt	power.ti.com	Transportation and Automotive	www.ti.com/automotive
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com	Wireless	www.ti.com/wireless-apps
RF/IF and ZigBee® Solutions	www.ti.com/lprf		
	TI E2E Community Home Page		e2e.ti.com

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265