How the voltage reference affects ADC performance, Part 3

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This article is Part 3 of a three-part series that investigates the design and performance of a voltage-reference system for a successive-approximation-register (SAR) analog-to-digital converter (ADC). Part 1 (see Reference 1) examined the ADC characteristics and specifications, with a particular interest in the gain error and signal-to-noise ratio, while assessing how the voltage reference impacts the ADC transfer function and DC accuracy. Part 2 (see Reference 2) examined the voltage-reference characteristics, focusing on how the voltage-reference noise produces the most error at the converter's full-scale range. Part 2 concluded by presenting a design for a voltage-reference circuit that is appropriate for 8- to 14-bit converters. This article, Part 3, tackles the challenge of designing a voltage-reference circuit that is appropriate for converters with 16+ bits. Part 3 examines methods of improving noise filtering and of compensating for losses caused by the improved filters.

Basics of reducing voltage-reference noise

As discussed in Part 2, the two sources of noise in the reference voltage are the internal output amplifier and the bandgap. The voltage-reference circuit from Part 2 that was configured with an 8- to 14-bit ADC can be used as a starting point to continue the discussion. The size of the least significant bit (LSB) of any converter in a 5-V system is equal to 5 V/2^N, where N is the number of converter bits. The 8-bit LSB size in this environment is 19.5 mV, and the 14-bit LSB size is 305 µV. The target value for voltage-reference noise should be less than these LSB values. The bandgap noise of the circuit from Part 2 was reduced by adding an external capacitor to the output to create a low-pass filter. This circuit's output noise can be further reduced by adding another capacitor as a passive low-pass filter. Figure 1 shows an example of such a design, which uses a voltage reference from the Texas Instruments (TI) REF50xx family. In this design, the 1-µF capacitor (C_1) provides a minimal 21-dB noise reduction at the internal bandgap reference. C_2, in combination with the open-loop output resistance (R_O) of the voltage reference's internal amplifier (see Reference 4), further reduces the output noise of the reference at the V_{REF_OUT} pin. In this case, the equivalent series resistance (ESR) of the 10-µF ceramic capacitor (C_2) is equal to 200 mΩ.

Figure 1. Voltage-reference design appropriate for 8- to 14-bit converter

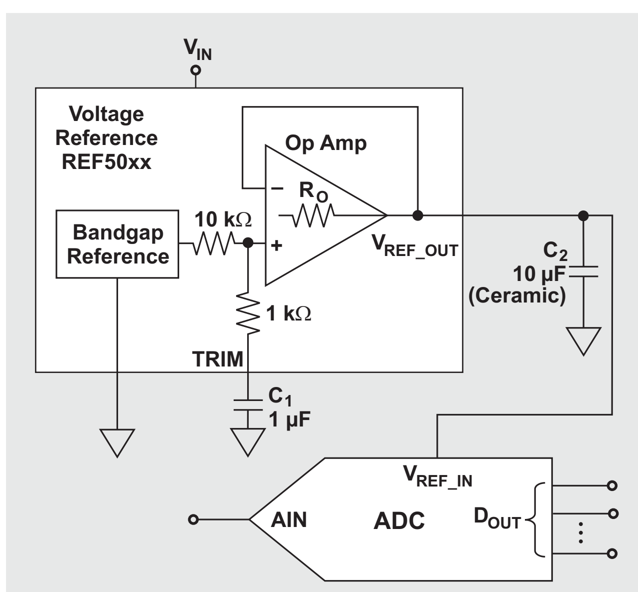


Figure 2 shows a fast-Fourier-transform (FFT) plot of the output signal of the circuit in Figure 1. Note that the output-noise level peaks at around 9 kHz because of the response of the circuit's internal amplifier to the capacitive load (C_2). This peaking is the main contributor to the overall measured noise. This output noise, measured with an analog meter over a frequency range of up to 80 kHz, is approximately 16.5 μV_{RMS}. If the voltage-reference circuit was connected to the input of an ADC, the measured noise across a 65-kHz frequency range would be 138 μV_{PP}. This noise level makes the solution in Figure 1 adequate for 8- to 14-bit converters.

Reducing voltage-reference noise for an ADC with 16+ bits

Since the voltage-reference circuit in Figure 1 would introduce too much noise into a converter with 16+ bits, another low-pass filter can be added to further reduce the reference's output noise. This filter consists of a 10-kΩ resistor (R_1) and an additional capacitor (C_3) as shown in Figure 3. The corner frequency of this added RC filter, 1.59 Hz, will reduce broadband noise as well as noise at extremely low frequencies.

Figure 2. FFT plot of V_{REF_OUT} signal of circuit in Figure 1

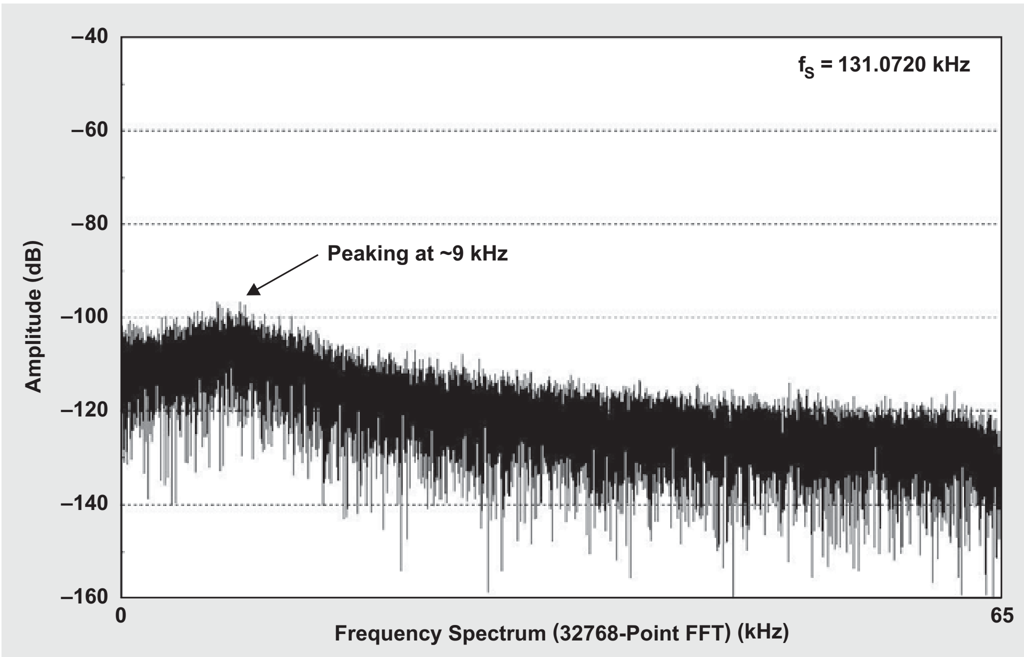


Figure 3. Voltage-reference circuit with R_1 and C_3 added as filters

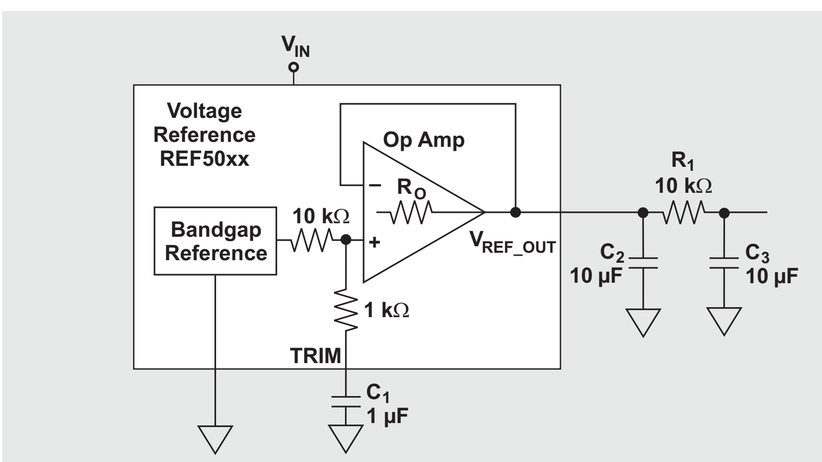


Figure 4. FFT plot of V_{REF_OUT} signal of circuit with RC filter added

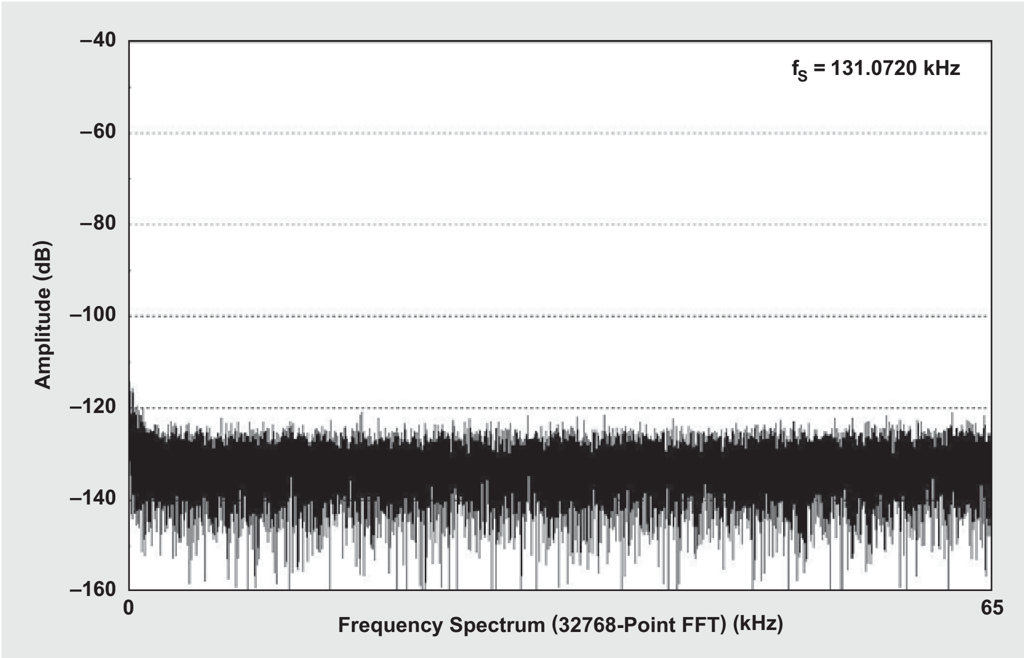


Figure 4 shows that the addition of R_1 and C_3 has a significant effect on the output noise for this system. The 9-kHz noise peak is gone. With this signal response, the output noise of the reference circuit in Figure 3 becomes 2.2 μV_{RMS} or 15 μV_{PP}, a reduction of nearly 90%. This improvement brings the noise level so well under control that the voltage-reference circuit is now appropriate for ADC resolutions of up to 20 bits.

This is encouraging; however, pulling current through R_1 from the ADC reference pin will corrupt the conversion by introducing a voltage drop equivalent to the average charge level from the reference pin of the ADC. Consequently, the output of this new circuit will not be able to adequately drive the ADC's voltage-reference input. To accomplish this, a buffer will need to be added to the low-pass filters.

Adding a buffer to the voltage-reference circuit

Figure 5 shows an example of the fluctuations in ADC reference drive current that can occur during a conversion. The signal was captured with a low-capacitance probe to show the voltage drop across the 10-kΩ resistor (R_1) between the input of the ADC voltage-reference pin and V_{REF_OUT}. The top trace in Figure 5 shows the trigger signal that the converter receives to initiate a new conversion. The ADC's voltage-reference circuit demands different amounts of current (bottom trace) for the initiation of the conversion and for each code decision. Therefore, the voltage-reference analog circuitry connected to the ADC must be able to accommodate these high-frequency fluctuations efficiently while maintaining a strong voltage reference for the converter.

Figure 5. Drive current required by ADC's reference input

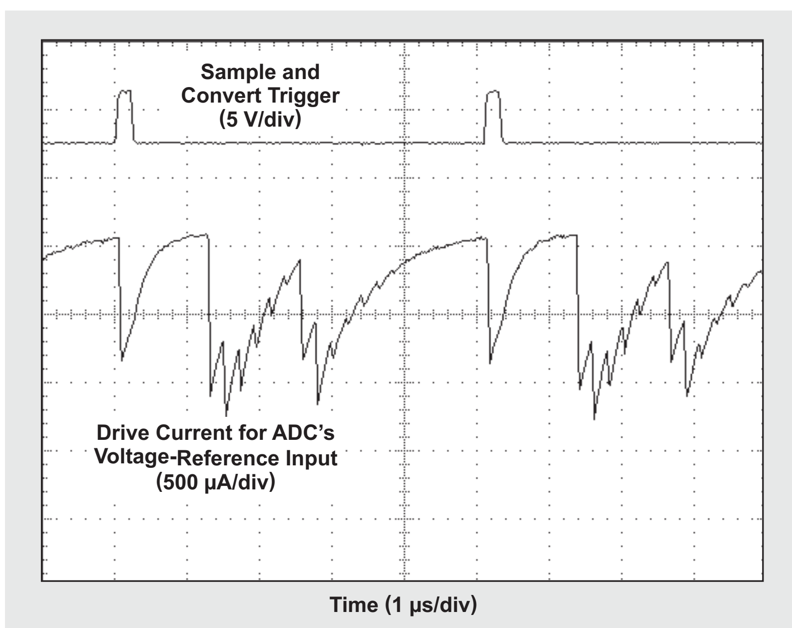


Figure 6. Voltage-reference circuit with added buffer and output filter

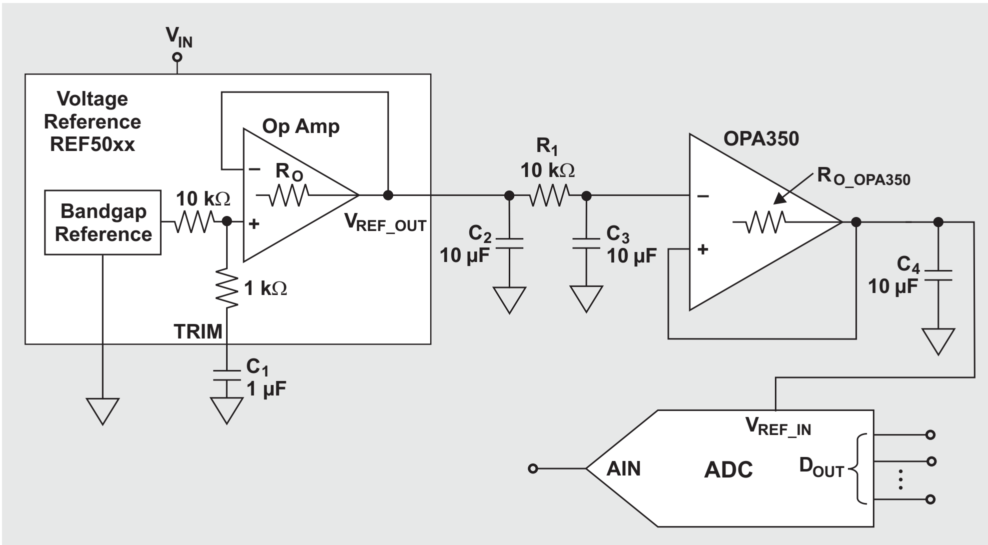


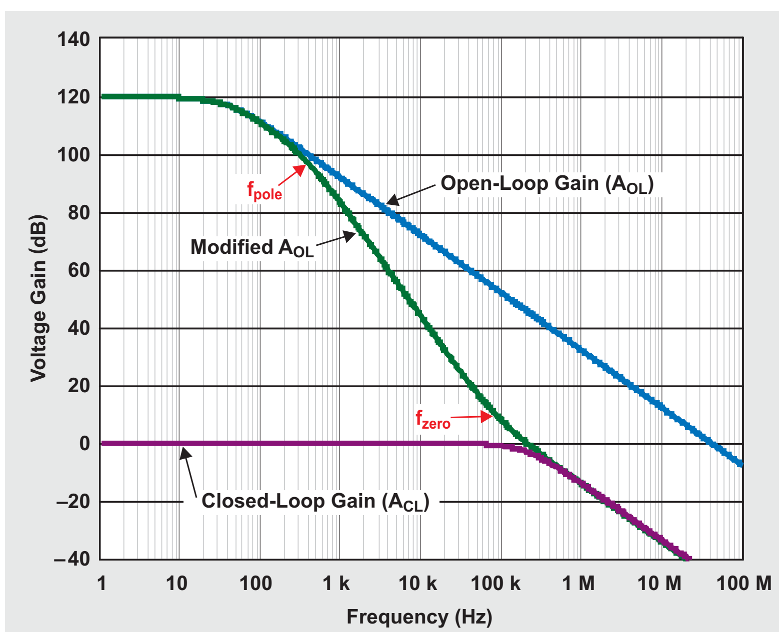
Figure 6 shows a voltage-reference circuit that will adequately drive a high-resolution ADC. In this circuit, the TI OPA350 is placed as a buffer after the low-pass filter that was constructed with R_1 and C_3 for the circuit in Figure 3. The OPA350 drives a 10-µF filter capacitor (C_4) and the voltage-reference input pin of the ADC. The noise measured at the output of the OPA350 in Figure 6 is 4.5 μV_{RMS} or 42 μV_{PP}. The input bias current of the OPA350 is 10 pA at 25°C. This current, in combination with the current through R_1, generates a 100-nV, constant-DC drop. Note that this voltage drop does not change with the ADC's bit decisions. It is true that the input bias current of the OPA350 changes over temperature, but a maximum current that is no more than 10 nA at 125°C can be expected. This value generates a change of 100 µV over a temperature range of 100°C.

It is useful to put the voltage drop across R_1 into perspective. This voltage drop is added to the errors contributed by the REF50xx and the OPA350. The initial error of the REF50xx output is ±0.05%, with an error over temperature of 3 ppm/°C. With a 4.096-V reference (REF5040), the initial reference error is equal to 2.05 mV at room temperature and an additional 1.23 mV at 125°C. Therefore, the reference output error is significantly larger than the errors produced by R_1 and variations in the OPA350's offset and input bias current.

Amplifier stability

There is a final word of caution about the circuit in Figure 6. The stability of the OPA350 can be compromised if C_4 and the OPA350's open-loop output resistance (R_{O_OPA350}) modify the open-loop voltage-gain (A_{OL}) curve to create a marginally stable state. To illustrate this phenomenon, Figure 7 shows how the output capacitor (C_4), with a 0.2-Ω ESR and the OPA350's open-loop output resistance (43 Ω), modifies the OPA350's A_{OL} curve. These curves can be used to quickly determine the stability of the circuit. A circuit with good stability would basically be one where the rate of closure of the operational amplifier's modified A_{OL} curve and closed-loop voltage-gain (A_{CL}) curve is

Figure 7. Frequency response of buffer with an RC load



20 dB/decade. This rule of thumb is presented in Reference 4. The open-loop output resistance of the OPA350 is 43 Ω, and the ESR of C_4 (R_{ESR_C4}) is 200 mΩ. The frequency locations of the pole and zero that are created by these values are

$$f_{pole} = \frac{1}{2\times\pi\times(R_{O\_OPA350} + R_{ESR\_C4})\times C_4} = 368 \text{ Hz and}$$

$$f_{zero} = \frac{1}{2\times\pi\times R_{ESR\_C4}\times C_4} = 79.6 \text{ kHz.}$$

Per Figure 7, the circuit in Figure 6 is stable.

Thinking ahead

Unfortunately, the voltage-reference designs in this article can degrade ADC performance by adding unwanted temperature drift and initial gain error. Higher-performance systems with 21+ bits may require a voltage-reference design that addresses these issues. Future articles will explore a new approach with auto-zero amplifiers that will compensate for these errors.

References

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Document Title	TI Lit. #
1. Bonnie Baker and Miro Oljaca, "How the Voltage Reference Affects ADC Performance, Part 1," *Analog Applications Journal* (2Q 2009)	slyt331
2. Miro Oljaca and Bonnie Baker, "How the Voltage Reference Affects ADC Performance, Part 2," *Analog Applications Journal* (3Q 2009)	slyt339
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