Impact of sampling-clock spurs on ADC performance

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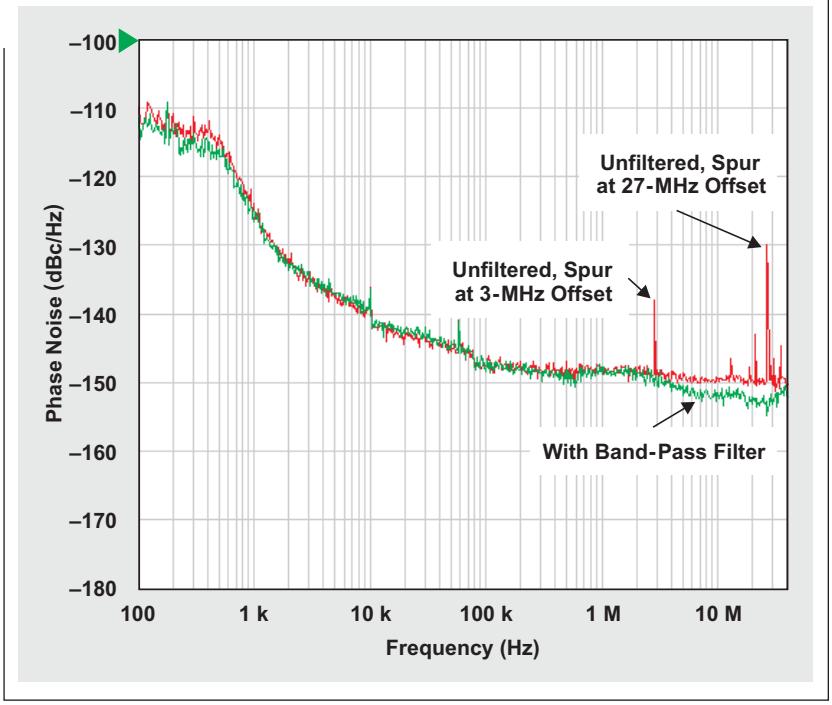
Introduction

As modern, high-speed analog-to-digital converters (ADCs) push the spurious-free dynamic range (SFDR) beyond the 100-dB barrier, the demand for a high-quality sampling clock has become greater than ever. Traditionally, system engineers focused mainly on the clock quality when they were trading off the signal-to-noise ratio (SNR) against the input-signal frequency in undersampling applications. As tougher system requirements such as multicarrier GSM emerge and are starting to demand dynamic ranges in excess of 80 dB over a wide bandwidth, system designers try to eliminate any possible SFDR degradation, such as the spur feedthrough from a distorted sampling clock.

Spurs on the sampling clock as low as –90 dBc can significantly impact the SFDR of the data converter. These low-level spurs can be very difficult to track down because they can have a variety of different origins. They can be generated from crosstalk with an adjacent digital circuit that occurs due to layout constraints, or they can occur simply because the clock source is not properly filtered. An example of improper filtering is shown in Figure 1, which compares two LVDS outputs of the Texas Instruments (TI) CDCE72010, one unfiltered and one with a band-pass filter. The spur reduction of the filtered output is clearly visible.

Figure 1. Phase noise of CDCE72010's filtered and unfiltered LVDS outputs



This article will discuss how spurs on the sampling clock get translated into the output spectrum of the data converter. It will also investigate how the spur amplitude changes with different input frequencies. More and more system designers are moving to an undersampling architecture, and the spur amplitude is highly dependent upon input frequency, as will be shown later. This article will also show how to estimate the SNR degradation caused by the sampling-clock spurs.

Sampling theory

The spurs that result from sampling a data converter with a distorted clock are best described by the relationship of their frequency and amplitude components to the same components of the sampled input signal. In order to derive that relationship, one has to start with the basic sampling theory. Let's consider the setup shown in Figure 2, where the input signal is

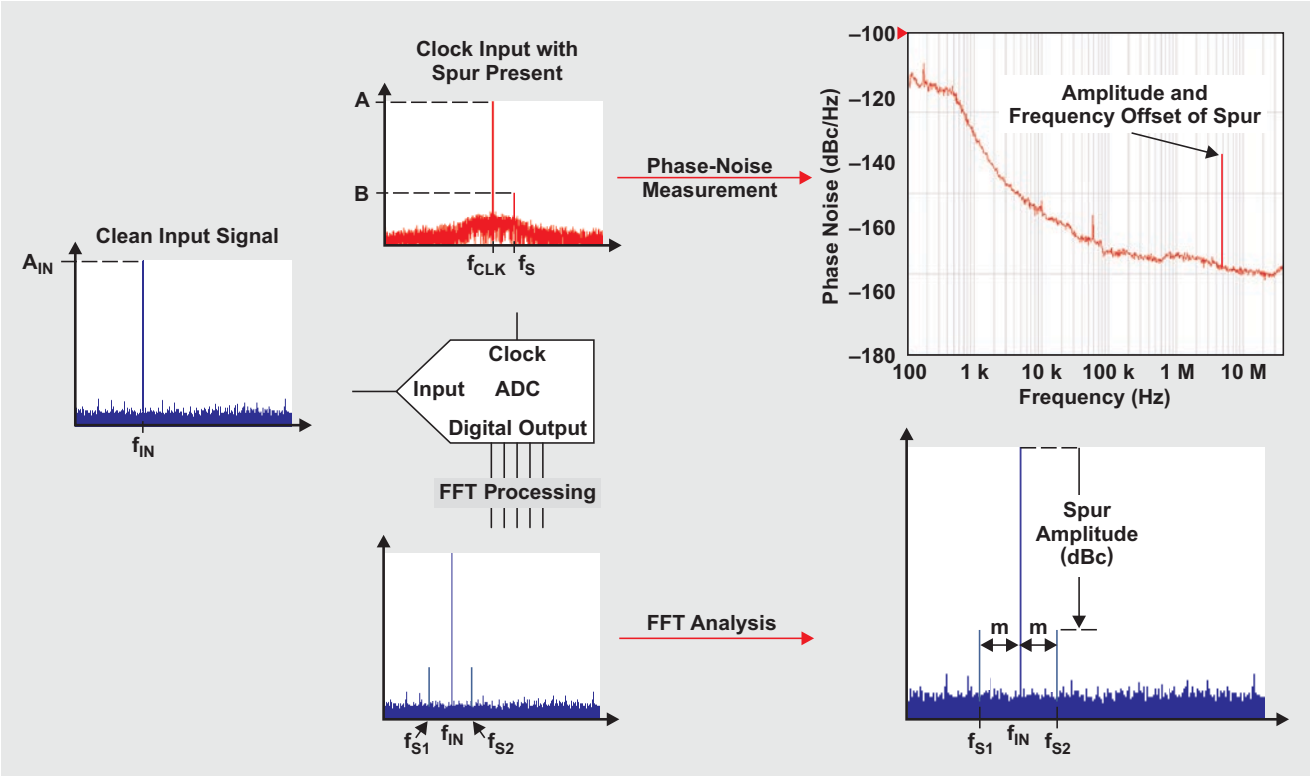
$$x(t) = A_{IN} \times \sin(\omega_{IN} t),$$

and the clock input with a spurious component is

$$y(t) = A \times \sin(\omega_{CLK} t) + B \times \sin(\omega_S t).$$

The quality of the sampling clock can easily be evaluated with a phase-noise analyzer. It displays the clock's phase noise versus frequency offset from the carrier, which is very helpful when the clock jitter is calculated to determine the SNR of the receiver. The phase-noise plot displays any spurious component on the clock signal, referencing its frequency offset and spur amplitude, S_X, to the main signal. If the amplitude is normalized in dBc/Hz, care must be

Figure 2. Setup with input signal, clock, and clock spur



taken to extract it with the resolution bandwidth of the instrument in that measurement:

$$\text{Amplitude (dBc)} = S_X \text{ (dBc/Hz)} + 10\log(\text{Resolution Bandwidth})$$

Due to the presence of the spur, the original sampling instant, or zero crossing of the clock, has shifted slightly by ΔT. Now the sampling instant, $y(t) = 0$, can be solved for:

$$y(t) = A \times \sin[\omega_{CLK}(t+\Delta T)] + B \times \sin[\omega_S(t+\Delta T)] = 0$$

$$y(t) = A \times \sin(\omega_{CLK}t) \times \cos(\omega_{CLK}\Delta T) + A \times \cos(\omega_{CLK}t) \times \sin(\omega_{CLK}\Delta T) + B \times \sin(\omega_S t) \times \cos(\omega_S \Delta T) + B \times \cos(\omega_S t) \times \sin(\omega_S \Delta T) = 0$$

Assuming that $B << A$ and $\Delta T \approx 0$ results in: $\cos(\omega_{CLK}\Delta T) \approx 1$ $\sin(\omega_{CLK}\Delta T) \approx \omega_{CLK}\Delta T$

$\cos(\omega_S \Delta T) \approx 1$ $\sin(\omega_S \Delta T) \approx \omega_S \Delta T$

The ideal sampling instant is $t = 0$, hence: $\sin(\omega_{CLK}t) = 0$ $\cos(\omega_{CLK}t) = 1$ $\cos(\omega_S t) = 1$

Substituting these results into $y(t) = 0$ produces:

$$y(t) = A \times \underbrace{\sin(\omega_{CLK}t)}_{0} \times \underbrace{\cos(\omega_{CLK}\Delta T)}_{1} + A \times \underbrace{\cos(\omega_{CLK}t)}_{1} \times \underbrace{\sin(\omega_{CLK}\Delta T)}_{\omega_{CLK}\Delta T} + B \times \sin(\omega_S t) \times \underbrace{\cos(\omega_S \Delta T)}_{1} + B \times \underbrace{\cos(\omega_S t)}_{1} \times \underbrace{\sin(\omega_S \Delta T)}_{\omega_S \Delta T} = 0$$

$$y(t) = A \times \omega_{CLK}\Delta T + B \times \sin(\omega_S t) + B \times \omega_S \Delta T = 0$$

Then ΔT can be solved for: $\Delta T = -\dfrac{B \times \sin(\omega_S t)}{A \times \omega_{CLK} + B \times \omega_S}$. Assuming that $A >> B$ results in $\Delta T = -\dfrac{B \times \sin(\omega_S t)}{A \times \omega_{CLK}}$.

Next, the input signal, $x(t) = A_{IN} \times \sin(\omega_{IN}t)$, is sampled at the zero crossing, $t + \Delta T$, of the non-ideal clock:

$$x(t) = A_{IN} \times \sin(\omega_{IN}T) = A_{IN} \times \sin\left[\omega_{IN}(t+\Delta T)\right] = A_{IN} \times \sin(\omega_{IN}t) \times \underbrace{\cos(\omega_{IN}\Delta T)}_{1} + A_{IN} \times \cos(\omega_{IN}t) \times \underbrace{\sin(\omega_{IN}\Delta T)}_{\omega_{IN}\Delta T}$$

This results in $x(t) = \underbrace{A_{IN} \times \sin(\omega_{IN} t)}_{\text{Ideal Sample}} + \underbrace{A_{IN} \times \cos(\omega_{IN} t) \times \omega_{IN} \Delta T}_{\text{Error Sample}}$.

Focusing on the error sample and substituting ΔT produces:

$$x(t) = A_{IN} \times \omega_{IN} \times \frac{-B \times \sin(\omega_S t)}{A \times \omega_{CLK}} \cos(\omega_{IN} t) = \underbrace{A_{IN} \times \omega_{IN} \times \frac{B}{A \times \omega_{CLK}} \times \frac{1}{2}}_{\text{Scale Factor of Spur Amplitude}} \underbrace{\left\{ \sin\left[(-\omega_S + \omega_{IN}) \times t\right] + \sin\left[(-\omega_S - \omega_{IN}) \times t\right] \right\}}_{\text{Two Frequency Products: } -\omega_S + \omega_{IN} \text{ and } -\omega_S - \omega_{IN}}$$

Therefore, it can be observed that each spurious component of the sampling clock generates two spurs, S1 and S2, in the data converter with amplitude and frequencies relative to the input signal as follows.

S1 and S2 amplitude: $\frac{B}{A} \times \frac{\omega_{IN}}{2 \times \omega_{CLK}} = \frac{B}{A} \times \frac{f_{IN}}{2 \times f_{CLK}}$ or, in terms of decibels,

$$= B - A + 20 \log\left(\frac{f_{IN}}{2 \times f_{CLK}} \right).$$

S1 and S2 frequencies: $f_{S1} = -f_S - f_{IN}$

$f_{S2} = -f_S + f_{IN}$

The resulting spurs can be shifted by one clock period, $2\pi/T = f_{CLK}$, and considering $f_S - f_{CLK} = m$ yields:

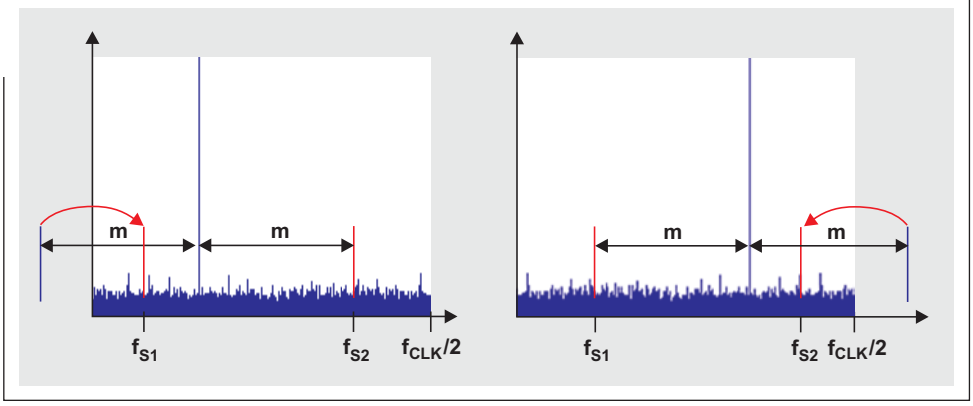
$f_{S1} = -f_S - f_{IN} + f_{CLK} = -f_{IN} + f_{CLK} - f_S = -(f_{IN} - f_{CLK} + f_S) = -(f_{IN} + m) = f_{IN} + m$

$f_{S2} = -f_S + f_{IN} + f_{CLK} = +f_{IN} + f_{CLK} - f_S = f_{IN} - m$

These equations show that the frequencies of the generated spurs will be centered around the input signal and offset by the distance m, which is the difference between the clock frequency and the clock-spur frequency. The amplitude of the generated spurs, on the other hand, is highly dependent upon the input frequency. For every doubling of the input frequency (e.g., f_{IN} = 20 MHz versus f_{IN} = 10 MHz), the spur amplitude increases by 6 dB! Hence, as system designers consider sampling in higher Nyquist zones, this relationship becomes very important to them.

Sometimes the fast Fourier transform (FFT) plot can be a bit misleading when one is trying to trace spurs back to their origins. If the clock spur is relatively far from the clock frequency, the generated spurs of the ADC can get pushed outside the plot's boundaries—either to negative frequencies or beyond $f_{CLK}/2$. The spurs then alias back in-band and generate an asymmetric FFT plot, as demonstrated in Figure 3.

Figure 3. Spurs pushed outside the FFT band and aliased back in-band



Measurements

To further demonstrate the impact of the spur's frequency and amplitude, the following experiment was set up (see Figure 4). A low-jitter-signal generator was used to provide a sine-wave input signal to TI's ADS5463 evaluation module (EVM). The ADC input was sampled with a 122.88-MHz clock, and a power combiner and third signal generator were used to mix a spur into the clock's frequency. This way the frequency and amplitude of the spur could easily be adjusted. The spur's amplitude and frequency were verified with a phase-noise analyzer.

For the first experiment, the spur generator was set up to output a tone with a frequency of 102 MHz and an amplitude of –30 dBm. The power combiner reduced the clock and spur signals by about 3 dB. The phase-noise analyzer showed the amplitudes of the clock and spur at –9 dBm and about –33 dBm, respectively, with an offset (m) of about 20.9 MHz (122.88 MHz – 102 MHz) as illustrated in the screen capture in Figure 5. As previously derived, this setup generated two spurs with a spur-amplitude scale factor of

$$B - A + 20\log\left(\frac{f_{IN}}{2\times f_{CLK}}\right) = -33\ \text{dBm} - (-9\ \text{dBm}) + 20\log\left(\frac{10\ \text{MHz}}{2\times 122.88\ \text{MHz}}\right) = -51.8\ \text{dBc}$$

and spur frequencies of

$f_{S1} = f_{IN} + m = 10\ \text{MHz} + 20.9\ \text{MHz} = 30.9\ \text{MHz}$ and

$f_{S2} = f_{IN} - m = 10\ \text{MHz} - 20.9\ \text{MHz} = -10.9\ \text{MHz}$.

Figure 4. Test setup to mix a spur and clock signal

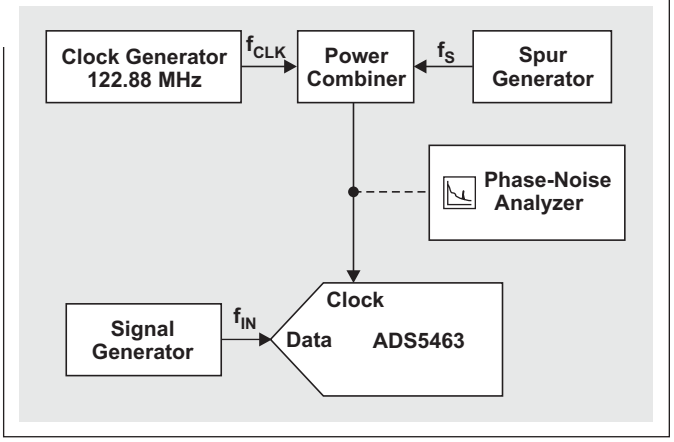
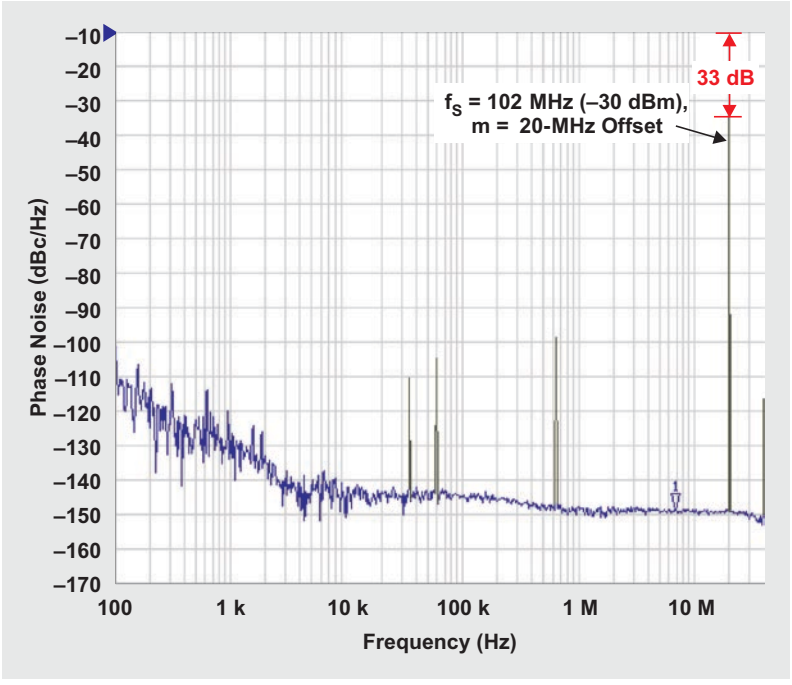


Figure 5. Phase-noise plot of 102-MHz spur with –33-dBm amplitude

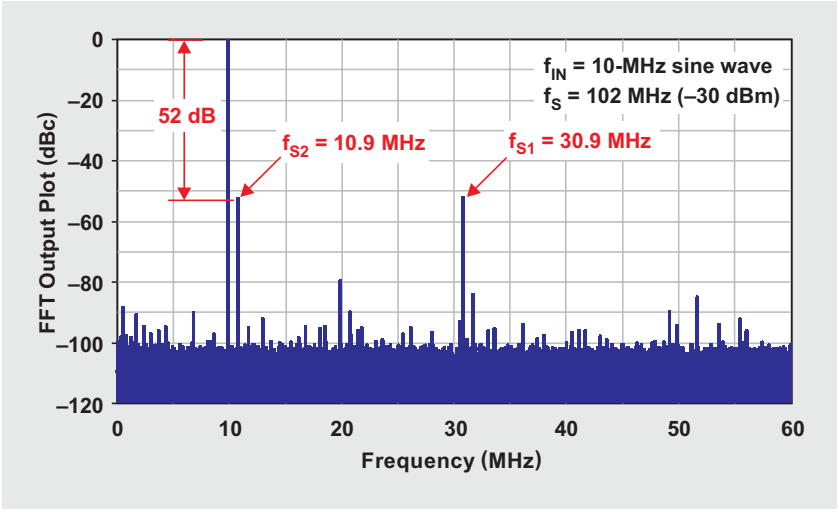


The resulting FFT plot of the ADS5463 output is shown in Figure 6. The generated spurs are about 52 dB lower than the input signal and are located at 10.9 and 30.9 MHz. This matches the calculated values very closely.

Next, the spur amplitude was lowered from –30 dBm to –40 dBm. It was expected that the S1 and S2 spur amplitudes would drop by 10 dB as well. This was confirmed with the FFT plot of the ADS5463 output, as illustrated in Figure 7. The frequencies of the spurs stayed the same.

As discussed previously, the spur amplitude is highly dependent upon the frequency of the input signal. To further illustrate this, the frequency of the input signal was increased from 10 MHz to 100 MHz. This changed the spur-amplitude scale factor to

Figure 6. FFT output of 102-MHz, –30-dBm clock spur



$$B - A + 20\log\left(\frac{f_{IN}}{2\times f_{CLK}}\right) = -33\text{ dBm} - (-9\text{ dBm}) + 20\log\left(\frac{100\text{ MHz}}{2\times 122.88\text{ MHz}}\right) = -24 - 7.8 = -31.8\text{ dBc}$$

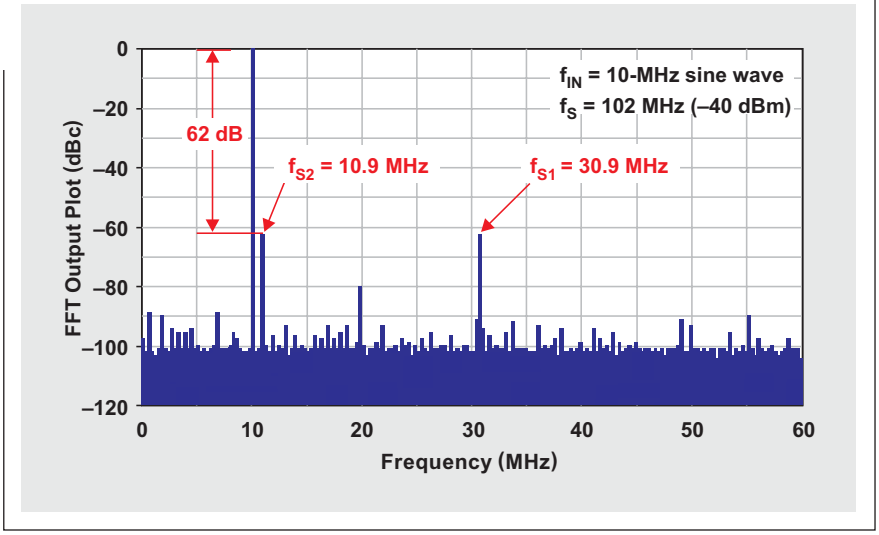
and the frequencies of the two spurs to $f_{S1} = -f_S + f_{IN} = -102\text{ MHz} + 100\text{ MHz} = -2\text{ MHz}$ and

$f_{S2} = -f_S - f_{IN} = -102\text{ MHz} - 100\text{ MHz} = -202\text{ MHz}$.

Aliasing them back in-band generated two spurs, $f_{S1} = -2\text{ MHz} = +2\text{ MHz}$ and

$f_{S2} = -202\text{ MHz} + (2\times 122.88\text{ MHz}) = 43.8\text{ MHz}$.

Figure 7. FFT output of 102-MHz, –40-dBm clock spur



This was also confirmed with the FFT plot of the ADS5463 output (see Figure 8).

For the last experiment, a comparison of spur frequencies was made with the clock frequency set at 102 MHz and at 132 MHz. The spur amplitude was set to –30 dBm, and the input signal was set to 10 MHz. These settings caused the spur-frequency offset (m) to change from about 20.9 MHz to about 9.1 MHz, respectively. Two new spur frequencies resulted:

$f_{S1} = f_{IN} + m = 10\ MHz + 9.1\ MHz = 19.1\ MHz$

$f_{S2} = f_{IN} - m = 10\ MHz - 9.1\ MHz = 0.9\ MHz$

Once again, this correlated very well with the FFT output plot from the ADS5463, as illustrated in Figure 9.

Practical example

Let's go back and analyze the case of the CDCE72010, mentioned earlier under "Introduction." This device's low-jitter phase-locked loop was configured to drive the TI ADS5483 with LVDS outputs at 122.88 MSPS. No filter was placed between the outputs of the CDCE72010 and the clock input of the ADS5483. This way the full effect of the clock spurs in a real-world design can be observed.

Figure 8. FFT output of 102-MHz, –30-dBm clock spur

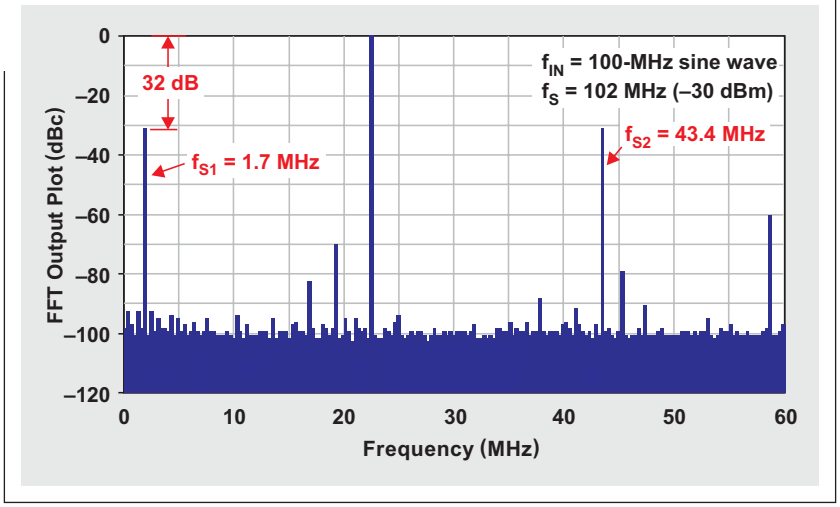
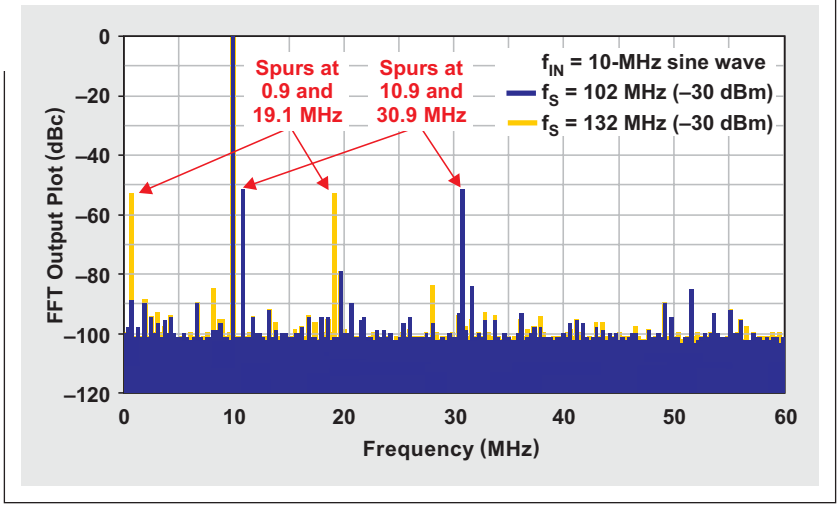


Figure 9. FFT output of –30-dBm clock spur at 132 MHz versus 102 MHz



The phase-noise plot of the unfiltered CDCE72010 in Figure 10 shows two spurs that will impact the SFDR performance of the ADS5483.One spur (S1) is offset about 27 MHz with an amplitude of about –130 dBc/Hz; the other spur (S2) is offset about 3 MHz with an amplitude of about –138 dBc/Hz. The actual spurs are 6 dB lower than shown in the plot because the phase-noise analyzer sums the spurs of the two sidebands together.

The amplitudes of the two spurs can be converted from dBc/Hz to dBc as described before:

$$\text{For S1, } 136 \text{ dBc/Hz} = -136 \text{ dBc} + 10\log(27 \text{ MHz} \times 1\%)$$
$$= -136 \text{ dBc} + 54.4 \text{ dB}$$
$$= -81.6 \text{ dBc}.$$
$$\text{For S2, } -144 \text{ dBc/Hz} = -144 \text{ dBc} + 10\log(3 \text{ MHz} \times 1\%)$$
$$= -144 \text{ dBc} + 45 \text{ dB}$$
$$= -99 \text{ dBc}.$$

These results can be used to calculate the spur amplitudes of the ADC output spectrum:

$$S1 = 81.6 \text{ dBc} + 20\log\left(\frac{100 \text{ MHz}}{2 \times 122.88 \text{ MHz}}\right)$$
$$= -81.6 \text{ dBc} - 7.8 \text{ dB}$$
$$= -89.4 \text{ dBc}$$
$$S2 = -99 \text{ dBc} + 20\log\left(\frac{100 \text{ MHz}}{2 \times 122.88 \text{ MHz}}\right)$$
$$= -99 \text{ dBc} - 7.8 \text{ dB}$$
$$= -106.8 \text{ dBc}$$

These amplitudes match the measured spur amplitudes of the ADC output spectrum fairly well (within 1 to 2 dB), as shown in Figure 11.

Figure 10. Phase-noise plot of CDCE72010's unfiltered LVDS output

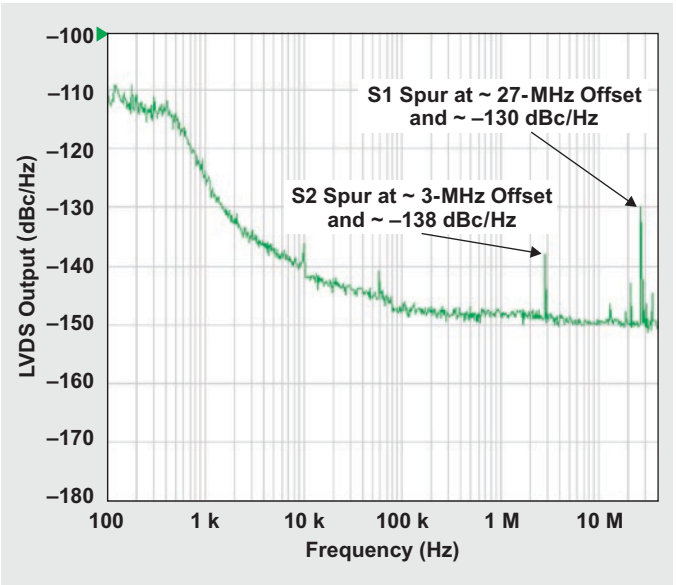


Figure 11. FFT output with 100-MHz input and a 122.88-MHz LVDS clock

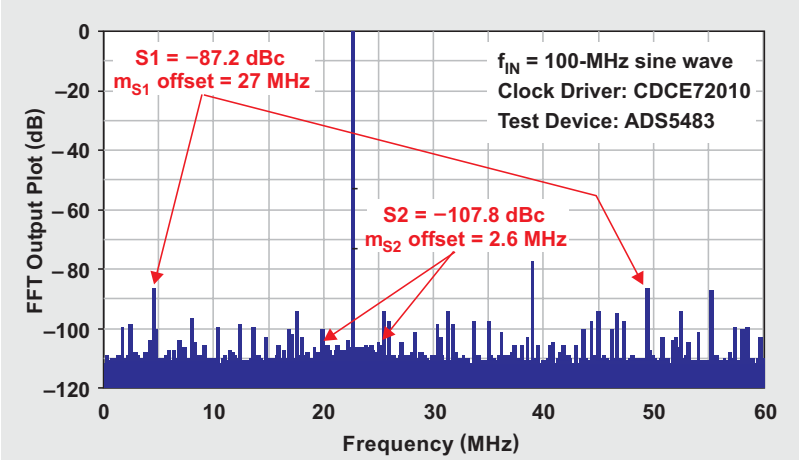
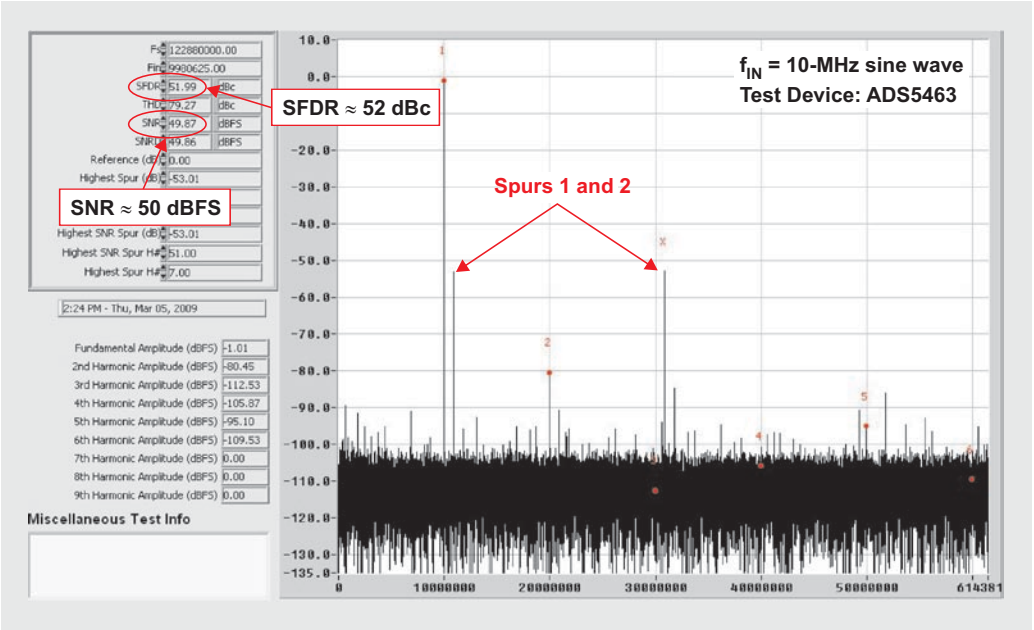


Figure 12. FFT output with 122.88-MHz clock and a 102-MHz, –30-dBm spur



Impact of clock spurs on SNR

Besides reducing the SFDR, spurs on the clock also impact the SNR of the data converter. Since the spurs are at a fixed frequency, they are considered deterministic jitter (DJ); and they contribute to the overall clock jitter, which in turn highly impacts the SNR.

The peak-to-peak DJ from the clock spur can be approximated by

$$DJ_{PP} \approx \frac{2\times10^{\frac{S_X(dBc)}{20}}}{\pi\times f_{CLK}},$$

where S_X (dBc) is the spur amplitude in dBc. The RMS jitter can be calculated as

$$DJ_{RMS} \approx \frac{DJ_{PP}}{14}.$$

As in the first experiment, with the measured amplitude of the spurs at –33 dBm and that of the clock at about –10 dBm, the relative spur amplitude is roughly

$$-33\text{ dBm} - (-10\text{ dBm}) = -23\text{ dBc}.$$

Substituting –23 dBc into the formula for DJ_{RMS} yields

$$DJ_{RMS} \approx \frac{DJ_{PP}}{14} = \frac{1}{14}\times\frac{2\times10^{\frac{-23}{20}}}{\pi\times122.88\text{ MHz}} = 26\text{ ps}.$$

Since there are two spurs with a 20-MHz offset, the 26-ps DJ of each spur can be summed together for a total DJ of about 52 ps.

For calculating the SNR of the data converter, the DJ needs to be added to the phase noise of the clock and the aperture jitter of the ADC. However, in this case, the DJ far exceeds the other two jitter components. Therefore, the resulting SNR can be calculated with a jitter of about 52 ps (f_{IN} = 10 MHz), which is approximately 50.5 dBFS.

The resulting FFT plot of this setup with the ADS5463 is shown in Figure 12. The plot clearly shows the two resulting spurs with an amplitude of –52 dBc and an SFDR of about –52 dBc. The SNR ≈ 50 dBFS, which matches the calculated value very well.

Conclusion

This article has shown that spurs on the ADC sampling clock can significantly degrade the overall system SFDR as well as the SNR. This effect gets amplified even more in undersampling applications where the signal input is moved to higher frequencies than those traditionally used for baseband input. Therefore, it can be concluded that a filtered, high-quality sampling clock is necessary for system engineers who are trying to achieve maximum data-converter performance.

Related Web sites

dataconverter.ti.com
www.ti.com/sc/device/*partnumber*
Replace *partnumber* with ADS5463, ADS5483, or CDCE72010

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