High-Performance Analog Products

Analog Applications Journal

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Introduction

Analog Applications Journal is a collection of analog application articles designed to give readers a basic understanding of TI products and to provide simple but practical examples for typical applications. Written not only for design engineers but also for engineering managers, technicians, system designers and marketing and sales personnel, the book emphasizes general application concepts over lengthy mathematical analyses.

These applications are not intended as "how-to" instructions for specific circuits but as examples of how devices could be used to solve specific design requirements. Readers will find tutorial information as well as practical engineering solutions on components from the following categories:

- Power Management
- Interface (Data Transmission)
- Amplifiers: Op Amps

Where applicable, readers will also find software routines and program structures. Finally, *Analog Applications Journal* includes helpful hints and rules of thumb to guide readers in preparing for their design.

Paralleling power modules for high-current applications

By Jason Arrigo
Plug-In Power Applications

Introduction

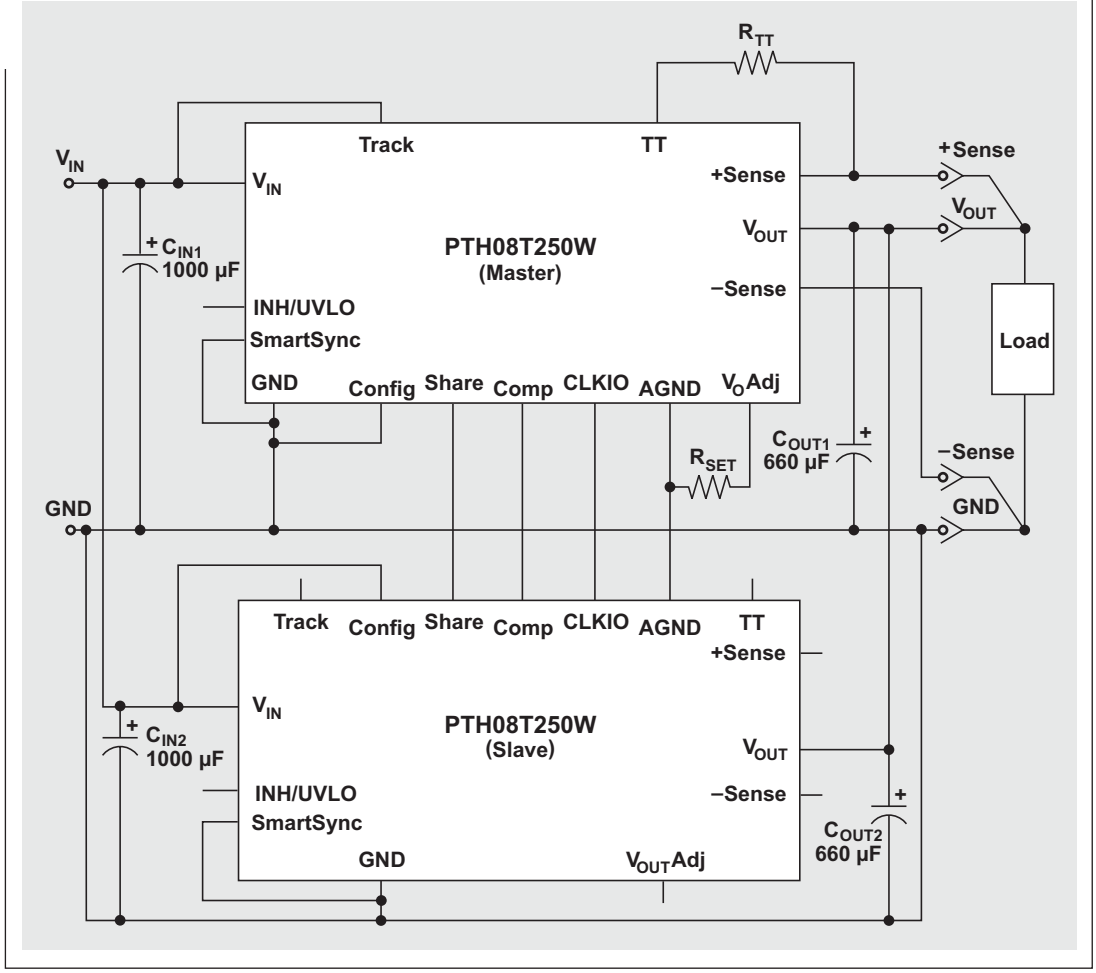
Powering servers and memory cards requires the generation of low supply voltages at very high DC currents approaching 100 A or more. In addition to the high-current-supply requirements, dynamic load requirements are extremely demanding. The load may quickly go from an inactive low-current state to a fully processing high-current state while requiring precise voltage regulation.

Paralleling power modules

A stand-alone, dual-phase power module like the Texas Instruments (TI) PTH08T250W can supply up to 50 A of output load current. However, the PTH08T250W incorporates TI's TPS40140 stackable-controller feature that allows the outputs of multiple modules to be connected in parallel, thereby producing a reliable solution capable of supplying a load current of 100 A or more.

Configuring a PTH08T250W as a master and each additional module as a slave allows start-up and transient conditions to be controlled by a single module. Figure 1 shows a typical two-module solution where all of the features and inputs are controlled by the master device while the slave inputs are left open.

Figure 1. Typical two-module solution



Considerations for paralleling PTH08T250W modules

Input and output capacitors

When multiple PTH08T250W modules are paralleled, the amount of capacitance must be enough to filter the input and output and meet the transient requirements of the high-current application. The amount of capacitance must be calculated for a single module and then multiplied by the number of parallel modules.

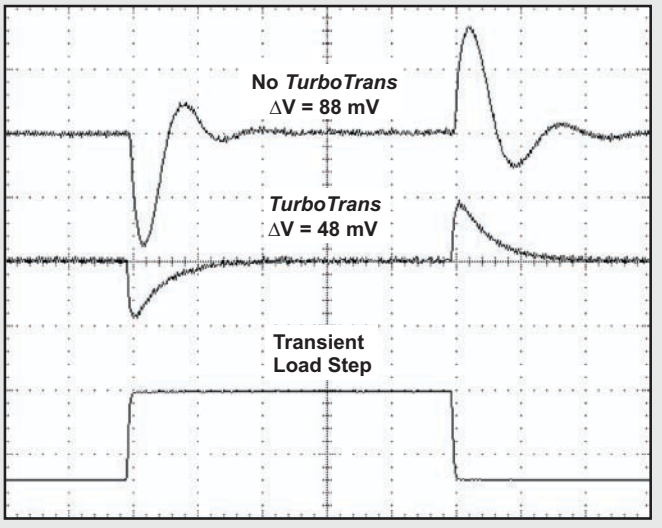
Each device requires a 16-V, 1000-µF, OS-CON capacitor along with three to four 16-V, 22-µF, X5R ceramic capacitors directly at the input pins of the module. The ceramic capacitors are required to reduce any ripple and switching noise across the input bus.

The required output capacitance must be determined by the transient requirement of the application. The maximum current step required by the load must be divided by the number of modules being paralleled. The *TurboTrans*™ graphs in the datasheet should then be used to determine the amount of output capacitance per module. High-quality, low-ESR polymer-tantalum or OS-CON output capacitors are required for this application. A list of approved capacitors is included in the PTH08T250W datasheet.

TurboTrans technology

The PTH08T250W power module features *TurboTrans* technology, which allows a power-supply designer to adjust the module to meet a specific transient-load requirement. The *TurboTrans* feature is set only on the master module with a single resistor, R_{TT}. The result is a high-current application with faster transient response, increased stability, and less output capacitance to meet tight requirements for output-voltage deviation. The benefits of *TurboTrans* are shown in Figure 2. The transient response to a load step is shown with and without the *TurboTrans* feature.

Figure 2. Transient response to load step with and without *TurboTrans*



Parallel connections

When multiple modules are operated in parallel, the control of each device feature is set only on the master device. A device is configured as a master by connecting the Config pin to the power GND. All slave devices must connect the Config pin to V_{IN}. The slave devices must leave all other control pins open (connect the SmartSync pin to the GND). See Table 1 for pin connections of the master and slave modules.

Table 1. Master and slave pin connections

PIN NAME	MASTER	SLAVE
V_{IN}	Connect to the input bus.	Connect to the input bus.
V_{OUT}	Connect to the output bus.	Connect to the output bus.
GND	Connect to the common power GND.	Connect to the common power GND.
INH/UVLO	Use for inhibit control and UVLO adjustment. If unused, leave open-circuit.	No connection. Leave open-circuit.
V_{OUT} Adjust	Use to set the output voltage. Connect R_{SET} resistor between this pin and AGND.	No connection. Leave open-circuit.
+Sense	Connect to the output voltage either at the load or at the module.	No connection. Leave open-circuit.
–Sense	Connect to the output GND either at the load or at the module.	No connection. Leave open-circuit.
Track	Connect to Track control. If unused, connect to V_{IN}.	No connection. Leave open-circuit.
TurboTrans	Connect *TurboTrans* resistor, R_{TT}, between this pin and +Sense pin.	No connection. Leave open-circuit.
SmartSync	Connect to an external clock. If unused, connect to GND.	Connect to the common power GND.
Config	Connect to the common power GND.	Connect to the input bus.
Share	Connect to pin 2 of the slave.	Connect to pin 2 of the master.
Comp	Connect to pin 3 of the slave.	Connect to pin 3 of the master.
AGND	Connect to pin 4 of the slave.	Connect to pin 4 of the master.
CLKIO	Connect to pin 5 of the slave.	Connect to pin 5 of the master.

Board layout

Special attention must be paid to the board layout for a parallel application. The amount of board space, the number of layers, and the amount of copper will determine the amount of current each solution can deliver. A careful layout is required to keep the interconnection pins as clean as possible.

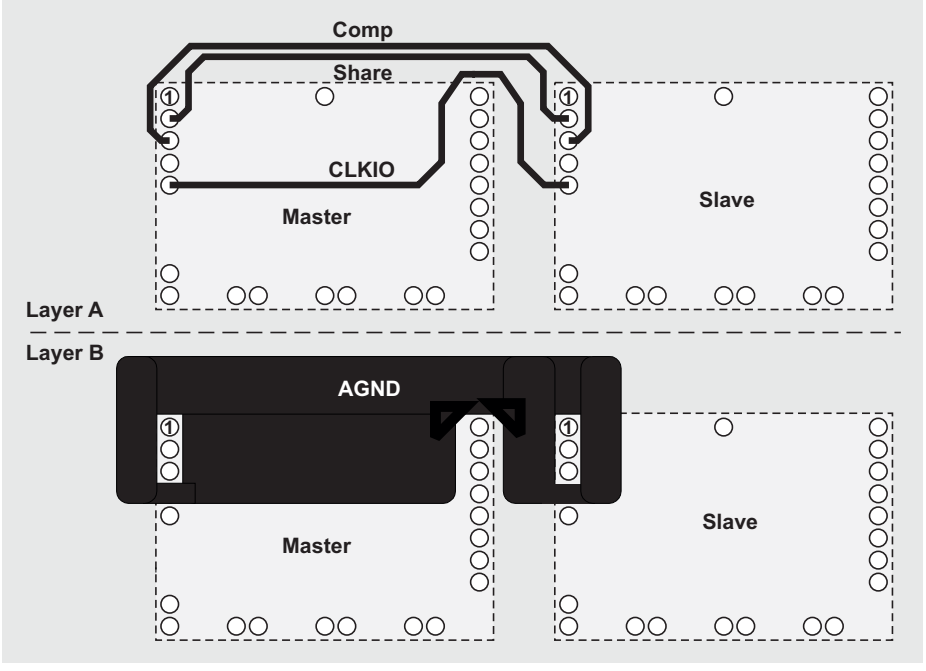
The power planes, V_{IN}, V_{OUT}, and GND, must be routed to the power pins in a tight, short, and wide path. Keeping the V_{IN} plane from running above or below the V_{OUT} plane wherever possible will help reduce overall switching noise. Keeping a short and tight path from the output of each module to the load is required to minimize losses.

The +Sense and –Sense connections must be routed to the load in a direct path, closely coupled with one another. The layout around these traces should be isolated as much as possible to avoid picking up switching noise. Additionally, connecting the ±Sense lines through a surface-mount resistor to the load allows a 1- to 2-Ω resistor to be placed in the sense path to aid in filtering.

The three interconnection traces (Share, Comp, and CLKIO) must be isolated from the rest of the board to keep switching noise from aggravating the signals to the slave modules. The AGND should act as a shield and be run on an adjacent layer to the other three traces. Care must be taken in routing the CLKIO trace to keep it slightly away from the Comp trace to reduce the chance of the clock pulses disturbing the Comp signal. See Figure 3 for an example layout of the interconnection pins. The three interconnection traces are routed on one layer, and the AGND is routed as a copper area that shields the three traces on an adjacent layer.

When multiple modules are operated in parallel, an eight-layer layout with 2-oz. copper is recommended to improve thermal conduction. Increased copper thickness is required to distribute the higher current over the power planes. Increased airflow is also strongly recommended to help the copper remove the heat associated with the higher-power solution.

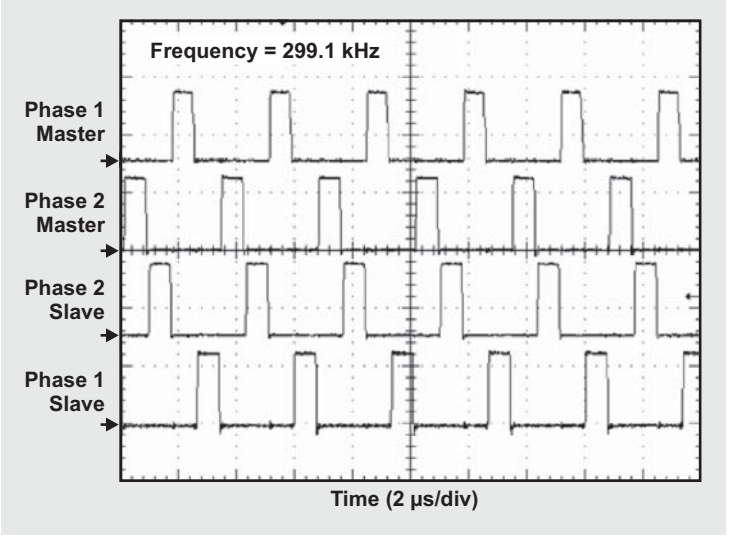
Figure 3. Example board layout of interconnection pins



Four-phase operation

When operated in parallel, the slave modules are synchronized to the frequency of the master. Each PTH08T250W is a two-phase device; each phase operates 180° out of phase. Placing two modules in parallel results in a four-phase operation by shifting the slave-module phases by 90° (see Figure 4). However, driving the master with an external frequency via SmartSync eliminates the 90° phase shift.

Figure 4. Four-phase operation



Four-phase operation results in a reduction of input and output voltage ripple. Each phase draws current from the input source out of phase, minimizing source loading. Four-phase operation also adds to the already exceptional transient response of the module, responding more quickly and delivering current more evenly to the load.

When multiple PTH08T250W modules operate in parallel, all slave modules operate in phase with one another, 90° out of phase with the master. Once again, driving the master with an external frequency eliminates the 90° phase shift.

PTH08T250W features

The PTH08T250W operates over a wide 4.5- to 14-V input-voltage range and generates a positive output voltage of 0.7 to 3.6 V. Additionally, the PTH08T2xxW family of power modules is designed to meet a very tight 1.5% DC tolerance, deliver exceptional transient response, and have the ability to synchronize to an external frequency.

This article also applies to the PTH08T255W, a spin-off of the PTH08T250W designed to produce a 5-V, 40-A output. The PTH08T255W operates over an 8- to 14-V input-voltage range, and the output voltage can be set from 3.0 to 5.25 V.

Related Web sites

power.ti.com
www.ti.com/sc/device/PTH08T250W
www.ti.com/sc/device/PTH08T255W

Improving battery safety, charging, and fuel gauging in portable media applications

By Jinrong Qian
Battery Management Applications Manager

Introduction

Portable media players and smartphones have become very popular over the past five years. The portable media player is a handheld device that can record and play back audio/video from a TV, DVD player, camera, or media file downloaded from the Internet. A smartphone is a mobile phone offering advanced capabilities beyond those of a typical mobile phone, often with PC-like functionality. Most smartphones can operate as complete personal organizers that support full-featured email programs. Other features might include a miniature "qwerty" keyboard; a touch screen; a built-in camera; contact management; built-in navigation hardware and software; the ability to read business documents in a variety of formats such as Adobe® Acrobat® and Microsoft® Office files; and media software for playing music, browsing photos, and viewing video clips or Internet browsers.

The high demand of smartphones for increased power to perform these tasks reduces battery run time. A common way to extend battery run time is to design the power-conversion system to be more efficient by using high-efficiency, synchronous switching regulators instead of linear regulators. To extend the battery standby time, the DC/DC converters can be designed to optimize the light-load efficiency by operating in pulse-frequency-modulation mode, while the pulse-width-modulated controller IC operates in low-quiescent-current mode during system standby.

In addition to extending battery life, three very important parts of portable-power design are system safety, battery charging, and fuel-gauging accuracy. These are the focus of this article.

Improving battery safety

Due to their high gravimetric and volumetric energy density, Li-Ion and Li-Polymer batteries are widely used in portable devices. One of the greatest design challenges is the safety of the battery-operated system. There have been several recalls of battery-operated portable devices such as laptop computers and cellular phones due to safety issues arising from the use of counterfeit batteries. Memory chips with a unique battery-identification number, such as the Texas Instruments (TI) bq2022A or a SHA-1-based security chip such as the TI bq26100, can verify whether a battery is from an authorized vendor and therefore safe to use.

Battery temperature is another critical parameter for battery safety. An excessive operating temperature accelerates cell degradation and causes thermal runaway and explosion in Li-Ion batteries. This is a specific concern with this type of battery because of its highly aggressive active material. Rapid temperature increases can occur if a battery is overcharged at high current or has an internal short. During overcharging of a Li-Ion battery, active metallic lithium is deposited onto the anode. This material dramatically increases the danger of explosion that can occur when it reacts with a variety of materials, including electrolyte and cathode materials. For example, a lithium/carbon-intercalated compound reacts with water, and the released hydrogen can be ignited by the heat of the reaction. Cathode material such as $LiCoO_2$ starts reacting with the electrolyte when the temperature exceeds its thermal-runaway threshold of 175°C with 4.3-V cell voltage. On the other hand, charging a battery at low temperatures also shortens battery life, since the lithium ion can be deposited onto the anode and become the metallic lithium that easily reacts with the electrolyte. The lithium ion permanently disappears and no longer participates in the energy storage.

It is very critical for a battery-charge-management circuit to monitor the battery temperature. The battery charge current and charge voltage can be adjusted to maintain battery temperature within limits specified by the manufacturer. A thermistor is usually used to monitor the Li-Ion cell temperature for cell overtemperature protection. For example, a Li-Ion battery is usually not allowed to charge when the cell temperature is below 0°C or above 45°C; nor is it allowed to discharge when the cell temperature is above 65°C.

The battery is deeply discharged when its voltage is below 3.0 V. A precharge safety timer is often used to detect whether the battery has an internal short circuit. The safety timer can trigger a warning signal to be sent to the end user if the battery could not charge to 3.0 V within the specified precharge time period. The fast-charge safety timer provides another level of protection, terminating the battery charging if the timer expires due to an unexpected system failure.

Battery-charge-management ICs such as TI's bq24060 and bq24070 typically include battery-temperature monitoring and precharge and fast-charge safety timers to improve battery safety.

Operating the system while charging a deeply discharged battery

In many portable media applications, being able to operate the system while simultaneously charging a deeply discharged battery is desirable, since the end user may make a phone call or play games regardless of the battery condition as long as the adapter is available.

Figure 1 shows a commonly used battery-charging and system-power architecture where the system is directly connected to the battery. This architecture is simple and low-cost, but connecting a system load to the battery can cause various issues.

In this configuration, the charger output current, I_{CHG}, is not dedicated to charging the battery but shared between the system and the charger. Therefore, the charger cannot directly monitor and control the battery's effective charge current.

A small precharge current is used to charge a deeply discharged battery when the cell voltage falls below 3.0 V. The system load, I_{SYS}, uses some portion of this current, making the effective charge current even smaller. This not only increases battery charging time but may also cause a false expiration of the precharge timer because the battery voltage cannot rise to 3.0 V within the precharge time period. It's even possible for the system current to be larger than the precharge current, thereby discharging the battery instead of charging it. In addition, a minimum system bus voltage of 3.0 V is usually required to operate the system in many portable applications. The system cannot operate when a deeply discharged battery voltage is used as the system bus voltage in this power architecture.

These issues are caused by the interaction between the charger and the system, which can be eliminated by powering the system and charging the battery via independent power paths. This technique is known as power-path management (PPM).

Figure 2 shows a simplified block diagram of a PPM configuration. MOSFET Q1 is used either as a switch or to preregulate the system bus voltage, V_{OUT}, at a set value such as 4.4 V (for example). Either way, a direct path from the input to the system is established for providing power to the system. MOSFET Q2 is dedicated to fully controlling the battery charging, so the system no longer interferes, and the false safety-timer expiration is completely eliminated. System operation is guaranteed and independent of the battery conditions whenever the adapter is available.

Another technique for supplying system power and charging the battery simultaneously is dynamic PPM (DPPM). DPPM monitors the system bus voltage, V_{OUT}, for drops in input power that are due to current limiting or removal of the input supply. When the current required by the system and battery charger is greater than the input current available from the AC adapter or USB, the bus output capacitor, C_{OUT}, starts to discharge, causing the system bus voltage to drop. Once the system bus voltage falls to the preset DPPM threshold, the charge current is reduced so that the total current demand from the system and battery charger is equal to the maximum current available from the adapter. This maximizes the use of the power available from the adapter or USB. Most system loads are very dynamic, with a high peak current. Since the average power from the system is much smaller than its peak power, the adapter will be overdesigned if its power rating is based on the peak power from the system and battery charger. DPPM allows the designer to use a smaller power rating and a less expensive AC adapter.

Figure 1. Block diagram of battery-charging and system-power architecture

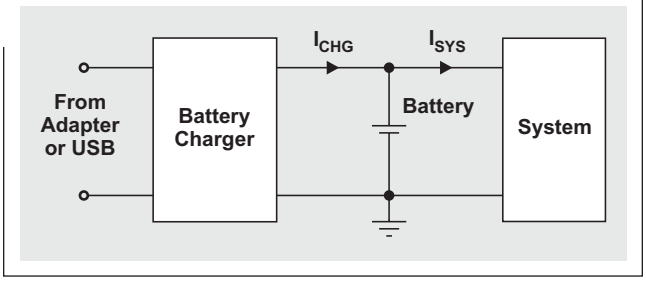


Figure 2. Simplified block diagram of PPM battery charger

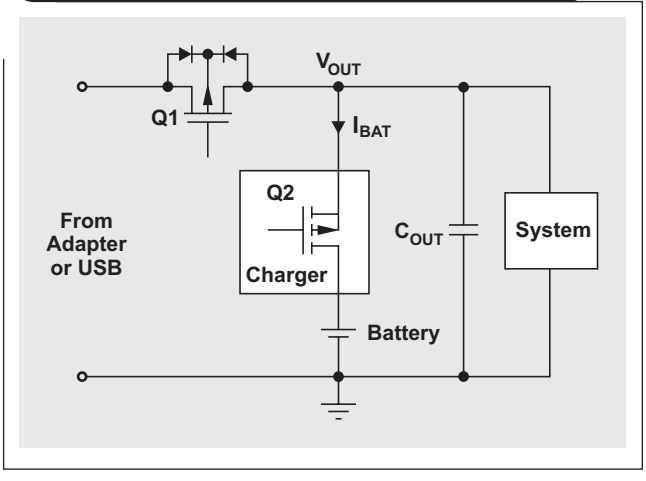


Figure 3. DPPM battery charger

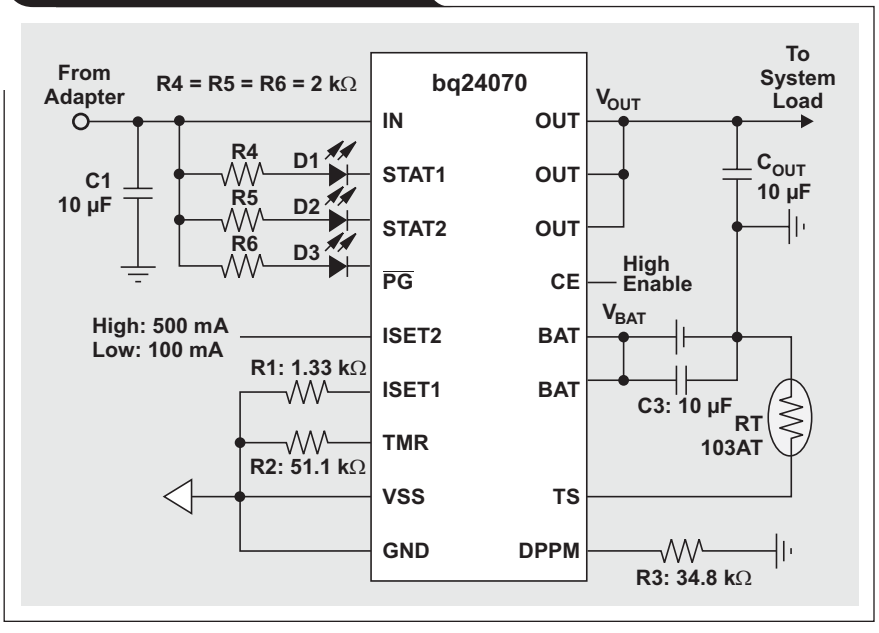
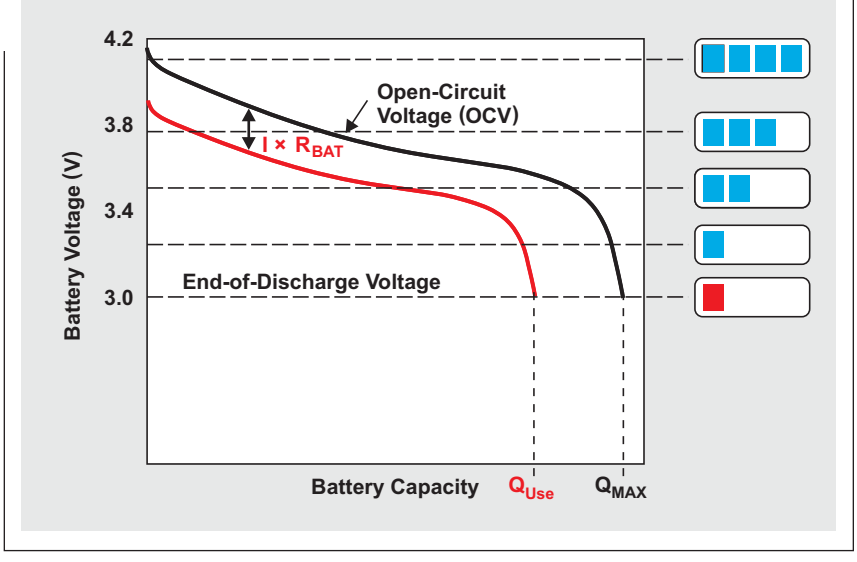


Figure 3 shows an example DPPM Li-Ion battery charger. A thermal regulation loop reduces the charge current to prevent the silicon temperature from exceeding 125°C. Whenever the charge current is reduced because of active thermal regulation or active DPPM, the safety timer's precharge time is automatically increased to eliminate a false safety-timer expiration.

Figure 4. Performance of typical voltage-based fuel gauge with bar indicators



Fuel-gauging accuracy

Some of the end user's most commonly asked questions include: "How much battery life do I have left in my portable device? How many songs or games can I play with my portable device?" A few simple bar indicators in cellular phones, for example, may not be enough to answer these questions. Battery state-of-charge (SOC) indication has evolved from a simple warning to a more complex system-level use of the information, such as soft shutdown to prevent data loss. An error in capacity estimation equivalently reduces the usable run time available to the end user. Using a capacity indicator with 10% error is the same as using a battery with 10% less capacity or a power-conversion system with 10% less efficiency.

Conventional fuel-gauging technologies, mainly the voltage-based and the coulomb-counting algorithms, have obvious performance limitations. Widely adopted in hand-held devices such as cellular phones, the voltage-based method suffers from changes in battery resistance over time. The battery voltage is given by

$$V_{BAT} = V_{OCV} - I \times R_{BAT}, \quad (1)$$

where V_{OCV} is the battery open-circuit voltage (OCV) and R_{BAT} is the battery internal DC resistance. Figure 4 shows the relationship between the battery voltage and the fuel-gauge bar indicators. Many end users have experienced fuel-gauge bar jumps and sudden system shutdown when

the usable capacity, Q_{Use}, has fallen below Q_{MAX} because of an increase in internal resistance. The coulomb-counting method takes the alternative approach by continuously integrating coulombs to compute the consumed charge and SOC. With a previously determined value for full capacity, the remaining capacity can be obtained. The drawback of this approach is that self-discharge is difficult to model since it is a function of aging and temperature. Without periodic full-cycle calibration, the gauging error accrues over time. Neither of these algorithms addresses the resistance variations of the battery. To avoid an unexpected shutdown, the designer must reserve more capacity by terminating system operation prematurely, leaving a significant amount of energy unused.

TI's patented Impedance Track™ technology is a unique and much more accurate method of determining the remaining battery capacity than either the voltage-based or the coulomb-counting algorithm alone. It actually uses both techniques to overcome the effects of aging, self-discharge and temperature variations. The Impedance Track technology implements a dynamic modeling algorithm to learn and track the battery's characteristics by first measuring and then tracking the impedance and capacity changes during actual battery use. It provides near-real-time information such as the battery's run time, maximum operating temperature, cycle count, maximum cell voltage, and maximum charging and discharging current. It is a self-learning mechanism that accounts for the no-load chemical capacity (Q_{MAX}) and the aging effects that cause the battery's resistance to change. Compensation for load and temperature is modeled accurately with the aid of cell-impedance knowledge. With this algorithm, no periodic full-cycle capacity learning is required. System design can be relieved from conservative shutdown, allowing the battery's full capacity to be utilized. Most important, fuel-gauging accuracy can be maintained during the whole lifetime of the battery.

For Impedance Track technology to work, a database of tables must be constantly maintained to keep battery resistance (R_{BAT}) as a function of depth of discharge (DOD) and temperature. To understand when these tables are updated or utilized, we need to know what operations occur during different states. Several current thresholds are programmed into the nonvolatile gauge memory to define a charge; a discharge; and "relaxation time," which is time that allows the battery voltage to stabilize after charging or discharging ceases.

Before a handheld device is turned on, the Impedance Track technology determines the exact SOC by measuring the battery OCV, then correlating it with the OCV(DOD,T) table stored in the IC. When the device operates in an active mode and a load is applied, current-integration-based coulomb counting begins. Integration of the passed charge measured by the coulomb counter is used to continuously calculate the SOC.

The total battery capacity, Q_{MAX}, is generally reduced by 3 to 5% after 100 cycles. To know the real maximum capacity of the battery, we need to measure and update Q_{MAX}. The total capacity is calculated through two OCV readings taken at fully relaxed states when the variation of battery voltage is small enough before and after charge or discharge activity. As an example, before the battery is discharged, the SOC is given by

$$SOC_1 = \frac{Q_1}{Q_{MAX}}, \quad \textbf{(2)}$$

where Q_1 is the available charge from the battery before discharge. After the battery is discharged with a passed charge of ΔQ, the SOC is given by

$$SOC_2 = \frac{Q_2}{Q_{MAX}}, \quad \textbf{(3)}$$

where Q_2 is the available charge from the battery after discharge. Subtracting and rearranging these two equations yields

$$Q_{MAX} = \frac{\Delta Q}{\left|SOC_1 - SOC_2\right|}, \quad \textbf{(4)}$$

where $\Delta Q = Q_1 - Q_2$. Equation 4 illustrates that it is not necessary to have a complete charge and discharge cycle to determine the total battery capacity, which means the time-consuming battery-learning cycle can be eliminated from pack manufacturing.

The battery-resistance table, $R_{BAT}(DOD,T)$, is updated constantly during discharge, and the resistance is calculated as

$$R_{BAT}(DOD,T) = \frac{OCV(DOD,T) - \text{Battery Voltage Under Load}}{\text{Average Load Current}}. \quad \textbf{(5)}$$

This enables the Impedance Track technology to compute when the termination voltage will be reached at the present load and temperature. Knowing the battery resistance, we can determine the remaining capacity (RM) using a voltage-simulation method in the firmware. Simulation starts from the present SOC_{Start}, and the future battery-voltage profile is calculated under the same load currents by decreasing SOC repeatedly in small steps. When the simulated battery voltage, $V_{BAT}(SOC_1,T)$, reaches the battery termination voltage, typically 3.0 V, the SOC corresponding to this voltage is captured as SOC_{Final}. RM can then be calculated as

$$RM = (SOC_{Start} - SOC_{Final}) \times Q_{MAX}. \quad \textbf{(6)}$$

Figure 5 shows a typical circuit that uses a system-side Impedance Track fuel gauge, the bq27500-V120, in a portable media application. To accurately compensate for the aging effect, the battery impedance is measured in real time and updated in every battery-discharge cycle. Up to 99% fuel-gauge accuracy can be achieved over the lifetime of the battery.

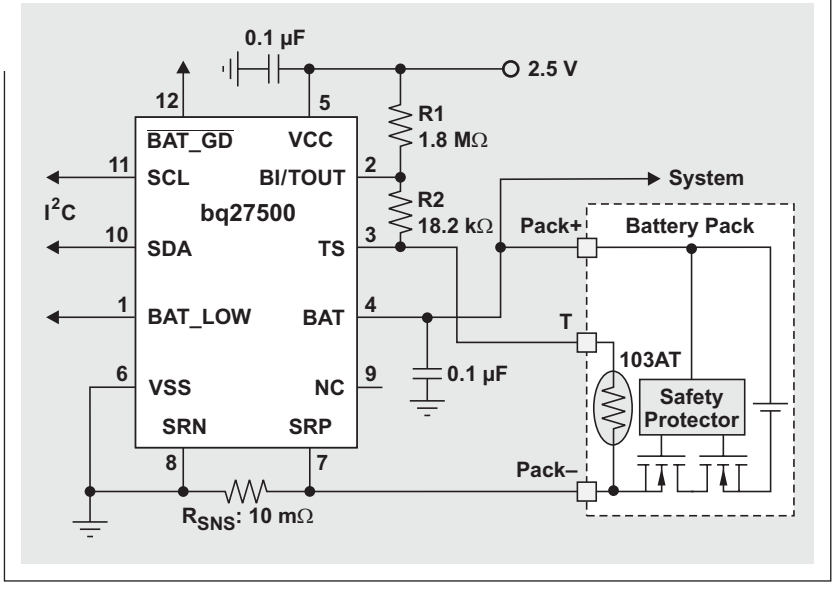
Conclusion

Battery-power management plays a critical role in battery safety by preventing overcharging, overdischarging, and overtemperature conditions. The PPM battery charger can operate the system while simultaneously charging a deeply discharged battery. PPM also eliminates charger and system interaction by providing separate power paths from the input power source to the system and the battery. The Impedance Track fuel gauge reports the remaining battery capacity with up to 99% accuracy, providing full use of all available battery energy and extending battery run time.

Related Web sites

power.ti.com
www.ti.com/sc/device/*partnumber*
Replace *partnumber* with bq2022a, bq24060, bq24070, bq26100, or bq27500-V120

Figure 5. Typical application circuit with single-cell Impedance Track fuel gauge



Cell balancing buys extra run time and battery life

By Sihua Wen
Applications Engineer, Battery Management Solutions

Introduction

Common to every battery system with series cells is the problem of cell imbalance. Cell balancing is a method of designing safer battery solutions that extends battery run time as well as battery life. The latest battery-protection and fuel-gauging ICs from Texas Instruments (TI)—the bq2084, the bq20zxx family, the bq77PL900, and the bq78PL114—present a wealthy lineup for cell-balancing needs.

What is cell imbalance?

If overheated or overcharged, Li-Ion cells are prone to accelerated cell degradation and can catch fire or even explode. Hardware and software protection is in place to mitigate these immediate dangers. In a multicell battery pack, which is commonly used in laptop computers and medical equipment, placing cells in series opens up the possibility of cell imbalance, a slower but persistent degradation of the battery.

No two cells are identical. There are always slight differences in the state of charge (SOC), self-discharge rate, capacity, impedance, and temperature characteristics, even for cells that are the same model from the same manufacturer and even from the same batch of production. When building multicell packs, manufacturers usually sort cells with similar SOCs by voltage. However, variations in an individual cell's impedance, capacity, and self-discharge rate can still lead to a divergence in its voltage over time. Since most battery chargers detect full charge by checking whether the voltage of the entire string of cells has reached the voltage-regulation point, individual cell voltages can vary as long as they do not exceed the limits for overvoltage (OV) protection. However, weak cells—i.e., cells with lower capacity or higher internal impedance—tend to exhibit higher voltage than the rest of the series cells at full charge termination. These cells are weakened further by continuous overcharge cycles. The higher voltage of weak cells at charge completion causes accelerated capacity degradation.

On the other hand, in discharge, the weak cells tend to have lower voltage than the other cells, due to either higher internal resistance or the faster rate of discharge that results from their smaller capacity. This means that if any of the weak cells hits the cell undervoltage-protection limit while the pack voltage is still sufficient to power the system, the full capacity of the battery will not be used.

Cell-balancing techniques

The impact of cell imbalance on run-time performance and battery life in applications using series-connected cells is certainly undesirable. The fundamental solution of cell balancing equalizes the voltage and SOC among the cells when they are at full charge. Cell balancing is usually categorized into two types—passive and active. The passive cell-balancing method, also known as "resistor bleeding balancing," is simple and straightforward: Discharge the cells that need balancing through a dissipative bypass route. This bypass can be either integrated or external to the IC. Such an approach is favorable in low-cost system applications.

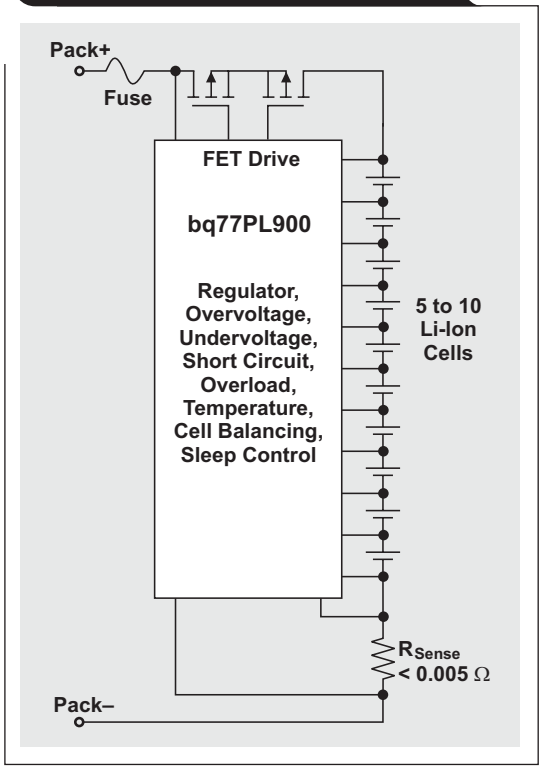
The fact that 100% of the excess energy from a higher-energy cell is dissipated as heat makes the passive method less preferable to use during discharge because of the obvious impact on battery run time. Active cell balancing, which utilizes capacitive or inductive charge shuttling to transfer charge between battery cells, is significantly more efficient because energy is transferred to where it is needed instead of being bled off. Of course, the trade-off for this improved efficiency is the need for additional components at higher cost.

Passive cell balancing

The easiest approach to cell balancing is to equalize cell voltages. For example, the bq77PL900, a battery-pack protector for 5 to 10 Li-Ion series cells, is used in cordless power tools, power-assisted bicycles and scooters, uninterruptible power supplies, and medical equipment. The bq77PL900 can act as a stand-alone battery-protection

system (see Figure 1), comparing cell voltages with programmable thresholds to determine if cell balancing is needed. Figure 2 shows the operation principle. If any particular cell hits the threshold, charging is halted and an internal bypass is enabled. The charging is halted until the high-voltage cell hits the recovery limit, when the cell balancing will stop.

Figure 1. The bq77PL900 acting as stand-alone battery protector



Cell-balancing algorithms that use only voltage divergence as a balancing criterion have the disadvantage of overbalancing or underbalancing because of the different impedance between cells (see Figure 3). The problem is that cell impedance also contributes to voltage divergence during charging. The pack protector using simple voltage-based cell balancing cannot tell if the voltage difference is caused by the capacity or the impedance imbalance. Therefore, this type of balancing cannot guarantee that all cells will reach 100% capacity at full charge.

The bq2084 is a fuel gauge with an improved version of voltage-based balancing. To minimize the effect of impedance differences between cells, the bq2084 balances only near the end of charge, where the current tapers off. In addition, the bq2084 is a more efficient implementation

Figure 2. Simple passive cell balancing based on voltage

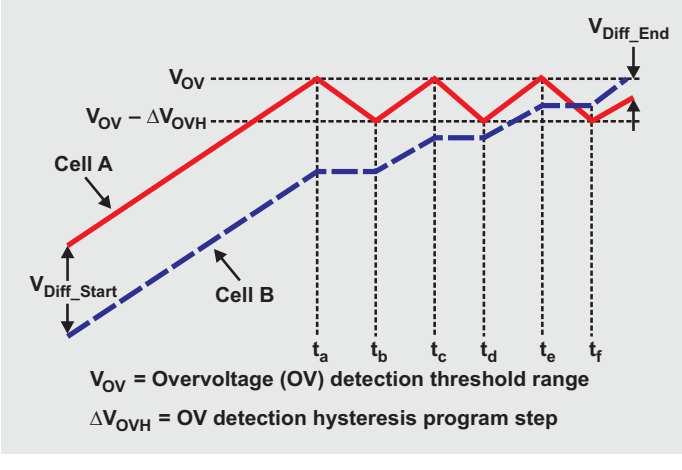
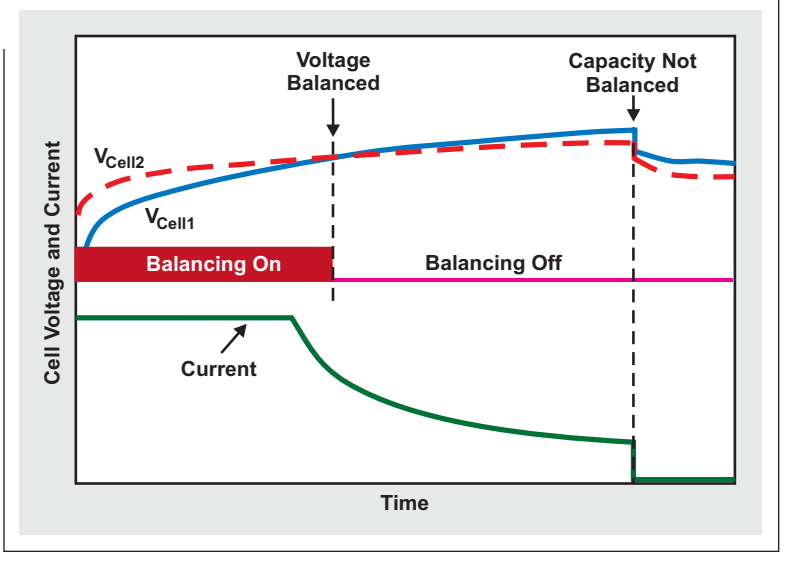


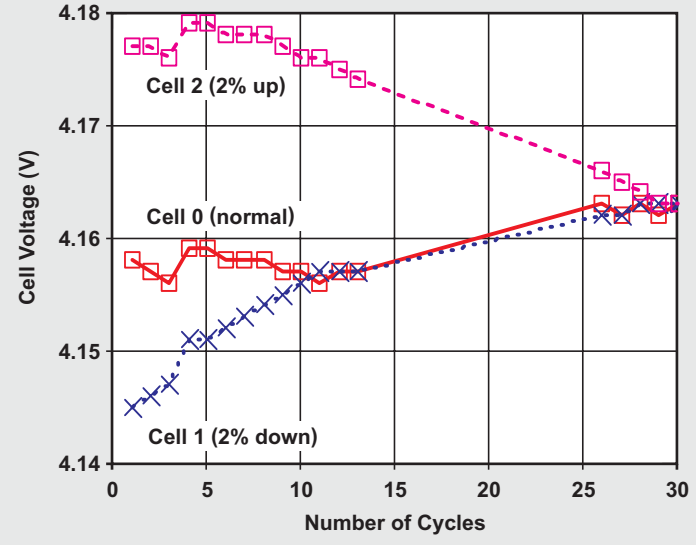
Figure 3. Simple voltage-based cell balancing may not effectively balance capacity



because it makes the balancing decision based on all cell voltages. Despite the improvements, this technique limits the balancing to high-SOC regions and can be performed only during charging.

The bq20zxx family of Impedance Track™ fuel gauges uses a different balancing strategy based on cell SOC and capacity. Instead of balancing voltage divergence, the bq20zxx gauges calculate the charge, Q_{need}, that each cell needs to reach a full-charge state, then find the difference, ΔQ, between the Q_{need} of each cell. The balancing algorithm turns on the cell-balancing FETs during charging to zero out ΔQ. The Impedance Track fuel gauges implement these tasks with ease because the total capacity, Q_{max}, and the SOC are readily available from the gauging function. Furthermore, since this method of cell balancing is not compromised by cell impedance (it actually monitors cell impedance), it can be performed at any time, during charge or discharge or even at idle. More important, it achieves the best passive-balancing accuracy (see Figure 4).

Figure 4. Passive cell balancing based on SOC and capacity



Active cell balancing

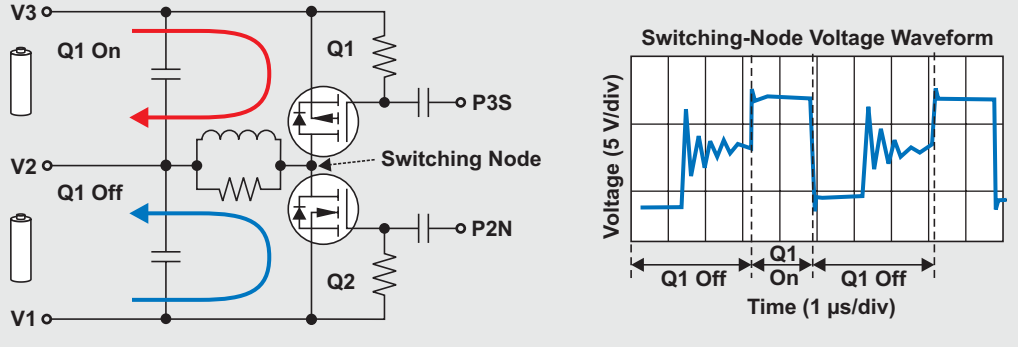
Active cell balancing overcomes the energy loss of the passive method by using capacitive or inductive charge storage and shuttling to deliver energy to where it is needed most, and with little loss. Thus it is preferable for efficiency-conscious designs and for applications where delivering maximum run time is top priority.

The bq78PL114 PowerPump™ cell-balancing technology is TI's latest implementation of active cell balancing using inductive charge transfer. PowerPump uses an n- and p-channel MOSFET pair and a power inductor to complete a charge-transfer circuit between an adjacent pair of cells. Shown in Figure 5, the MOSFETs and the power inductor form a buck/boost circuit. If the bq78PL114 determines that the top cell needs to transfer energy to the lower cell, the P3S signal, running at about 200 kHz with a duty cycle of 30%, triggers the energy to transfer from the top cell to the inductor through the top p-channel MOSFET, Q1. When the P3S signal resets, Q1 is turned off, and the energy stored in the inductor reaches a maximum. Because the inductor current must flow continuously, the body diode of Q2 is forward-biased, completing the charge transfer from the inductor to the lower cell. In this process, energy is stored in the inductor with only minor loss due to the series resistance of the inductor and the ON resistance of the body diode.

The bq78PL114 features three selectable balancing algorithms:

- *Terminal-voltage pumping* is just like the voltage-based passive cell balancing described earlier.
- *Open-circuit voltage (OCV) pumping* compensates for impedance differences by estimating the OCV based on measurements of the pack current and cell impedance.
- *SOC pumping (predictive balancing)* is like the bq20zxx family's passive cell-balancing method based on SOC and capacity. The SOC-pumping algorithm

Figure 5. PowerPump cell balancing

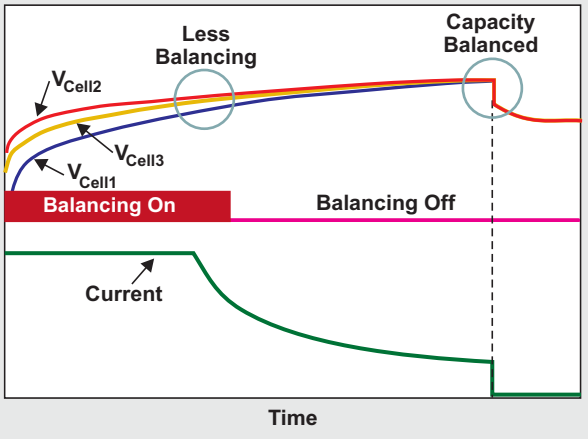


determines the exact charge that needs to be transferred between cells so that cell capacities are balanced at the end of charge. This method therefore achieves the best active-balancing accuracy, as shown in Figure 6.

Because of the higher balancing current, PowerPump technology corrects cell imbalance much better than conventional integrated, passive balancing with internal bypass FETs. Adjustable by changing component values, the typical effective balancing current for a notebook PC is about 25 to 50 mA, which is about 12 to 20 times better than the internal IC bypass balancing. With this strength, most typical capacity imbalances (of less than 5%) can be overcome in one or two cycles.

Apart from the obvious advantages, the beauty of the PowerPump cell-balancing technology is that balancing is achievable regardless of the individual cell voltages. Balancing can happen during any battery operation—charge, discharge, or rest—and even if the cell that provides the charge has a lower voltage than the cell that receives it! Compared with passive cell balancing, little energy is lost as heat.

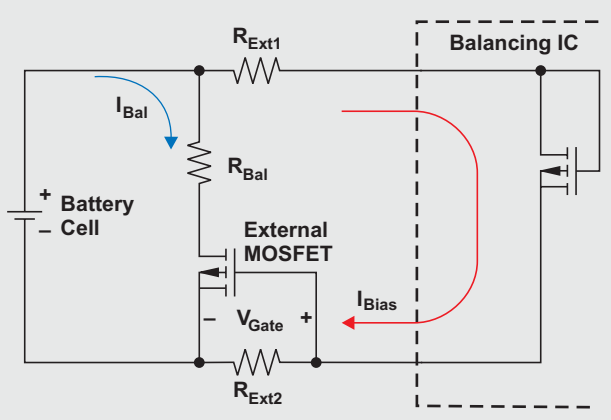
Figure 6. Active cell balancing with SOC-pumping algorithm



Performance considerations for passive and active cell balancing

PowerPump cell balancing is fast by nature. A 2% capacity imbalance from a 2200-mAh cell can be balanced within a charge cycle or two. However, as previously mentioned, passive cell balancing using integrated FETs is limited by low balancing current and therefore may require multiple cycles to correct a typical imbalance. The balancing may even be overpowered by the rate of cell divergence/imbalance. To improve the speed of passive cell balancing, an external bypass can be established to utilize existing hardware. A typical implementation, shown in Figure 7, can be used with the bq77PL900, the bq2084, or the bq20zxx family. The internal balancing MOSFET for a particular cell is first turned on, creating a low-level bias current through the external filter resistors, R_{Ext1} and R_{Ext2}, that connect the cell terminals to the IC. The gate-to-source voltage is thus established across R_{Ext2}, and the external MOSFET is turned on. The $R_{DS(on)}$ of the external MOSFET is negligible, and the external balancing current, I_{Bal}, is governed by cell voltage and R_{Bal}.

Figure 7. Principle of external passive cell balancing



The drawback of this method is that balancing cannot be performed on adjacent cells at the same time (see Figure 8a). This is because, when adjacent internal FETs are turned on, there is no current flowing through R_{Ext2}, so Q1 remains off even when the internal switch is enabled. In practice, this is not an issue because the fast external cell balancing can quickly balance the cell associated with Q2, and then the cell associated with Q1 will be balanced.

Another issue is the stress from the high drain-to-source voltage, V_{DS}, that occurs when every other cell is balanced. In Figure 8b, the top and bottom cells are being balanced. Due to the cell-balancing bias, there is a high V_{DS} at the middle internal switch that may exceed what the switch can sustain. The solution to this problem is to limit the maximum value of R_{Ext} or exclude simultaneous balancing of every other cell.

Fast cell balancing is a new way of thinking about enhancing battery safety and performance. In passive balancing, the practical goal is to achieve capacity balance at the end of charge; but, due to the low balancing current, little can be done to also correct voltage imbalance at the end of discharge. In other words, overcharging weak cells can be avoided, but it may not be possible to improve battery run time because the extra energy is wasted in the bypass resistance as heat. With fast PowerPump active balancing, the two goals—achieving capacity balance at the end of charge, and minimizing voltage differences among cells at the end of discharge—can potentially be achieved at the same time. Energy is conserved and transferred to weaker cells, which increases discharge capacity.

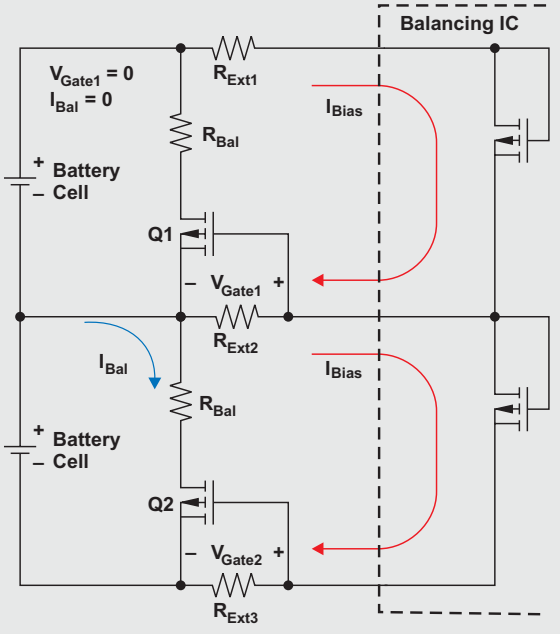
Conclusion

One of the emerging technologies for enhancing battery safety and extending battery life is advanced cell balancing. Since new cell balancing technologies track the amount of balancing needed by individual cells, the usable life of battery packs is increased, and overall battery safety is enhanced. In fast PowerPump active balancing, battery run time can also be maximized by balancing at high efficiency at the end of discharge in every cycle.

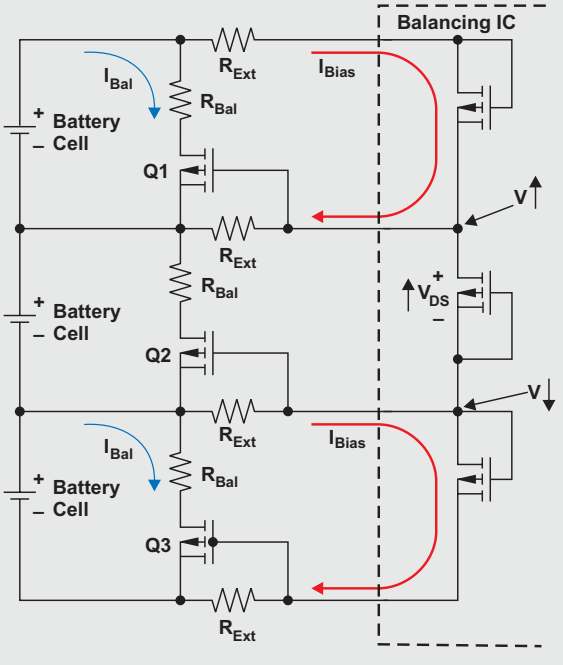
Related Web sites

power.ti.com
www.ti.com/sc/device/*partnumber*
Replace *partnumber* with bq2084-V143, bq20z90-V110, bq77PL900, or bq78PL114

Figure 8. Issues with internal-FET balancing



(a) Adjacent cells cannot be balanced at the same time



(b) High-V_{DS} stress occurs when every other cell is balanced

Using a portable-power boost converter in an isolated flyback application

By Jeff Falin, *Senior Applications Engineer,*
and Brian King, *Member, Group Technical Staff*

Some electronic applications require an isolated auxiliary power supply that must be generated from a low-voltage AC adapter. Examples of such applications include isolated MOSFET drive circuits and relay controls. Finding an isolated power-supply controller that will operate at such low voltages can prove difficult. Fortunately, it is possible to configure some low-power boost converters, such as the Texas Instruments (TI) TPS61175, to operate and control a flyback power stage. This article explains how to use the TPS61175 in an isolated flyback application.

Consider, for example, an application that is supplied from a 5-V wall wart and requires an isolated 5-V, 500-mA auxiliary supply. In this application, the input voltage can range from 3 to 6 V, and small size is a higher priority than efficiency. The low output-power and isolation requirements make the flyback an obvious choice for the power-supply topology. Taking into account the size limitations, a boost controller with an integrated FET is ideal for this type of application. With its 2.9-V minimum input voltage, the TPS61175 is one of the few boost converters that can meet these input-voltage specifications. In addition, the switching frequency of up to 2.2 MHz allows for a smaller transformer and reduced component sizes for the input and output filters.

The TPS61175 is a highly integrated current-mode controller. This controller internally limits the peak FET current to 3 A, which makes continuous conduction mode (CCM) a good choice. Selecting an operating frequency of 1 MHz keeps the switching losses manageable and reduces the transformer inductance and physical size. Although the TPS61175 includes a fixed amount of internal slope compensation, limiting the maximum duty cycle to less than 50% eliminates the possibility of bimodal operation and also reduces the rms current in the output capacitors.

Equation 1 computes the required primary-to-secondary turns ratio, N_{p2s}, of the transformer:

$$N_{p2s} = \frac{V_{IN(min)} \times D_{max}}{(V_{OUT} + V_d) \times (1 - D_{max})} \quad (1)$$

In order to limit the duty cycle to 45%, a ratio of 1:2.5 was selected. The internal MOSFET of the TPS61175 is rated for 40 V, so the voltage stress is not an issue for this design.

In CCM converters, using too large an inductance can cause the right-half-plane zero (RHPZ) to limit the bandwidth of the feedback loop. The location of the RHPZ is determined by Equation 2:

$$RHPZ = R_{Load} \times \frac{(1 - D)^2}{2\pi \times L_{Sec} \times D} \quad (2)$$

If this frequency is not significantly higher than the unity-gain frequency of the feedback loop, stability is jeopardized. Fortunately, with a 1-MHz switching frequency, a relatively large inductance can be used and still allow for an adequate loop bandwidth. Selecting a primary inductance of 1.2 µH keeps the converter in CCM operation down to a load current of 150 mA and puts the RHPZ in the neighborhood of 200 kHz.

The amount of output capacitance required for a given peak-to-peak output ripple voltage is determined by Equation 3:

$$C_{min} = \frac{I_{OUT} \times \left\{1 - D \times \left[V_{IN(max)}\right]\right\}}{f_{SW} \times V_{PP}} \quad (3)$$

In this design, using a single 22-µF ceramic capacitor limits the ripple voltage to 17 mV_{PP} with a 6-V input. Using another 22-µF ceramic capacitor on the input limits the input ripple voltage to similar levels.

Figure 1. TPS61175 boost controller used in simple isolated flyback

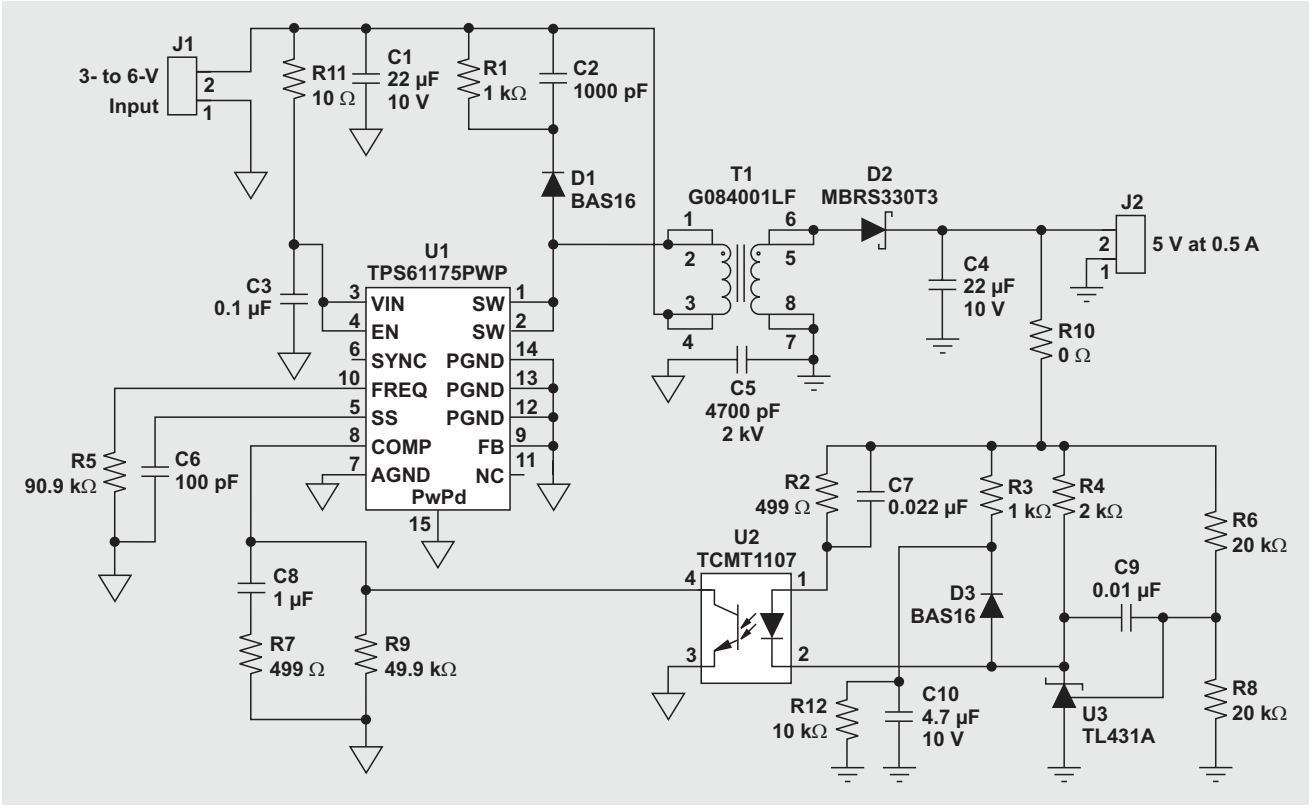


Figure 1 shows a schematic for this power-supply design. The TPS61175 contains a transconductance error amplifier. Normally, in nonisolated applications, the output voltage is fed back through a resistor divider to the feedback pin (FB, or pin 9). For an isolated feedback, the feedback pin must be grounded. This turns the output of the transconductance amplifier, located at the COMP pin, into a 130-µA current source. Connecting a 49.9-kΩ resistor (R9) from the COMP pin to ground allows the optocoupler to control the voltage of the COMP pin over its entire dynamic range (0.75 to 3 V).

The value of R2 must be small enough to allow the TI TL431 to sufficiently drive the optocoupler. The DC gain of the optocoupler circuit is determined by the current-transfer ratio (CTR), R2, and R9. Because the optocoupler needs to drive only 130 µA, the CTR is relatively low (approximately 10%), but the 100:1 ratio of R9 to R2 gives the optocoupler circuit a total DC gain of 20 dB. C8 and R7 were added to attenuate the gain and allow the loop to cross near 10 kHz. C8 and R9 form a pole at 30 Hz, while C8 and R7 form a zero at 3 kHz. This lowers the gain by 40 dB at frequencies above 3 kHz.

Figure 2. The optocoupler limits the bandwidth to around 10 kHz

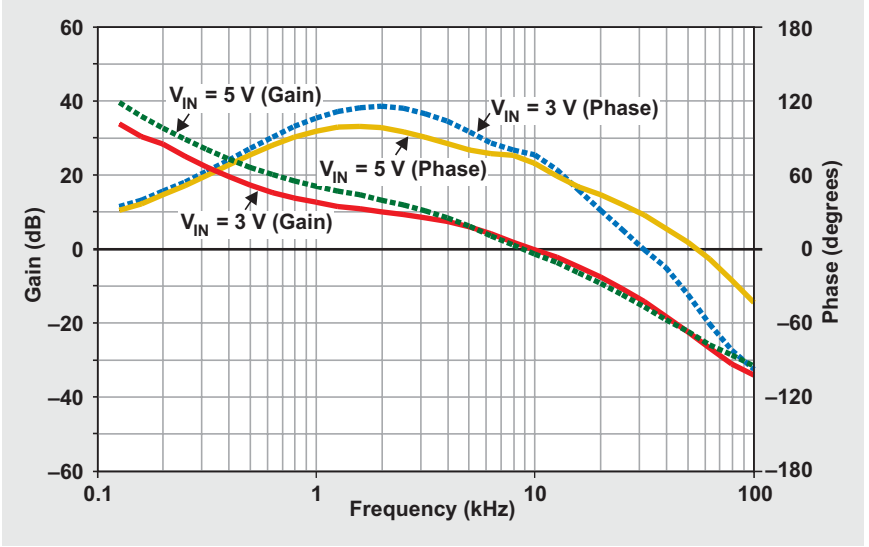
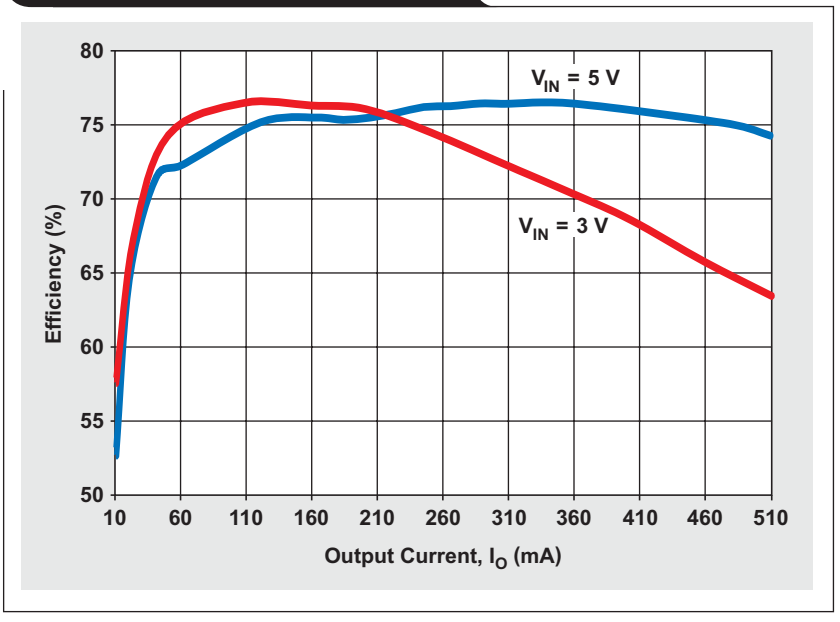


Figure 2 shows Bode plots of the feedback loop at full rated load for input voltages of 3 and 5 V. The response

Figure 3. Efficiency with a 5-V input



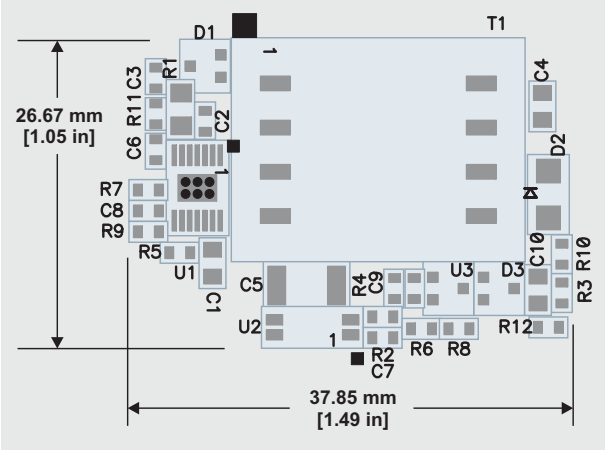
was measured by breaking the loop and injecting a disturbance at R10. In the power stage, the load resistance and output capacitance form a pole at 700 Hz. This pole is compensated for by the zero of the TL431 circuit, formed by the values of C9 and R6. An additional zero was added at 30 kHz by placing C7 in parallel with R2. This zero helps negate the limited bandwidth of the optocoupler and increases the phase margin.

The efficiency of this design is shown in Figure 3. With a typical ON resistance of 130 mΩ, the internal MOSFET contributes around 850 mW of conduction losses with a 5-V input. The output diode dissipates approximately 200 mW. The remaining loss can be attributed to switching losses, bias loss in the TPS61175 and TL431, and losses in the snubber.

This simple design can be placed in a small amount of board space. Figure 4 shows the parts placement for this design on a single-sided PWB. The design consumes a total of 1.5 in^2 on one side of the board.

This simple and compact design demonstrates how integrated boost converters, usually relegated to portable applications, can be leveraged in isolated auxiliary supplies. This example showed how to use the TPS61175 with a low input voltage. With a 40-V rating on the drain of the internal FET, and a maximum input-voltage rating of 18 V, this design could be adjusted to work with a 12-V input, with an internally set peak-current limit of 3 A.

Figure 4. Typical PWB layout



Related Web sites

power.ti.com
www.ti.com/sc/device/TPS61175
www.ti.com/sc/device/TL431

RS-485: Passive failsafe for an idle bus

By Thomas Kugelstadt
Senior Applications Engineer

Despite the integrated failsafe features of modern RS-485 transceivers, many applications use legacy parts lacking these features. Knowing how to provide failsafe operation, particularly during an idle-bus condition, therefore ranks at the top of the list of customer inquiries to interface-application groups worldwide. This article shows how to apply failsafe biasing for idle buses externally and also suggests low-cost solutions that integrate this feature.

Failsafe operation

RS-485 specifies that the receiver output state should be logic high for differential input voltages of $V_{AB} \geq +200$ mV and logic low for $V_{AB} \leq -200$ mV. For input voltages in between these limits, a receiver's output state is not defined and can randomly assume high or low.

Removing the uncertainty of random output states, modern transceiver designs include internal biasing circuits that put the receiver output into a defined state (typically high) in the absence of a valid input signal.

There are three possible scenarios that can cause the loss of an input signal:

- an open circuit caused by a wire break or the unintentional disconnection of a transceiver from the bus;
- a short circuit due to an insulation fault, connecting both conductors of a differential pair to one another; or
- an idle bus when none of the bus transceivers are active. (This particular condition is not a fault but occurs regularly when bus control is handed over from one driver to another to avoid bus contention.)

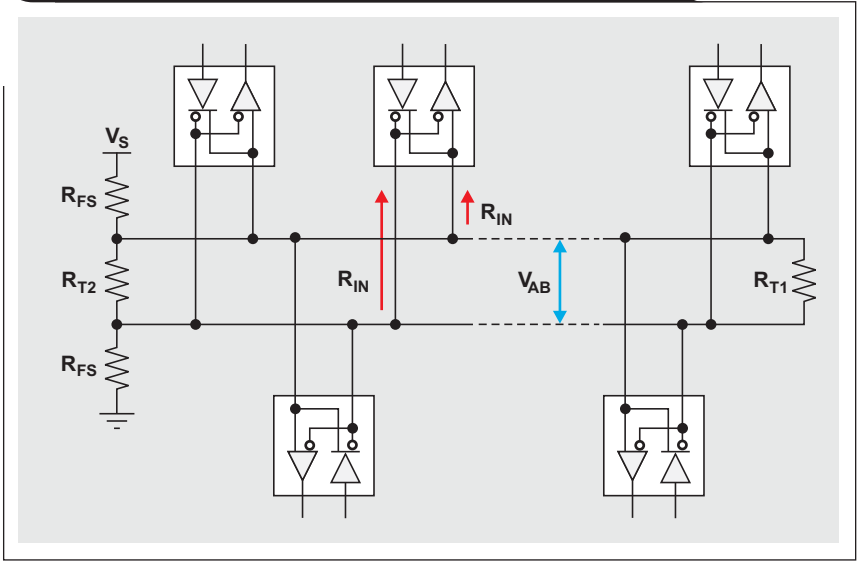
While modern transceiver designs provide failsafe operation for all three categories, legacy designs don't. For these components it is necessary to provide external resistor biasing to ensure failsafe operation during an idle bus.

External idle-bus failsafe biasing

Figure 1 shows an RS-485 bus with its distributed network nodes. If none of the drivers connected to the bus are active, the differential voltage (V_{AB}) approaches zero, thus allowing the receivers to assume random output states.

To force the receiver outputs into a defined state, failsafe biasing resistors, R_{FS}, are introduced that, through voltage-divider action with the terminating resistors, R_{T1} and R_{T2}, must provide sufficient differential voltage to exceed the input-voltage threshold, V_{IT}, of the receiver.

Figure 1. RS-485 network with failsafe bias resistors



For clarity, Figure 2 shows the equivalent circuit of the RS-485 bus with the failsafe biasing resistors, R_{FS}, the terminating resistors, R_{T1} and R_{T2}, and the equivalent input resistance, R_{INEQ}, lumped together to represent the common-mode input resistance of all transceivers connected to the bus.

To find an equation that allows us to calculate the R_{FS} values, we determine the node currents in A and B (Figure 2) and solve for the respective line voltages, V_A and V_B.

Node A:

$$\frac{V_S - V_A}{R_{FS}} = \frac{V_A - V_B}{R_{T2}} + \frac{V_A - V_B}{R_{T1}} + \frac{V_A}{R_{INEQ}} \rightarrow$$

$$V_A = R_{INEQ} \times \left[\frac{V_S - V_A}{R_{FS}} - \left(V_A - V_B \right) \times \left(\frac{1}{R_{T1}} + \frac{1}{R_{T2}} \right) \right]$$

Node B:

$$\frac{V_A - V_B}{R_{T2}} + \frac{V_A - V_B}{R_{T1}} = \frac{V_B}{R_{FS}} + \frac{V_B}{R_{INEQ}} \rightarrow$$

$$V_B = R_{INEQ} \times \left[\left(V_A - V_B \right) \times \left(\frac{1}{R_{T1}} + \frac{1}{R_{T2}} \right) - \frac{V_B}{R_{INEQ}} \right]$$

Establishing the difference between both line voltages yields the differential input voltage,

$$V_{AB} = \frac{V_S}{R_{FS}} \times \frac{1}{\frac{1}{R_{INEQ}} + \frac{1}{R_{FS}} + 2\left(\frac{1}{R_{T1}} + \frac{1}{R_{T2}} \right)}. \quad \textbf{(1)}$$

The value of R_{FS} is subject to a number of system and standard constraints:

- The RS-485 standard specifies a maximum common-mode loading (or minimum common-mode resistance) of R_{CM} = 375 Ω. Because the failsafe bias resistors present a common-mode load to both the A and B wires, the parallel combination of R_{FS} and R_{INEQ} must be greater than or equal to 375 Ω, which is expressed as

$$R_{FS} \parallel R_{INEQ} = R_{CM}, \text{ or } \frac{1}{R_{INEQ}} + \frac{1}{R_{FS}} = \frac{1}{375\ \Omega}. \quad \textbf{(2)}$$

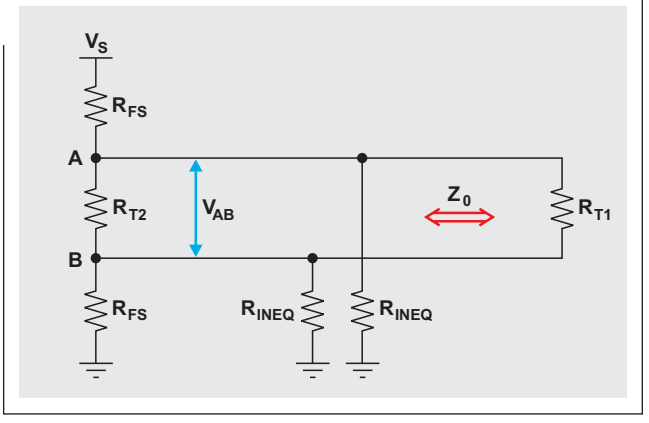
- The cable end without the biasing network is usually terminated with the resistor R_{T1}, whose value matches the line impedance. For RS-485, this is

$$R_{T1} = 120\ \Omega, \text{ or } \frac{1}{R_{T1}} = \frac{1}{120\ \Omega}. \quad \textbf{(3)}$$

- During normal operation, a driver output sees the series of both failsafe bias resistors in parallel to the terminating resistor R_{T2}. Thus, for line impedance matching, the parallel circuit of R_{T2} and $2R_{FS}$ should equal Z_0:

$$R_{T2} \parallel 2R_{FS} = Z_0, \text{ or } \frac{1}{R_{T2}} = \frac{1}{120\ \Omega} - \frac{1}{2R_{FS}}. \quad \textbf{(4)}$$

Figure 2. Equivalent circuit with transceiver resistances lumped together



Inserting Equations 2, 3, and 4 into Equation 1 simplifies the expression for V_{AB} to

$$V_{AB} = \frac{V_S}{0.036 \times R_{FS} - 1}. \quad \textbf{(5)}$$

Solving for R_{FS} yields

$$R_{FS} = \left(\frac{V_S}{V_{AB}} + 1 \right) \times 27.8\ \Omega. \quad \textbf{(6)}$$

Note that Equation 6 is a generic form for calculating the bias resistor value, with the constant of 27.8 Ω representing the common-mode loading and line-matching constraints of an RS-485 system.

Because idle-bus failsafe must work under worst-case conditions, the values of the bias resistors must be calculated for minimum supply voltage at maximum noise. While $V_{S(min)}$ = 4.75 V for a standard 5-V supply with ±5% tolerance, the maximum noise is usually subject to measurement. For a well-balanced system, however, we can assume a differential noise of less than 50 mV, so that the sum of receiver input threshold and noise yields a differential input voltage of

$$V_{AB} = V_{IT} + V_{Noise} = 200\ \text{mV} + 50\ \text{mV} = 250\ \text{mV}.$$

Calculating R_{FS} under these conditions provides a theoretical value of

$$R_{FS} = \left(\frac{4.75\ \text{V}}{0.25\ \text{V}} + 1 \right) \times 27.8\ \Omega = 556\ \Omega.$$

Choosing the next lowest value of 549 Ω from the E-96 series allows for a slightly higher voltage drop across R_{T2}.

With R_{FS} in place, we can now determine R_{T2} using the reciprocal of Equation 4 and the actual value of R_{FS} = 549 Ω:

$$R_{T2} = \frac{1}{\frac{1}{120\ \Omega} - \frac{1}{2R_{FS}}} = \frac{1}{\frac{1}{120\ \Omega} - \frac{1}{2 \times 549\ \Omega}} = 134\ \Omega$$

Choosing the closest E-96 value makes R_{T2} = 133 Ω and the differential impedance of $R_{T1} \parallel R_{T2} \parallel 2R_{FS}$ = 59.7 Ω.

As mentioned earlier, failsafe biasing presents an additional common-mode load to both the A and B wires. To stay below the specified common-mode load of 375 Ω, it is necessary to determine the maximum number of transceivers that can be connected to the bus. For this purpose we solve Equation 2 for R_{INEQ}:

$$R_{INEQ} = \frac{1}{\frac{1}{R_{CM}} - \frac{1}{R_{FS}}} = \frac{1}{\frac{1}{375\ \Omega} - \frac{1}{549\ \Omega}} = 1.183\ k\Omega$$

The maximum number of transceivers, n_{max}, is determined by dividing the rated number of unit loads (UL) by the value of R_{INEQ}:

$$n_{max} = \frac{UL}{R_{INEQ}} = \frac{12\ k\Omega}{1.183\ k\Omega} = 10.14$$

This result indicates that a maximum of 10 standard unit-load transceivers, 10 × UL, which is equivalent to 20 × ½ UL, 40 × ¼ UL, or 80 × ⅛ UL, can be connected to the bus. The final circuit with the actual resistor values is shown in Figure 3.

Conclusion

While the calculation of a failsafe-biased network for legacy transceivers is straightforward, the use of modern RS-485 transceivers such as the SN65HVD308xE family from Texas Instruments eliminates external failsafe biasing. These low-cost devices provide integrated failsafe biasing for open-circuit, short-circuit, and idle-bus conditions as well as a rating of ⅛ UL, thus increasing the possible number of transceivers that can be connected to a bus to 256.

Reference

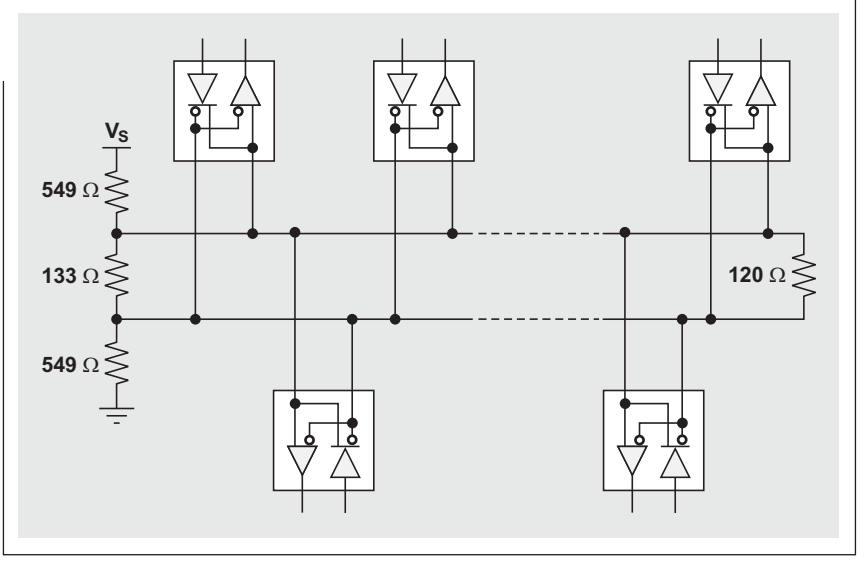
For more information related to this article, you can download an Acrobat Reader file at www-s.ti.com/sc/techlit/*litnumber* and replace "*litnumber*" with the **TI Lit. #** for the materials listed below.

Document Title	**TI Lit. #**
1. "Interface Circuits for TIA/EIA-485 (RS-485)," Application Report.	slla036d

Related Web sites

interface.ti.com
www.ti.com/sc/device/SN65HVD3080E

Figure 3. Final RS-485 network with actual resistor values



Message priority inversion on a CAN bus

By Steve Corrigan
New Product Definition

This article examines the problems encountered during data transmission when multiple dominant bits are simultaneously placed on a bus by more than one node during arbitration or an ACK bit. CAN buses are often constructed with many nodes placed physically close together. When these "clumps" of nodes are spaced a long distance from other nodes on the bus, random data errors can occur. A "message priority inversion" error causes a high-priority message to receive low-priority placement after arbitration. Uneven node spacing can also affect the ACK procedure in a CAN message. If a message is not properly acknowledged because of interruptions from reflected waves, an error is generated with each occurrence until the controller reaches an error limit that is internally set by the CAN protocol. The controller places itself in a bus-off state when this internal limit is reached so that a single node cannot block all communication on the bus. These errors are not easily uncovered by a system designer.

Minimum distance between nodes on a CAN bus

The ISO 11898-2:2003 CAN bus is a distributed-parameter circuit whose electrical characteristics are primarily defined by the distributed inductance and capacitance* along the physical media. The media are defined as the interconnecting cable or the conducting paths, connectors, terminators, and CAN transceivers added along the bus.

The following analysis examines a trade-off between the amount of node capacitance that can be added and the amount of node spacing that can be used on a bus without compromising signal integrity. For a good approximation, the characteristic transmission-line impedance looking into an arbitrary end point in an unloaded CAN bus is defined by $Z = \sqrt{L/C}$, where L is the inductance per unit length and C is the capacitance per unit length. When capacitance is added to the bus in the form of devices and their interconnection, the bus impedance is lowered to Z'. When bus impedance is lowered, an impedance mismatch occurs between unloaded and loaded sections of the bus.

The worst case occurs during an arbitration or an ACK bit when multiple dominant bits are simultaneously sent from two or more nodes. In the equivalent bus circuit shown in Figure 1, when S1 switches at time zero from a dominant state to a recessive state, the differential output voltage, V_S, of the CAN driver moves from a dominant state to a steady-state, 0-V, recessive differential signal on the bus. When this signal wave propagates down the line and arrives at the loaded section of the bus, the mismatch in impedance reflects the voltage back towards the source.

*All capacitances are differential in this article. The differential is approximately one-half of the single-ended capacitance.

Figure 1. Imbalanced CAN-bus equivalent circuit

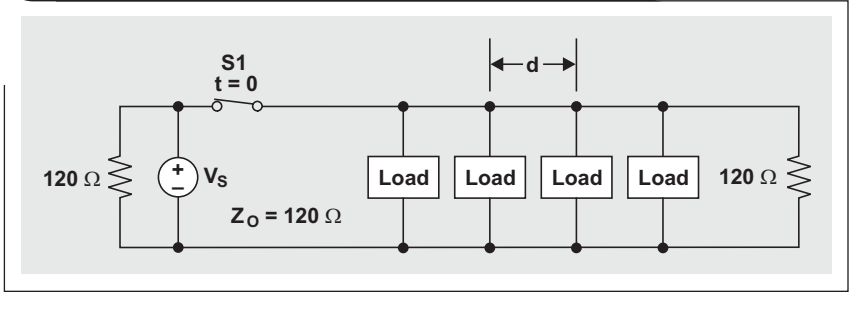
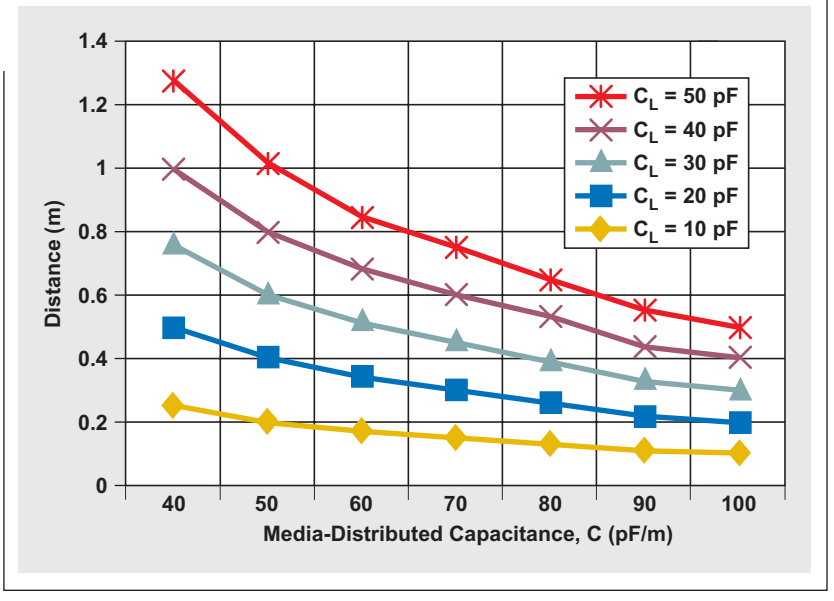


Figure 2. Minimum distance required between CAN nodes



The minimum safe distance between nodes, d, is a function of the device lumped-load capacitance, C_L, and the cable's distributed capacitance per unit length, C, where $d > C_L/0.98\ C$ meters (if C is in pF/m) or feet (if C is in pF/ft). Figure 2 displays this relationship graphically. For a complete development of this equation, please see Reference 1.

Load capacitance includes contributions from a CAN transceiver's bus pins, connector contacts, printed-circuit-board traces, protection devices, and any other physical connections as long as the distance from the bus to the transceiver is kept electrically short.

3.3-V CAN transceivers such as the Texas Instruments SN65HVD233 have about 16 pF of differential capacitance. Board traces add about 0.5 to 0.8 pF/cm, depending upon their construction. The capacitance of connectors and suppression devices can vary widely, and media-distributed capacitance ranges from about 35 pF/m for low-capacitance, shielded, twisted-pair cable to 70 pF/m for backplanes.

As a demonstration of how multiple dominant bits on the same bus affect data-transfer waveforms, ten SN65HVD233 CAN transceivers were connected to a bus with 12.7 cm of 120-Ω twisted-pair cable between each node (see Figure 3). The last node of the group was terminated with a 120-Ω termination resistor, and the first node was connected through an additional 200 m of Belden 3105A twisted-pair cable to another node and terminated.

Figure 3. Example of a capacitive load

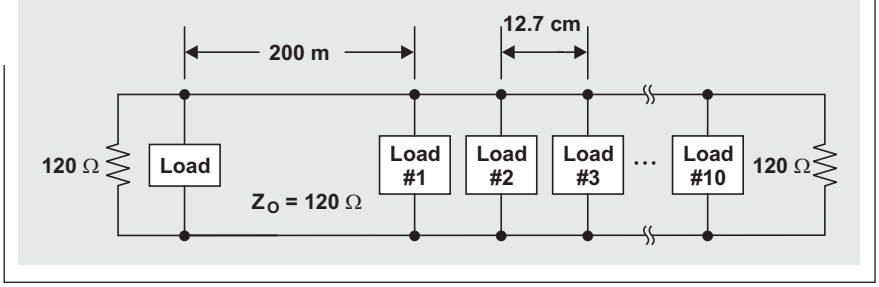


Figure 4 shows the receiving waveform of the 250-kbps data being transmitted onto the bus from the single-node load to the capacitive clump of nodes across the 200-m cable. Figure 5 shows the same waveform when more than one node sends a dominant bit onto the bus during an arbitration. Note the change in magnitude of the waveform. The propagation delay of 5 ns/m for 200 m is 1000 ns, or 1 µs, and is clearly evident. The negatively charged waveform is reflected back and attenuates the back of the waveform at the receiving clump of nodes. Figure 6 presents a higher resolution of this reflection.

Figure 6 is a good example of the possible arbitration bit-error problem, since the waveform voltage that is due to the negative reflection reduces the differential voltage of the signal to below the 900-mV dominant-bit threshold. Note that this is a single point-to-point bus connection and that any variation such as adding a drop-line to this configuration would serve only to exacerbate the problem. Also, if the signaling rate were increased to 500 kbps, this reflection would last for 50% of the waveform's 2-µs duration.

The lumped-load capacitance, C_L, of each CAN transceiver, board trace, and Berg connector amounts to approximately 20 pF per node in this example; and the distributed capacitance per unit length, C, is about 40 pF/m. The node-spacing calculation results presented in Figure 2 (C_L = 20 pF and C = 40 pF/m) indicate that 0.5 m of cable between each of the clumped nodes in place of the 12.7-cm cable will correct the problem (see Figure 7). Clearly, the calculations prove to be correct. The reflected wave has almost completely disappeared, and the added twisted-pair cable is a small price to pay for a reliable solution.

Figure 4. Normal data traffic on a CAN bus

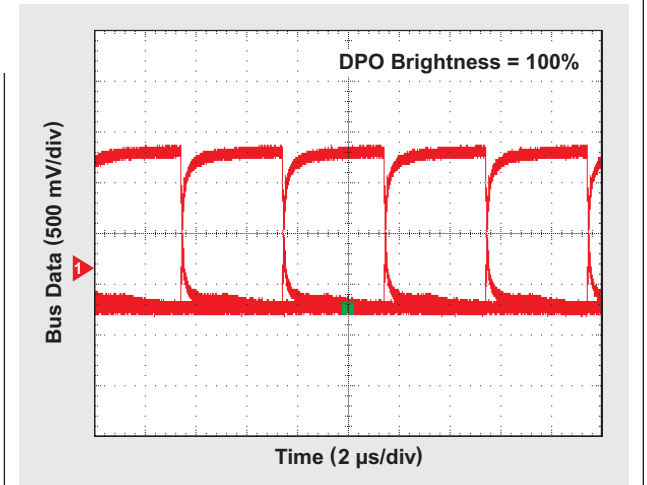


Figure 5. Distortion from multiple dominant bits on the same bus during arbitration

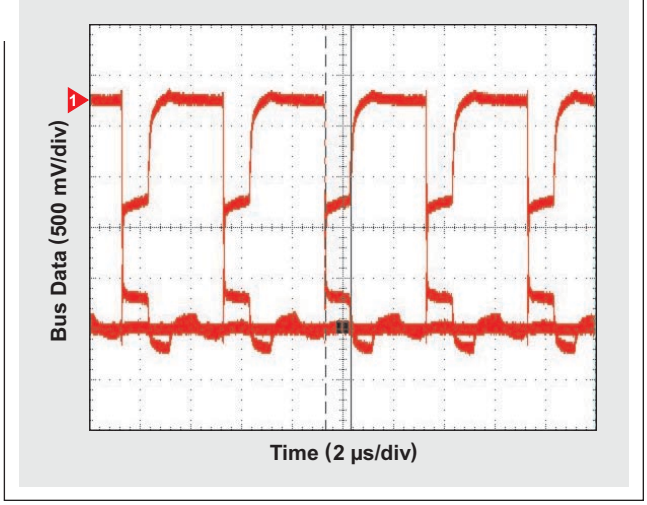


Figure 6. Reflected-wave distortion by multiple dominant bits

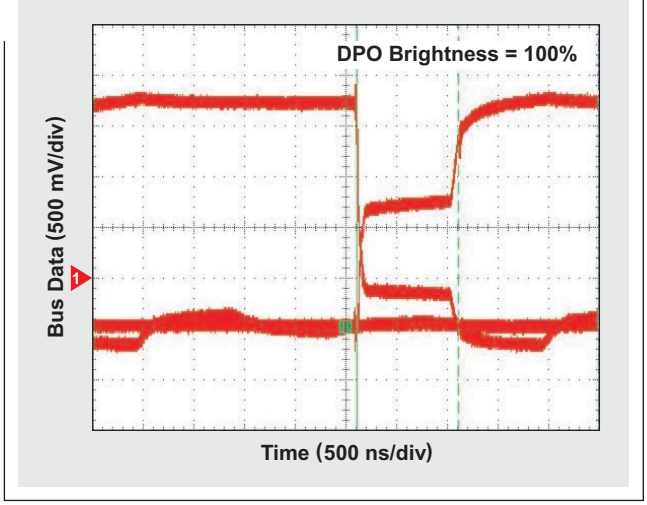
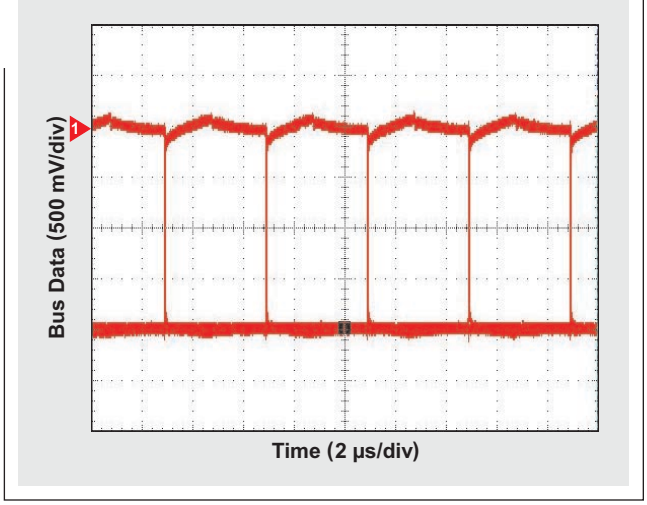


Figure 7. Addition of 0.5 m to bus length



Conclusion

A CAN bus that has not been optimized to minimize reflected energy at each node can cause a host of network problems. Even when data transfer seems to be working normally, dominant-bit collisions that occur randomly during arbitration or by design during an ACK bit may create sufficient signal reflections to cause priority inversion and delays from acknowledgment errors. Of course, more pronounced reflections can cause excessive bus delays due to bit-stuffing errors and normal data errors. These reflections can usually be controlled by optimizing the spacing between nodes according to established data-transmission practices.

Reference

For more information related to this article, you can download an Acrobat Reader file at www-s.ti.com/sc/techlit/*litnumber* and replace "*litnumber*" with the **TI Lit. #** for the materials listed below.

Document Title	**TI Lit. #**
1. Steve Corrigan, "Controller Area Network Physical Layer Requirements," Application Report	slla270

Related Web sites

interface.ti.com
www.ti.com/sc/device/SN65HVD233

Output impedance matching with fully differential operational amplifiers

By Jim Karki
Member, Technical Staff, High-Performance Analog

Introduction

Impedance matching is widely used in the transmission of signals in many end applications across the industrial, communications, video, medical, test, measurement, and military markets. Impedance matching is important to reduce reflections and preserve signal integrity. Proper termination results in greater signal integrity with higher throughput of data and fewer errors. Different methods have been employed; the most commonly used are source termination, load termination, and double termination. Double termination is generally recognized as the best method to reduce reflections, while source and load termination have advantages in increased signal swing. With source and load termination, either the source or the load (not both) is terminated with the characteristic impedance of the transmission line. With double termination, both are terminated with this characteristic impedance. No matter what impedance-matching method the designer chooses, the termination impedance to implement must be accurately calculated.

Fully differential operational amplifiers (FDAs) can provide a broadband, DC-coupled amplifier for balanced differential signals. They also have a unique ability to convert broadband, DC-coupled single-ended signals into balanced differential signals.

A common method to provide output impedance matching is to place resistors equal to the desired impedance in series with the amplifier's output. With double termination, this has the drawback that the signal level delivered to the line is reduced by –6 dB (or half) from the signal at the amplifier's output.

Synthetic impedance matching allows lower-value resistors to be used in conjunction with positive feedback around the amplifier. The benefit of doing this is that the output attenuation is reduced. This increases efficiency by lowering the loss and allows support of higher-amplitude signals on the line than can be achieved with standard termination.

Using standard series matching resistors to analyze the output impedance of FDAs is very easy, but synthetic impedance matching is more complex. So we will first look at the output impedance using only series matching resistors, and then use that as a starting point to consider the more complex synthetic impedance matching.

The fundamentals of FDA operation are presented in Reference 1. Since the principles and terminology presented there will be used throughout this article, please see Reference 1 for definitions and derivations.

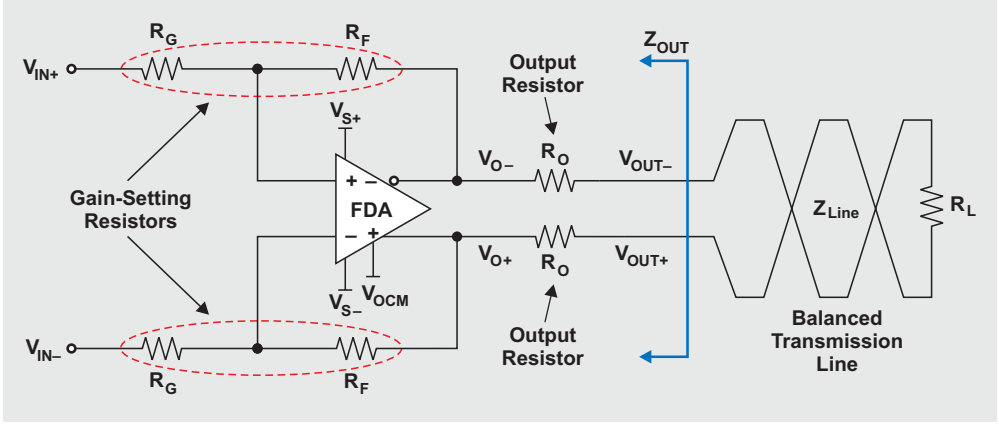
Standard output impedance

An FDA works using negative feedback around the main loop of the amplifier, which tends to drive the impedance at the output terminals, V_{O-} and V_{O+}, to zero, depending on the loop gain. An FDA with equal-value resistors in each output to provide differential output termination is shown in Figure 1. As long as the loop gain is very high, the output impedance, Z_{OUT}, in this circuit is approximately equal to $2 \times R_O$.

Parameter definitions for Figure 1 are as follows:

- R_F and R_G are the gain-setting resistors for the amplifier.
- R_L is the impedance of the load, which should be balanced and, for double termination, equal to Z_{Line}.
- R_O is the output resistor.
- $V_{O\pm}$ is the output terminal.
- V_{OCM} is the output common mode of the FDA.
- $V_{OUT\pm}$ is the differential output signal.
- $V_{S\pm}$ is the power supply to the amplifier.
- Z_{Line} is the characteristic impedance of the balanced transmission line from the amplifier to the load.

Figure 1. FDA with differential resistors for output termination



For analysis, it is convenient to assume that the FDA is an ideal amplifier with no offset and has infinite gain. Each output of the amplifier can be viewed as a voltage source with an output impedance of r_O. With high loop gain, both r_O and the differential output impedance, Z, of the FDA will be very small; for instance, the output impedance of the Texas Instruments (TI) THS4509 is less than 1 Ω at frequencies below 40 MHz. For output-impedance analysis, the inputs are grounded so that $V_{IN\pm} = 0$ V, resulting in $V_{O\pm} = V_{OCM}$. Since we are interested in only the AC response, and since V_{OCM} is a DC voltage, $V_{O\pm}$ is set to 0 V. The differential output impedance can be determined from Figure 2: $Z_{OUT} = 2(r_O + R_O)$; and, since as r_O is nearly 0 Ω, $Z_{OUT} \approx 2 \times R_O$.

For an example of how to select the value of R_O, let's look at driving a twisted pair differentially from the FDA. A value of $Z_{Line} = 100$ Ω is common for twisted-pair cables. For double termination, the source needs to provide $R_O = 50$ Ω on each side for a 100-Ω differential output impedance, and the line needs to be terminated with $R_L = 100$ Ω. It is assumed that the output impedance of the FDA is approximately 0 Ω, so 49.9-Ω resistors are placed in each series with each output.

In a terminated system, it is common practice to take the gain of the amplifier stage from the source to the load, or from $V_{IN\pm}$ to $V_{OUT\pm}$; so gain is given by

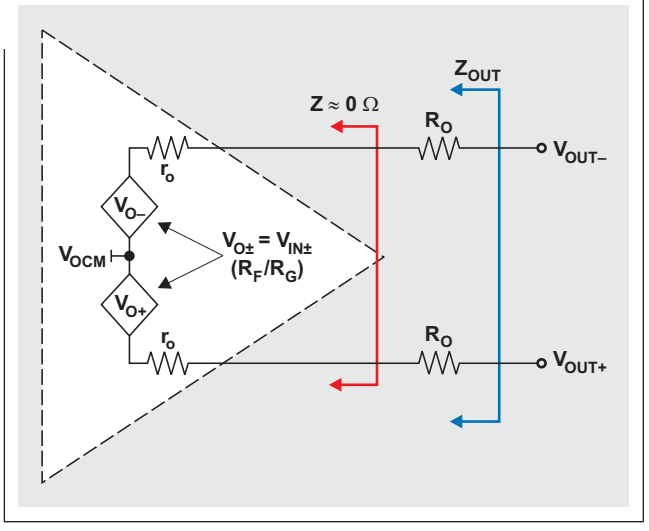
$$\frac{V_{IN\pm}}{V_{OUT\pm}} = \frac{R_L}{R_L + 2R_O} \times \frac{R_F}{R_G}. \quad (1)$$

Assuming that the output impedance matches the load impedance,

$$\frac{V_{IN\pm}}{V_{OUT\pm}} = \frac{1}{2} \times \frac{R_F}{R_G}. \quad (2)$$

It is recommended that R_F be kept to a range of values for the best performance. Too large a resistance will add excessive noise and will possibly interact with parasitic board capacitance to reduce the bandwidth of the amplifier; and too low a resistance will load the output, causing increased distortion. For example, the THS4509 performs best with R_F in the range of 300 to 500 Ω. In the design process, the designer first selects the value of R_F, then calculates R_O and R_G to match the desired gain. The value of Z_{OUT} is then calculated as $2 \times R_O$.

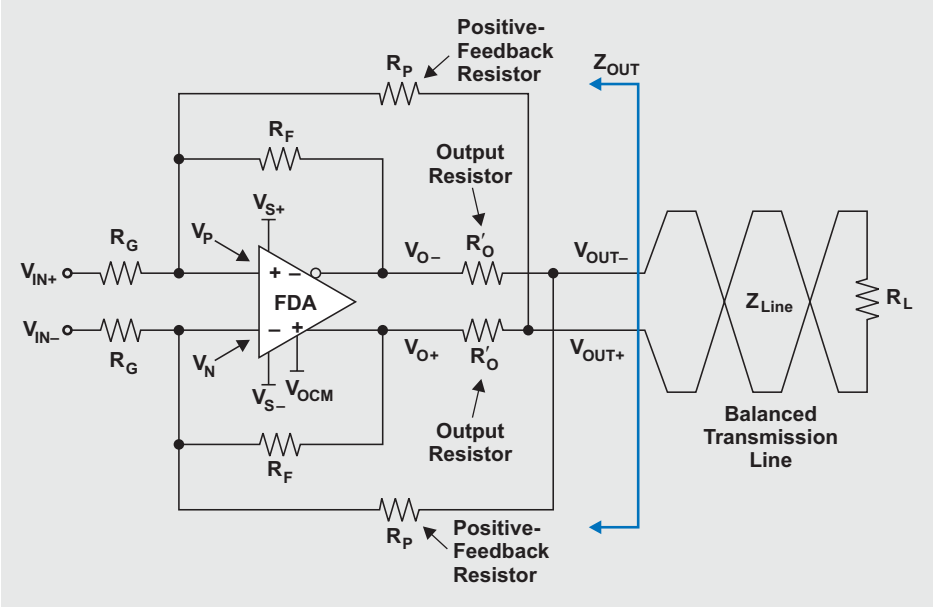
Figure 2. FDA circuit for analysis of balanced output impedance



Synthesized output impedance

In Figure 3, the positive-feedback resistors, R_P, are added from V_{OUT+} to V_P and from V_{OUT-} to V_N. Given a balanced differential system, these resistors provide positive feedback around the amplifier that makes R'_O look larger from the line than the actual value, R_O. The amount of positive feedback used determines the scaling and has an effect on the forward gain of the amplifier.

Figure 3. FDA differential output impedance with synthesized resistors

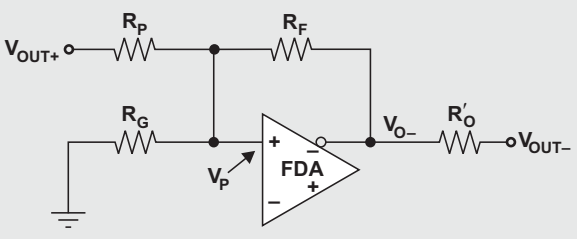


It is convenient to first look at half of this circuit (see Figure 4) to analyze the response of the amplifier to a signal that was applied from the line because resistors R_P were added. To determine the output impedance of the amplifier as seen from the transmission line, a signal is injected at V_{OUT-} with the input at V_{IN+} grounded. The signal from the other side of the line at V_{OUT+} is seen as an input signal to the amplifier, with gain to V_{O-} set by R_F/R_P. Note that the output pins will have a common-mode voltage set by V_{OCM}, which is assumed to be a DC voltage and is set to 0 V for AC analysis as before.

In a balanced system it is assumed that the differential signals are symmetrical and 180° out of phase. Therefore $V_{OUT+} = -V_{OUT-}$, and

$$V_{O-} = -V_{OUT+} \times \frac{R_F}{R_P} = V_{OUT-} \times \frac{R_F}{R_P}.$$

Figure 4. Simplified view for analysis of adding R_P



Thus R_P effectively adds positive feedback to the system, resulting in an in-phase response at V_{O-} to a signal from the line. This in turn makes R'_O appear (from the line) to be a larger-value resistor than it actually is. Inclusion of the other half of the amplifier permits the differential response of the circuit to be shown as

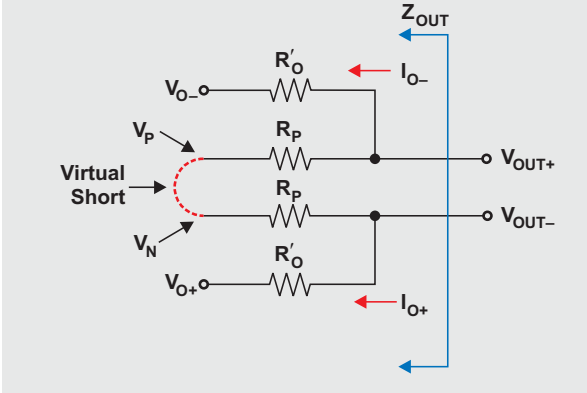
$$V_{O\pm} = V_{OUT\pm} \times \frac{R_F}{R_P}.$$

To complete the analysis, this result is used in conjunction with a virtual short* to construct a simplified view of the impedance seen from the line with this architecture; the diagram is shown in Figure 5. This figure shows that the differential output equals 2 × R_P in parallel with the effective value of $R'_O = 2(V_{OUT\pm} - V_{O\pm})/I_{O\pm}$. With the expressions for $V_{O\pm}$ from before and some algebra, an equation to calculate the output impedance of the circuit can be derived:

$$Z_{OUT} = 2 \times \left(\frac{R'_O}{1 - \frac{R_F}{R_P}} \parallel R_P \right) \qquad (3)$$

*The term "virtual short" means that while an op amp is in linear operation with negative feedback and the loop gain is high, the input terminals are driven to the same voltage and appear to be "virtually" shorted together.

Figure 5. Simplified view for analysis of impedance seen from the line



The positive feedback from adding resistors R_P affects the forward gain of the amplifier and adds another load in parallel with R_L. Accounting for this effect and the voltage divider between R'_O and $R_L \| 2R_P$, the gain from $V_{IN\pm}$ to $V_{OUT\pm}$ is given by

$$\frac{V_{OUT\pm}}{V_{IN\pm}} = \frac{R_F}{R_G} \times \frac{1}{\frac{2R'_O + R_L \parallel 2R_P}{R_L \parallel 2R_P} - \frac{R_F}{R_P}}. \qquad (4)$$

The derivation of this equation is left to the interested reader.

Design is best accomplished by first choosing the values of R_F and R'_O. Next, the required value of R_P is calculated to arrive at the desired Z_{OUT}. Then R_G is calculated for the required gain. These equations are easy to solve when set up in a spreadsheet. To see an example Excel® worksheet, click on the Attachments tab or icon on the left side of the Adobe® Reader® window. Open the file FDA_Output_Impedance_Wksht.xls, then select the Synthesized Output Resistor worksheet tab.

As an example of the design method, let's say a twisted pair is driven differentially from the THS4509 FDA with Z_{OUT} = 100 Ω, and a gain of 1.58 (4 dB) to the load is desired. Values of R_F = 402 Ω and R'_O = 25 Ω are chosen. R_P can then be calculated by rearranging Equation 3 and substituting the chosen values:

$$R_P = \frac{R_F - R'_O}{1 - \frac{2R'_O}{Z_{OUT}}} = \frac{402 - 25}{1 - \frac{50}{100}} = 754.0\ \Omega$$

The nearest standard value, 750 Ω, should be used.

R_G can be found by rearranging Equation 4 and substituting the known values:

$$R_G = R_F \times \frac{1}{\frac{2R'_O + R_L \parallel 2R_P}{R_L \parallel 2R_P} - \frac{R_F}{R_P}} \times \frac{V_{IN\pm}}{V_{OUT\pm}}$$

$$= 402 \times \frac{1}{\frac{50 + 100 \parallel 1500}{100 \parallel 1500} - \frac{402}{750}} \times 1.58 = 255.1\ \Omega.$$

The nearest standard value, 255 Ω, should be used.

SPICE simulation of standard and synthesized output impedance matching

SPICE simulation is a great way to compare expected circuit performance from standard versus synthesized output impedance matching. There are numerous ways to find the output impedance in SPICE. An easy way is to drive the output from a differential source with output impedance equal to Z_{OUT} and with $V_{IN\pm}$ grounded. Then verify that half the differential source amplitude is seen at $V_{OUT\pm}$, which is expected for double termination with equal impedances.

To see a TINA-TI™ simulation circuit of the two examples given, click on the Attachments tab or icon on the left side of the Adobe Reader window. If you have the TINA-TI software installed, you can open the file FDA_Output_Impedance_Standard_vs_Synthesized_Resistors.TSC to view the examples. To download and install the free TINA-TI software, visit www.ti.com/tina-ti and click the Download button.

For clarity, the simulation circuits and expected waveforms are shown as separate circuits in Figures 6 and 7, which show that the termination is correct.

Figure 6. TINA-TI simulation of FDA output impedance with standard impedance-matching resistors

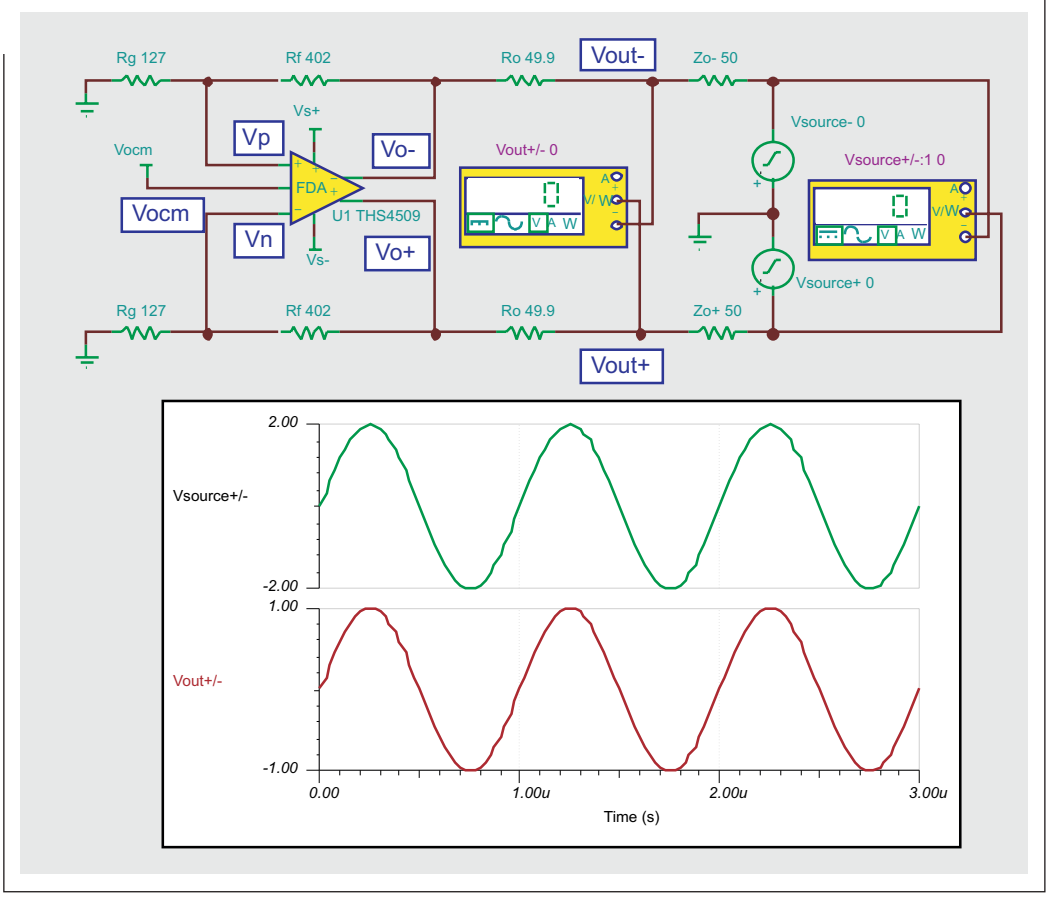


Figure 7. TINA-TI simulation of FDA output impedance with synthesized impedance-matching resistors

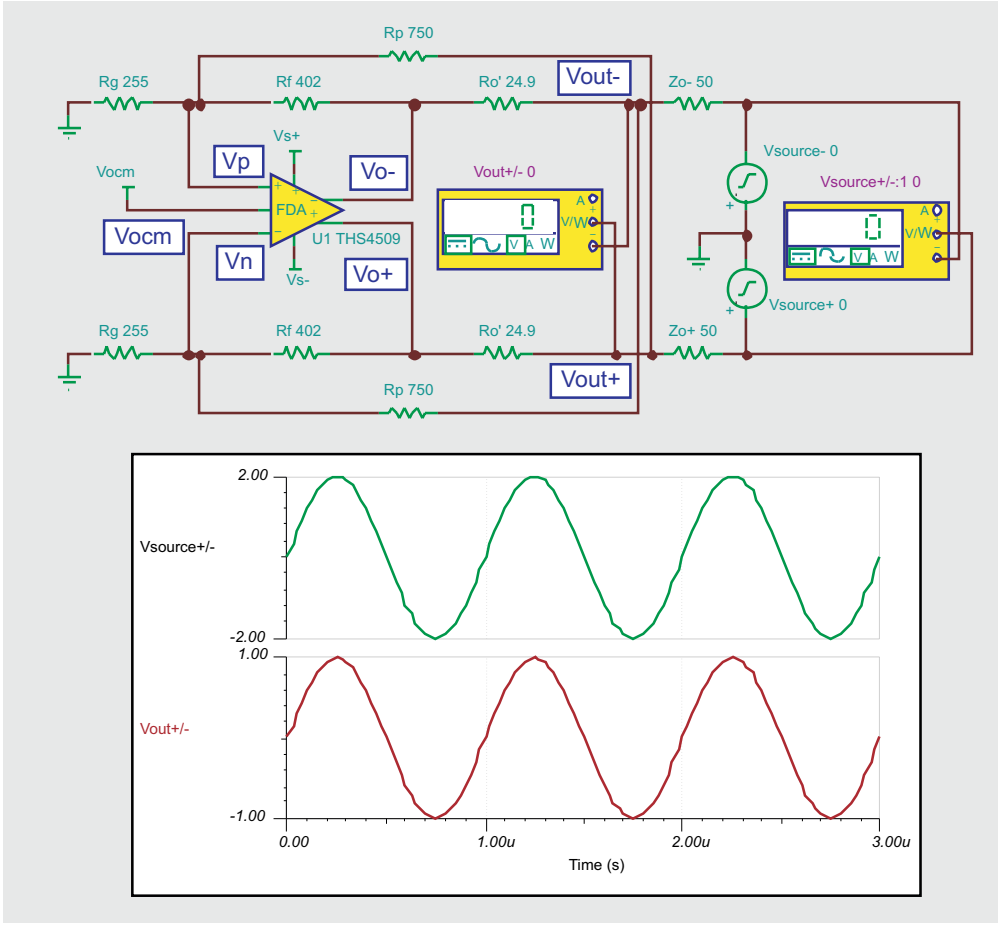


Figure 8 shows the amplifier's expected signal amplitudes at the input, at the output, and at the load for the two scenarios. To see a TINA-TI simulation circuit of the gain and signal amplitudes, click on the Attachments tab or icon on the left side of the Adobe Reader window. If you have the TINA-TI software installed, you can open the file FDA_Gain_and_Voltages_with_Synthesized_vs_Standard_Resistors.TSC to view the circuit example. To download and install the free TINA-TI software, visit www.ti.com/tina-ti and click the Download button.

Figure 8. TINA-TI simulation of FDA output voltages with standard and synthesized impedance matching

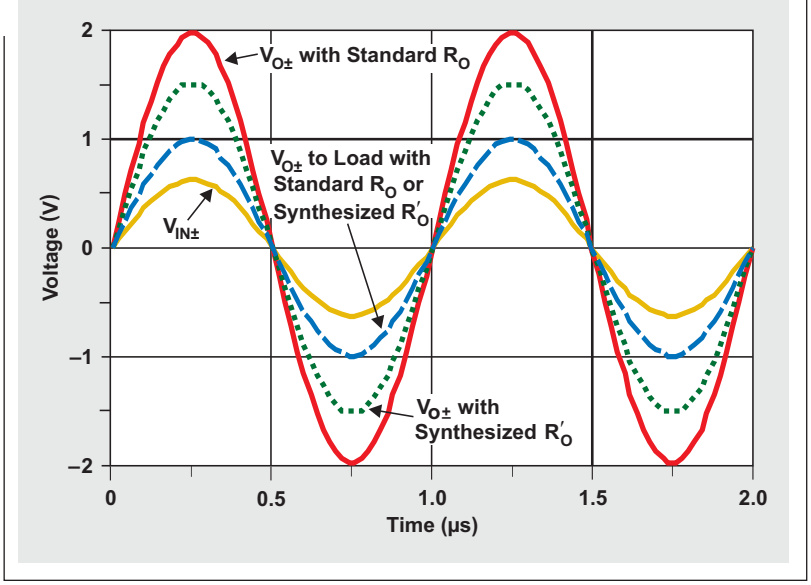
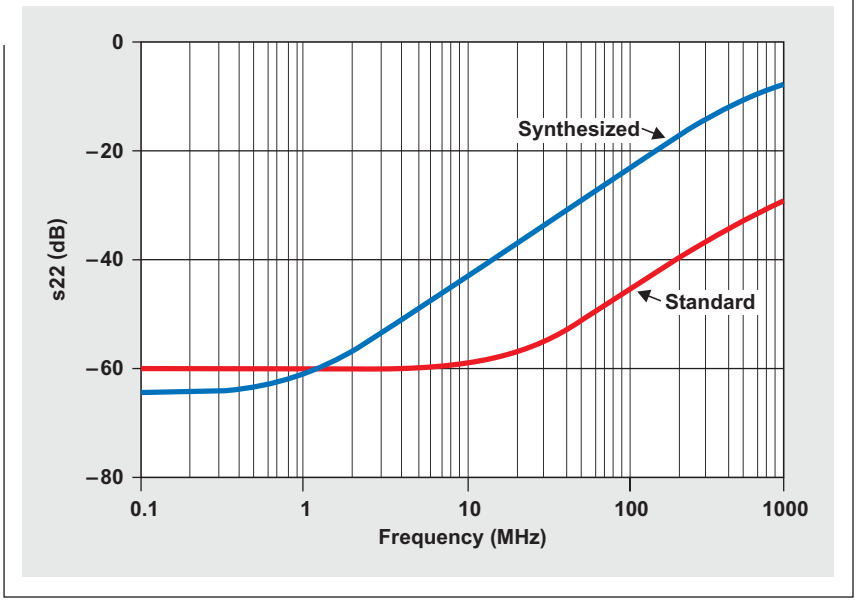


Figure 9. Simulated s22 of FDA with standard and synthesized impedance matching



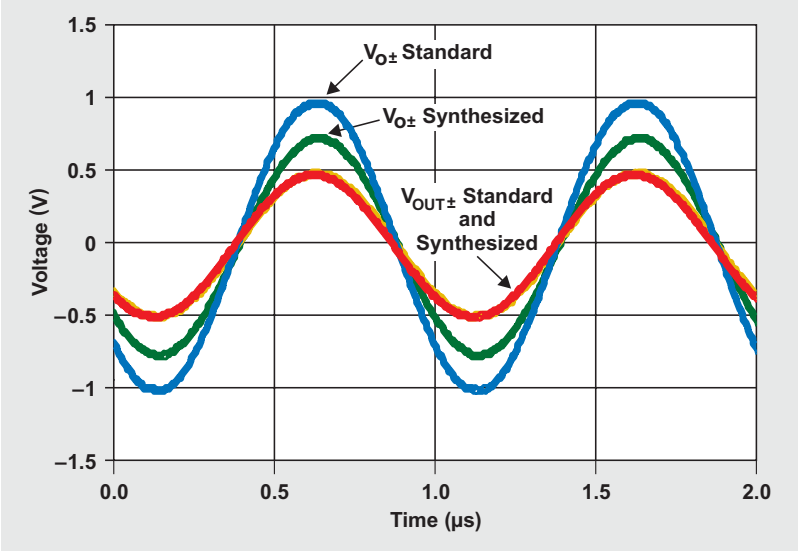
Lab testing of standard and synthesized output impedance matching

Using a network analyzer to measure the output return loss, or scattering parameter s22,** is a common way to show the performance of impedance matching in the lab. Figure 9 shows the simulated s22 of the FDA with standard and synthesized output impedance matching.

To further validate the design equations, test circuits using the THS4509 FDA were built and tested on the bench. The lab equipment used for testing had single-ended, 50-Ω inputs and outputs; so the circuits presented earlier were redesigned to match Z_{OUT} = 50 Ω. The circuits were also modified to convert the output differential signal to single-ended (and vice versa) by adding a Mini-Circuits ADT1-1WT 1:1 transformer on the output.

First, the signal swings were tested by connecting a signal generator to the input and using an oscilloscope with a 50-Ω input to look at the output waveforms. The results, shown in Figure 10, demonstrate that the performance matches the simulations.

Figure 10. Bench test of signal voltages with standard and synthesized impedance matching



** A common two-port method to show performance uses scattering parameters, or s-parameters. The standard nomenclature used is "s" followed by the incident port number and then the measurement port number. The notation "s22" means the signal is injected to the output port of the device and the reflection is measured. A lower value indicates less reflection and a better impedance match.

Next, the s22 was measured with a network analyzer to show the quality of the impedance match over frequency. The results are shown in Figure 11. The performance was limited by the transformer, which was to be expected based upon a review of the Mini-Circuits ADT1-1WT 1:1 datasheet. Up to about 40 MHz, the test showed the performance of the transformer for both the standard and synthesized impedance-matching circuits.

With standard impedance-matching resistors, the output impedance of the amplifier starts to degrade the impedance match above 40 MHz, up to the frequency limit of the transformer. With synthesized impedance-matching resistors, the impedance match shows the transformer performance up to about 200 MHz. At higher frequencies, the impedance match degrades significantly faster than with standard resistors due to the amplitude imbalance of the transformer.

Finally, the two-tone, third-order intermodulation distortion performance was tested to see if it would improve with the lower losses of synthetic impedance matching. Test signals f_1 = 70 MHz and f_2 = 71 MHz were used, along with a 2-V_{PP} envelope signal level (1 V_{PP} for each tone) delivered to the load. The test showed no significant difference between the two impedance-matching approaches for the near frequencies in third-order intermodulation terms; in fact, the results were actually better than what the datasheet shows for similar loading (see Table 1).

These results may seem contrary to expectations because lower signal amplitude is associated with better distortion performance. However, even though the impedance seen by the line looking into the amplifier with synthesized output-impedance resistors is the same as with standard resistors, the amplifier sees the actual resistance in both cases. Therefore, due to the lower-output resistors and the added parallel load of the R_P resistors, the amplifier with synthesized output impedance sees a heavier load. In this case the effects of the lower voltage and the higher load basically offset one another.

Table 1. Two-tone, third-order intermodulation distortion performance at 70 MHz

CIRCUIT	LOW-SIDE IMD3 Spur (69 MHz)	HIGH-SIDE IMD3 SPUR (71 MHz)
Standard (dBc)	–91	–88
Synthesized (dBc)	–94	–86

Note that positive feedback can lead to oscillation. When I tested the synthesized output impedance circuit, it worked as designed as long as the load was connected, but it oscillated when the load was disconnected. This is a drawback to consider if the application calls for supporting a wide load range that includes an open-circuit condition.

Reference

For more information related to this article, you can download an Acrobat Reader file at www-s.ti.com/sc/techlit/*litnumber* and replace "*litnumber*" with the **TI Lit. #** for the materials listed below.

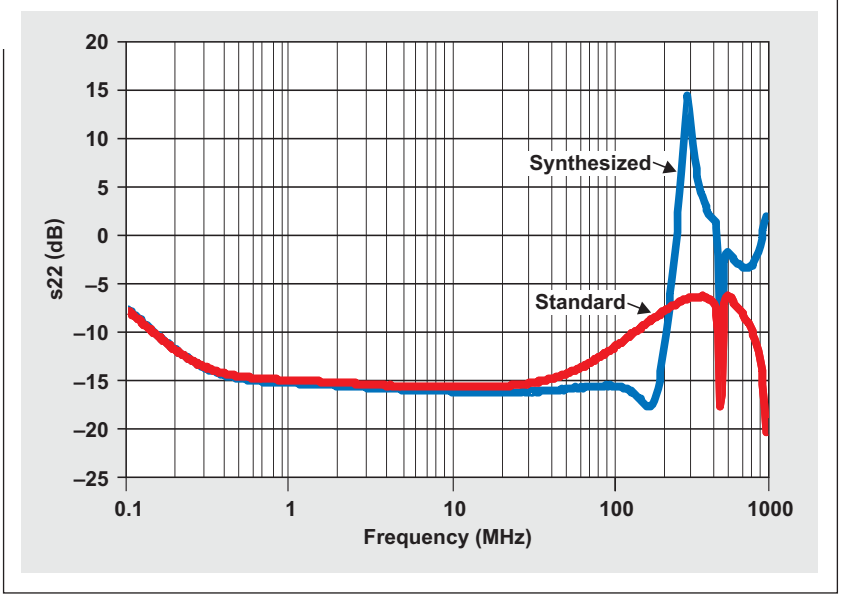
Document Title **TI Lit. #**

1. Jim Karki, "Fully Differential Amplifiers," Application Report. sloa054

Related Web sites

amplifier.ti.com
www.ti.com/sc/device/THS4509
www.ti.com/tina-ti

Figure 11. Bench test of s22 versus frequency for standard and synthesized impedance matching



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