New zero-drift amplifier has an I_Q of 17 µA

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Micropower applications require not only a very small offset and offset drift but also very low noise. Such applications include instrumentation front ends in biomedical electronics, conditioning stages in CO_2 detectors, and electronic sensor interfaces in precision metrology equipment. A front-end, low-noise amplifier combined with signal-conditioning circuits and a sensor forms a microsystem that often has to either be portable or stand alone and is therefore battery-powered. Hence, the power consumption has to be small. It is therefore crucial to eliminate the 1/f (flicker) noise and to reduce the overall noise down to the fundamental thermal noise, which is mainly determined by the allowable current consumption of the input stage.

While an auto-zero amplifier (AZA) removes its offset and 1/f noise at the cost of a raised white-noise level in the baseband, a chopper-stabilized amplifier reduces its baseband noise to the initial white-noise level but generates large output ripple instead. Because the input-stage noise is inversely proportional to its quiescent current, $e_n^2 \approx 1/I_Q$, an AZA often requires a significant increase in I_Q to achieve the desired noise levels after noise folding. Since this increase counteracts the requirements of a micropower amplifier, it is desirable to use a chopper-stabilized amplifier in micropower applications and to find some way to filter the output ripple.

This article describes a new, micropower, low-noise, chopper-stabilized operational amplifier, the OPA333, which operates from a 1.8-V supply, requiring a quiescent current of only 17 µA.

Overview

The OPA333 consists of a high-precision path (g_{m1}, g_{m2}, and g_{m3}) in parallel with a wideband path (g_{m4} and g_{m3}) (see Figure 1). The precision path ensures a high open-loop gain, A_{OL}, of 130 dB, while the wideband path provides a 350-kHz gain bandwidth at a phase margin of 60° (Figure 2). An internal, patent-pending notch filter removes chopper noise by a factor of more than 500, yielding a voltage-noise spectral density of 55 nV/√Hz across a 20-kHz bandwidth (Figure 3).

Figure 1. Internal block diagram

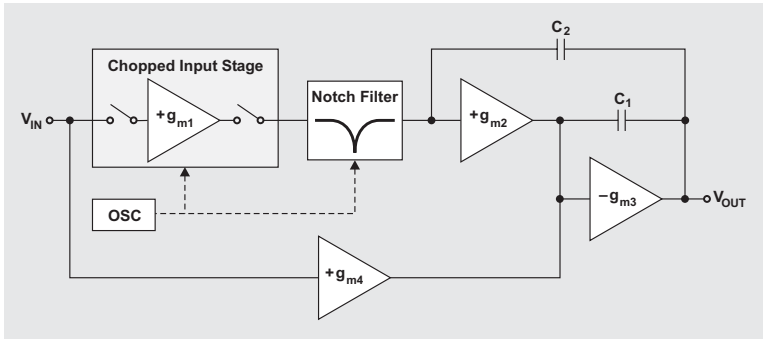


Figure 2. Open-loop gain and phase versus frequency

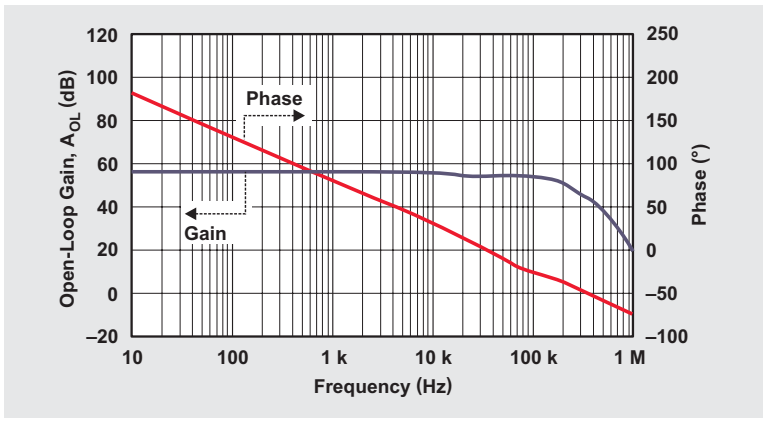
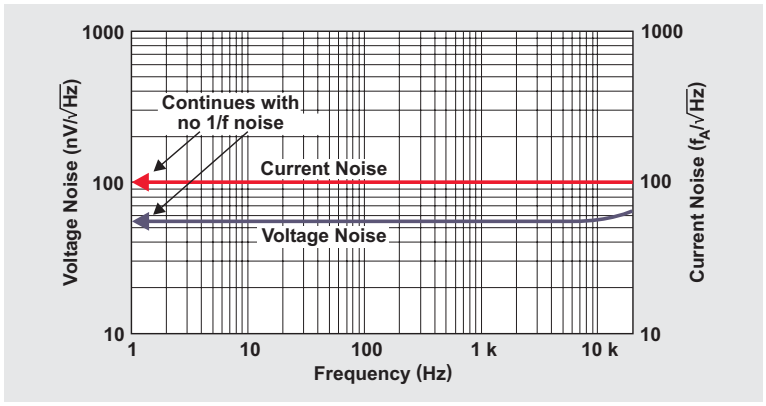


Figure 3. Noise densities versus frequency



With typical values for offset and drift of V_{OS} = 2 µV and dV_{OS}/dT = 20 nV/°C, respectively, the OPA333 also generates only 1.1 μV_{pp} of instantaneous noise in the 0.01- to 10-Hz band. The device offers rail-to-rail input and output and is available in SC70 and SOT23 packaging. Operation is specified from –40°C to 125°C.

OPA333 design rationale

The remainder of this article explains the underlying principles of the OPA333 design, describing the functional blocks and their individual contributions to the overall performance of this remarkable amplifier.

Offset cancellation of a wideband amplifier in general

Reducing the input offset voltage of a wideband amplifier, A_W, typically requires the support of an additional stabilizing or nulling amplifier, A_N, which is connected in parallel to the main amplifier (Figure 4). The stabilizing amplifier must be able to cancel its own offset, thus resembling an ideal amplifier. In addition, its open-loop gain has to be significantly larger than $A_N >> A_W$. This is usually achieved by using a multistage amplifier whose input gain is identical to A_W and whose output gain is G, with G >> 1. Note that the nulling amplifier can use chopping or auto-zeroing to null its own offset.

The output voltage of the circuit in Figure 4 is given by

$$V_{OUT} = V_W + V_N = A_W \times (G+1) \times \frac{V_{IN} + V_{OSW}}{G+1}.$$

Assuming G >> 1 and substituting $A_W G$ with A_N yields the effective open-loop gain and input offset for the amplifier model in Figure 5:

$$V_{OUT} = A_N \times \frac{V_{IN} + V_{OSW}}{G}.$$

Figure 4. Offset cancellation principle

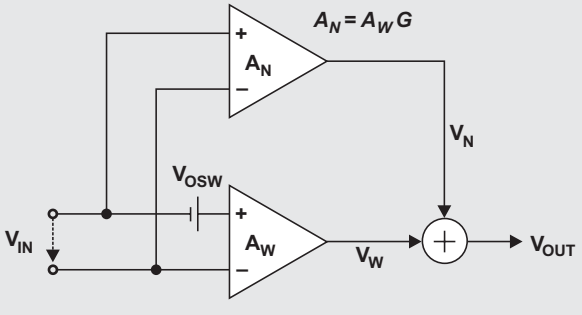
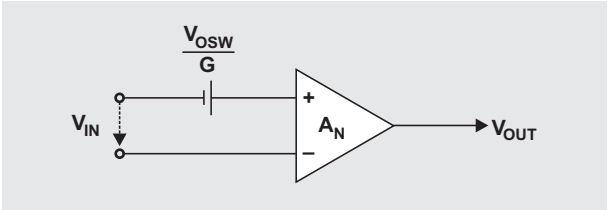


Figure 5. Effective amplifier model



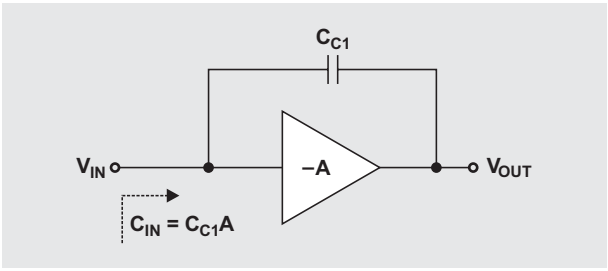
Thus, the DC gain has increased by factor G, from A_W to A_N, while the input offset of the wideband amplifier is reduced by G (typically 60 dB).

Multistage stabilizing amplifier

Large capacitance values are required to achieve low dominant pole frequencies. We recall that Miller compensation is used in op amp design to reduce these large values down to a size feasible for on-chip integration. Miller compensation relies on the effect that the input capacitance of an amplifier, C_{IN}, appears to be A times larger than the actual capacitance in the feedback loop, C_{C1}, with A being the amplifier gain (see Figure 6).

Because the precision path requires significantly higher gain than the wideband path, a three-stage cascade structure is used to provide that gain while allowing operation from very low supply voltages. If we neglect the chopper mechanism and the notch filter in Figure 1, the stabilizing

Figure 6. Miller effect: $C_{IN} = C_{C1}(A + 1)$. For A >> 1: $C_{IN} \approx C_{C1}A$.



amplifier that remains is a three-stage, nested Miller-compensated (NMC) cascade amplifier as shown in Figure 7.

Miller compensation provides the additional valuable feature of frequency-response shaping through a process known as *pole-splitting*. Figure 8 shows the frequency response of an uncompensated three-stage amplifier with its pole frequencies f_{p1}, f_{p2}, and f_{p3}. Through careful design of the g_m stages and appropriate selection of the Miller compensation capacitances, it is possible to shift f_{p1} down to a very low frequency, f_{p1}', making it the dominant pole of the precision path. At the same time, f_{p2} is pushed to higher frequencies, f_{p2}', expanding the 20-dB/dec slope and thus the range of stable operation.

In the case of a stand-alone amplifier, f_{p2} is usually located beyond the unity-gain frequency, allowing a three-stage NMC structure to achieve high bandwidth beyond 10 MHz while maintaining phase margins of up to 70°.

In the OPA333 design, however, the NMC amplifier operates in parallel with the wideband stages, g_{m4} and g_{m3}. Because this wideband forward path is responsible for providing the necessary bandwidth and phase margin of the overall amplifier, the stability requirements of the NMC amplifier are relaxed, allowing its second pole, f_{p2}, to occur before the unity-gain crossover.

Where do we apply the actual offset cancellation?

To answer this question we can, for convenience, replace the g_m stages with actual op amps, where the precision path comprising A_1 to A_3 is in parallel with the wideband path comprising A_4 and A_3 (Figure 9). For further simplification, the switching network and the notch filter have been left out, and the amplifier circuit is shown in a feedback configuration.

Figure 7. Three-stage NMC cascade amplifier

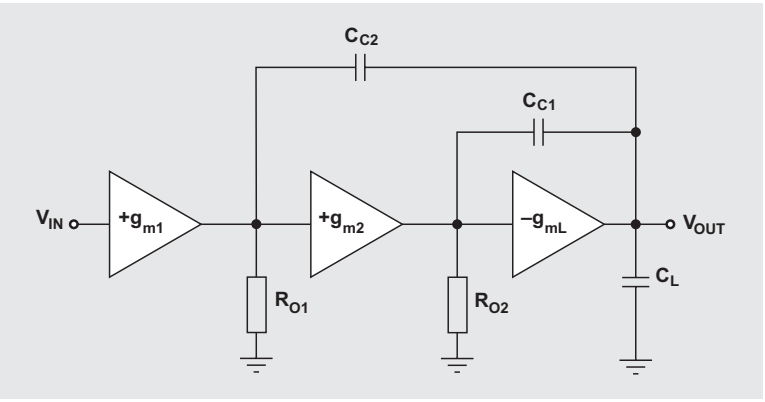


Figure 8. Pole splitting of the three-stage NMC amplifier

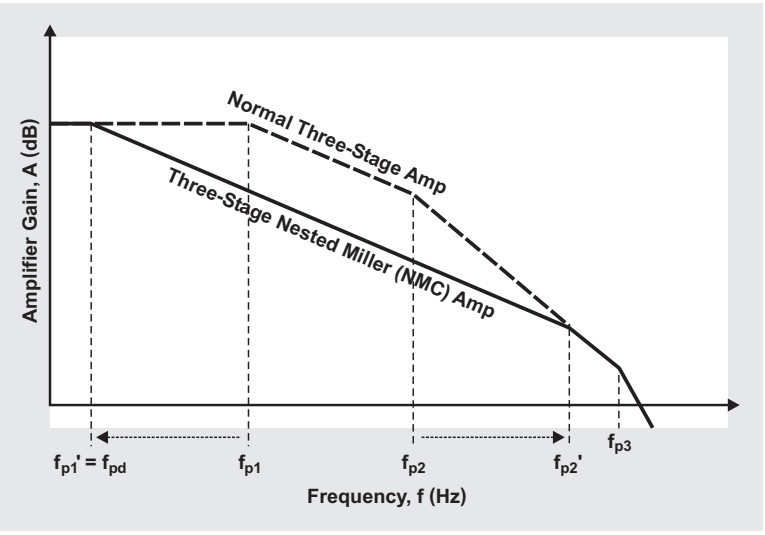
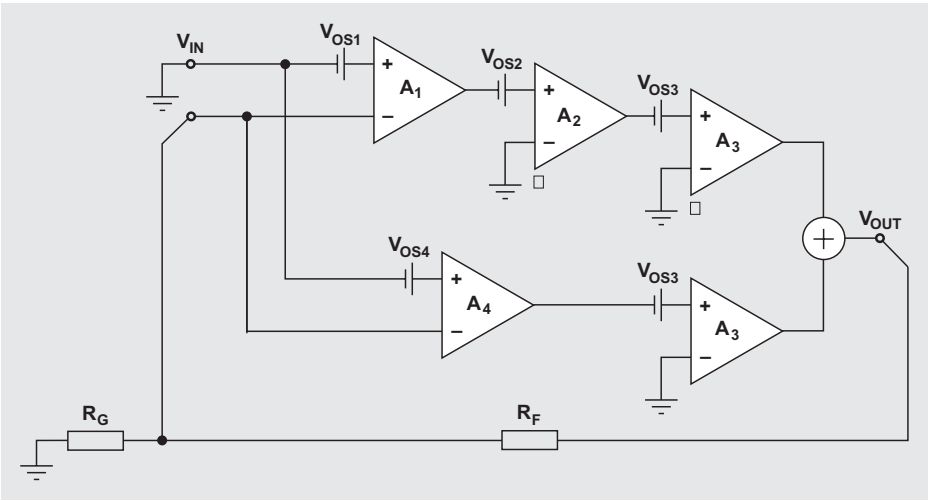


Figure 9. Deriving V_{OUT} as a function of individual offset voltages, V_{OSi}



Providing each amplifier with its individual input offset voltage and setting V_{IN} to zero yields an output of

$$V_{OUT} = A_3\left\{V_{OS3} + A_2\left[V_{OS2} + A_1\left(V_{OS1} - V_{OUT}\,\beta\right)\right]\right\} + A_3\left[V_{OS3} + A_4\left(V_{OS4} - V_{OUT}\,\beta\right)\right],$$

where

$$\beta = \frac{R_F}{R_F + R_G}.$$

Separating the V_{OUT} terms and solving for V_{OUT} gives

$$V_{OUT} = \frac{1}{\beta}\left(\frac{2V_{OS3} + V_{OS2}A_2 + V_{OS4}A_4 + V_{OS1}A_1A_2}{A_1A_2 + A_4}\right).$$

Assuming that the DC gains of A_4 and A_1 are matched,

$$V_{OUT} = \frac{1}{\beta}\left(\frac{2V_{OS3}}{A_1A_2} + \frac{V_{OS2}}{A_1} + \frac{V_{OS4}}{A_2} + V_{OS1}\right).$$

We see that, except for V_{OS1}, all offsets are strongly suppressed by the open-loop gains of at least one, if not two, preceding amplifiers. The nonattenuated V_{OS1}, however, requires active cancellation through either chopping or auto-zeroing.

Auto-zeroing versus chopping

Figures 10 and 11 show the simplified principles of both offset cancellation methods. Auto-zeroing consists of two phases, a nulling phase with switches in position 1 and an amplification phase with switches in position 2. In the nulling phase, the amplifier measures its own offset and stores it on capacitor C_1. In the amplification phase, the amplifier measures the input voltage plus the offset and subtracts the previously stored offset from the contaminated input. The resulting, offset-free output signal is stored on C_2 and operates as correcting voltage for the main amplifier.

The function of sampling and holding the offset voltage makes the AZA a data-sampling system prone to aliasing and folding effects. For DC and low frequencies, the noise properties in the time domain change slowly, and the subtraction of two consecutive noise samples results in a true cancellation. At higher frequencies this correlation diminishes, and subtraction errors translate into wideband fold-over components in the baseband, where they make up the lion's share of baseband noise.

Figure 12 shows that the AZA removes offset and 1/f noise, but at the cost of a significantly raised noise floor in the baseband.

Because the noise power density of an amplifier's input stage is inversely proportional to its transconductance

Figure 10. Auto-zero principle

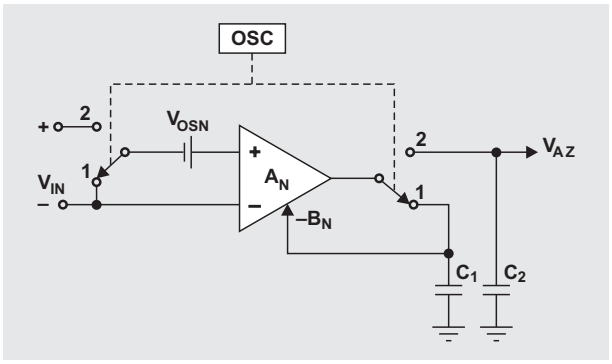


Figure 11. Chopper principle

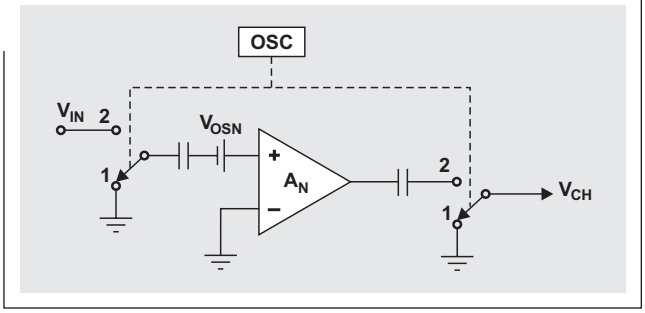


Figure 12. Auto-zeroing and chopping effects on baseband noise

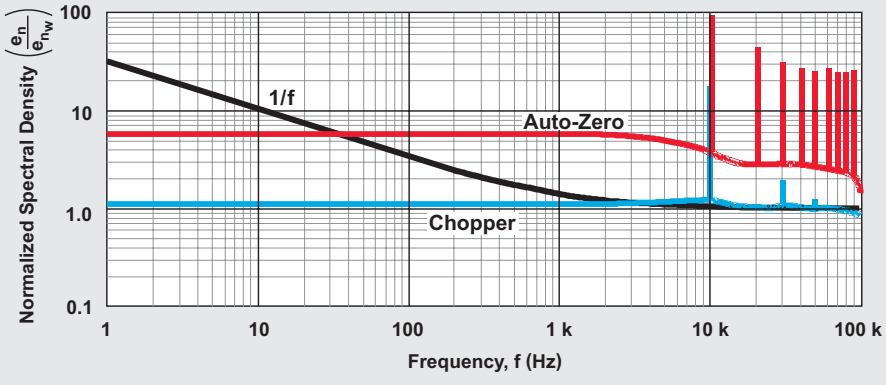
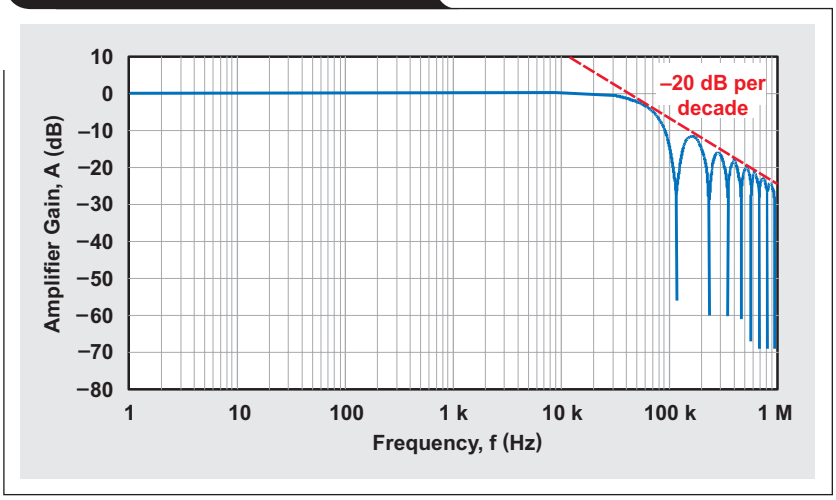


Figure 13. Filter transfer function



($e_n^2 = 2/3 \times 4KT/g_m$), and g_m is proportional to the stage quiescent current ($g_m \approx I_Q$), the power density is inversely proportional to the quiescent current ($e_n^2 \approx 1/I_Q$). Therefore, to reduce the baseband noise of an AZA to the desired level, the initial input noise must be lowered through a significant increase in quiescent current, which counteracts the intrinsic requirements of a micropower amplifier.

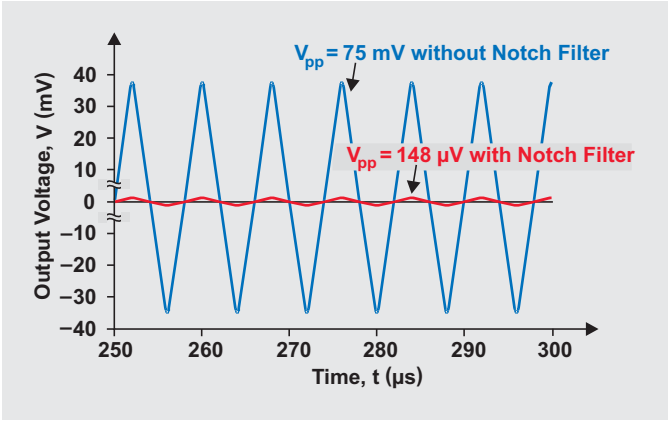
In strong contrast to the AZA, the chopper amplifier does not introduce aliasing fold-over components. As shown in Figure 11, a chopper simply modulates its offset and low-frequency noise to higher frequencies. Here the noise is neither sampled nor held, just periodically inverted without changing the general properties of the noise in the time domain. Although the power density of the chopper output noise results from a summation in the chopper modulation, as is the case for the sample-and-hold process in the AZA, the replicas (odd harmonics only) vary rapidly via a $1/n^2$ function, making their contribution to the baseband negligible.

As shown in Figure 12, for chopper frequencies larger than the noise-corner frequencies, the baseband white noise in the output is only slightly larger than the initial white-noise floor, which eliminates increases in quiescent current and makes the chopper amplifier suitable for micropower applications.

Output noise filter

While the chopper does not introduce wideband folding components into the baseband, the process of chopping does modulate the offset, or DC noise, into the higher frequency range where no noise existed before, thus creating large output ripples. The OPA333 therefore possesses a switched-capacitor (SC), low-pass notch filter in the offset cancellation path with filter notches at the chopper frequency and its harmonics. The filter's transfer function, shown in Figure 13, reduces the output ripple by a factor of more than 500. Figure 14 shows the difference in output ripple with and without the notch filter.

Figure 14. Output ripple with and without filter



The final amplifier system

Figure 15 shows the actual implementation of the chopper-stabilized amplifier, revealing a differential signal-path structure for g_{m1} and the SC notch filter. Note that, for signal symmetry, the implementation of a third capacitor, C_3, is required.

During phases 1 and 2, the input signal is modulated. During phases 3 and 4, the capacitors C_5 and C_6 work in tandem. While C_5 is charged with g_{m1}'s output current, the charge of C_6 is transferred to the integrator, g_{m2}, and vice versa.

Note that the input signal is modulated twice, once by the input switches of g_{m1} and a second time by the output switches. Relative to V_{IN}, the polarity or direction of g_{m1}'s output current remains the same during phases 1 and 2. However, the offset voltage, or offset current, is modulated only once by the output switches. Its polarity changes from phase 1 to phase 2.

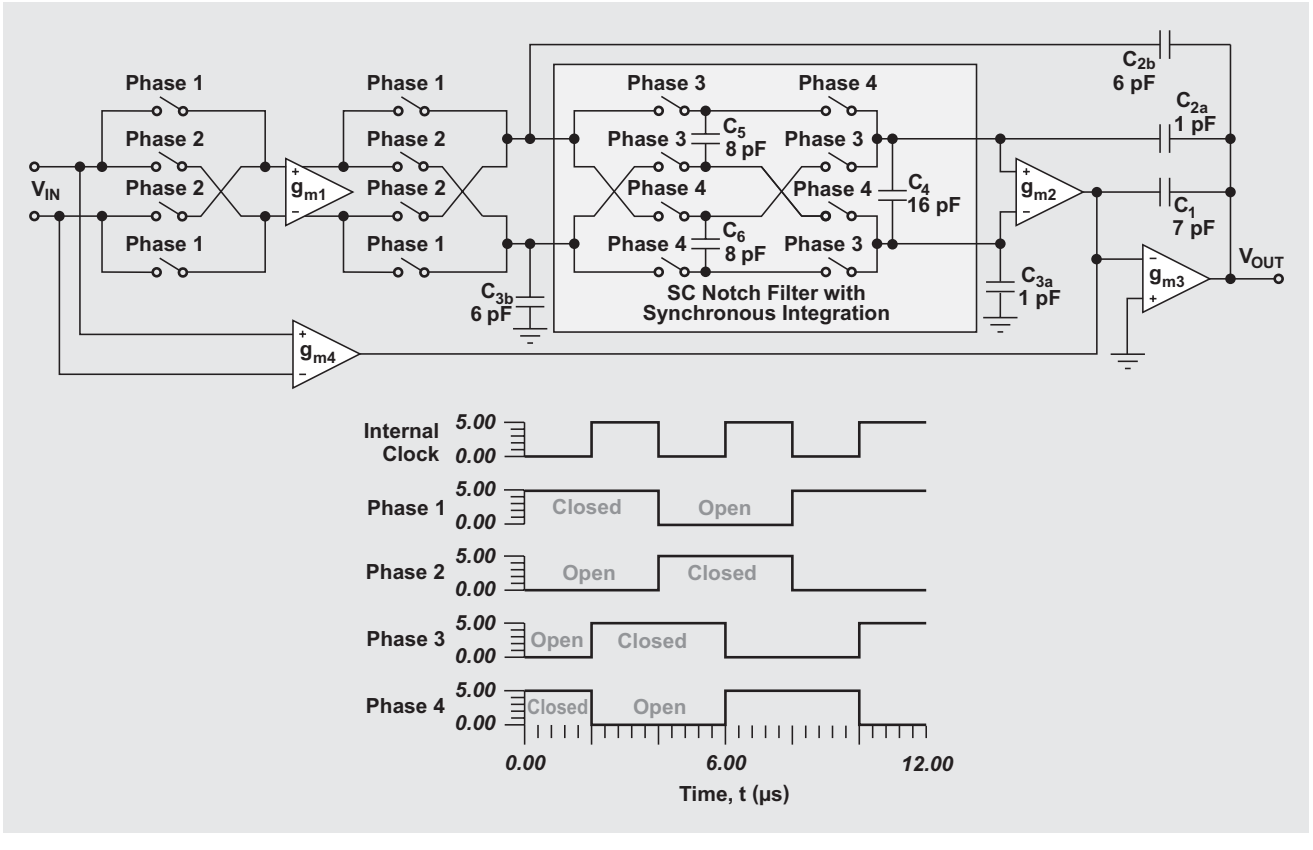
During the first half of phase 3 (that is, $t_{CK}/2$ of the clock period), the phase 1 switches are active and C_5 is charged with g_{m1}'s output current, $I_{SIG} + I_{OS}$. During the second half of phase 3, the phase 2 switches are active, the direction of the offset current changes, and C_5 is charged with $I_{SIG} - I_{OS}$.

The capacitor charge is given by $Q = I_C \times t$, with $t = t_{CK}/2$, $I_{C1} = I_{SIG} + I_{OS}$, and $I_{C2} = I_{SIG} - I_{OS}$. Thus, after phase 3 is completed, C_5 has the charge of $Q_{C5} = (I_{SIG} + I_{OS}) \times t_{CK}/2 + (I_{SIG} - I_{OS}) \times t_{CK}/2 = I_{SIG} \times t_{CK}$. The offset-free charge is then transferred to the next stage during phase 4, where the same procedure is applied to C_6.

While the large attenuation of the notch filter removes the output ripple, it may also filter the signal to some degree. A signal delay is created by the integrate-and-transfer action, which affects the circuit differently depending on how the compensation capacitors are connected.

Notice that C_2 and C_3 have been split into "a" and "b" portions (Figure 15). The "b" portion returns most of the compensation to the filter input, C_{2b} = 6 pF, maintaining good continuous-time characteristics for the signal path. The smaller "a" portion, C_{2a} = 1 pF, connects to the filter output, providing sufficient local-loop stability. The complex compensation scheme is responsible for a slight rise in the

Figure 15. Internal block diagram and timing sequence



noise floor beyond 20 kHz, which is visible in Figure 16.

Summary

This article elaborates on the technical implementations of the OPA333, the industry's superior, zero-drift micropower amplifier. Chopper stabilization ensures low baseband noise at very low supply currents. An integrated, patent-pending notch filter removes the output ripple created by the chopper modulation of the input offset.

Because an amplifier's noise power density is inversely proportional to its quiescent current, the product ($e_n^2 \times I_Q$) represents a figure of merit, revealing how much additional tail current was necessary to reduce the remaining baseband noise to the desired level after the process of offset cancellation. A more familiar figure is the ratio of gain bandwidth to quiescent current, GBW/I_Q, disclosing how much bandwidth per microampere was achieved. In both figures of merit, the OPA333 demonstrates far superior performance versus even its closest competitor (see Table 1).

Related Web sites

amplifier.ti.com
www.ti.com/sc/device/OPA333

Figure 16. DC to 20-kHz and 200-kHz noise spectra

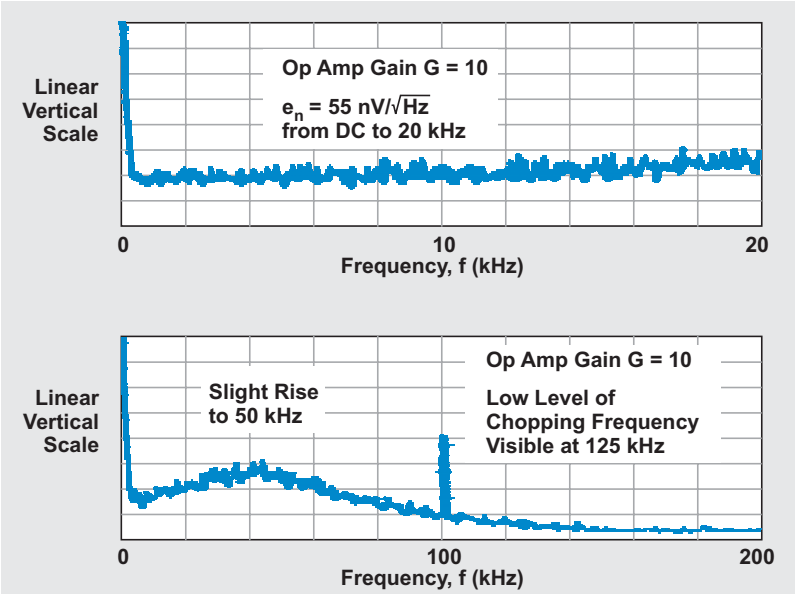


Table 1. Comparison of the OPA333 versus previous zero-drift amplifiers

	TI	COMPETITOR				
DEVICE	OPA333	(1) AD8628	(2) ICL7650	(3) LTC2054	(4) OPA335	(5) AD8551
Year	2006	2005	2005	2004	2002	2002
f_{CH} (kHz)	125	15	—	—	—	—
f_{AZ} (kHz)	—	15	0.25	1	10	4
V_{OS} (µV)	2	1	1	3	1	1
I_B (pA)	70	30	5	1	70	10
GBW (kHz)	350	2500	2000	500	2000	1500
e_n (nV/√Hz)	55	22	25	85	55	42
I_Q (µA)	15	1100	2000	150	285	975
$e_n^2 \times I_Q$ (nV² × µA)*	45	532	1250	1084	862	1720
GBW/I_Q (kHz/µA)*	23	2	1	3	7	2

*Figure of merit

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