Conversion latency in delta-sigma converters

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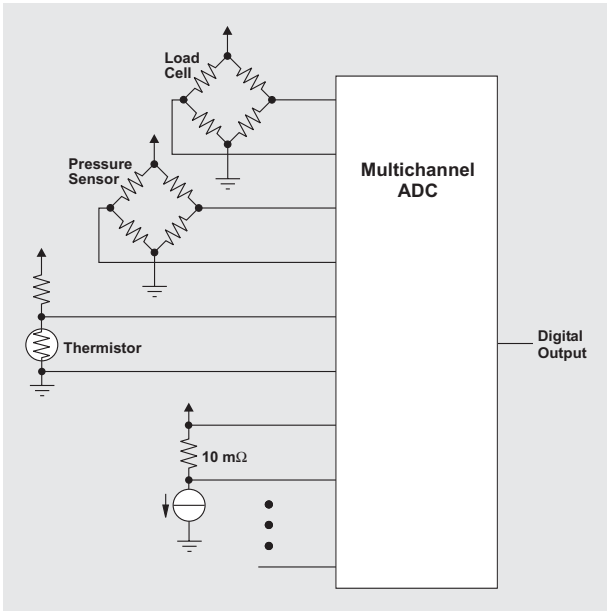
Small-signal sensors often generate slow-moving dc signals. For these types of sensors, the delta-sigma (ΔΣ) analog-to-digital converter (ADC) eliminates most of the analog input circuitry by providing a complete high-resolution, low-noise solution. Some systems have multiple sensors generating low-frequency signals. This situation may require a high-resolution, low-noise ADC with a multiplexer at its input. An example of a multiplexed sensor system is an automotive diagnostic application where numerous small-signal sensors monitor temperature, tire pressure, air-bag readiness, etc. (see Figure 1). Examples of other sensor-input multiplexed systems are found in industrial-control, medical, avionics, and process-control applications. Even though the sensors at the input of the multiplexer in these systems present low-frequency (nearly dc) signals, switching from channel to channel creates the need for an ADC that is capable of a high-speed response.

There are two common units of measure that describe the latency of an ADC: cycles and seconds. Cycle latency is the number of complete data cycles between the conversion initiation and the availability of the corresponding output data. Latency time, measured in seconds, tells the user how fast fully settled conversions can be performed.

In the system in Figure 1, the multiple-channel ADC must have high resolution, low noise, zero-cycle latency, and low latency time. (Zero latency or 0-cycle latency is sometimes called no latency.)

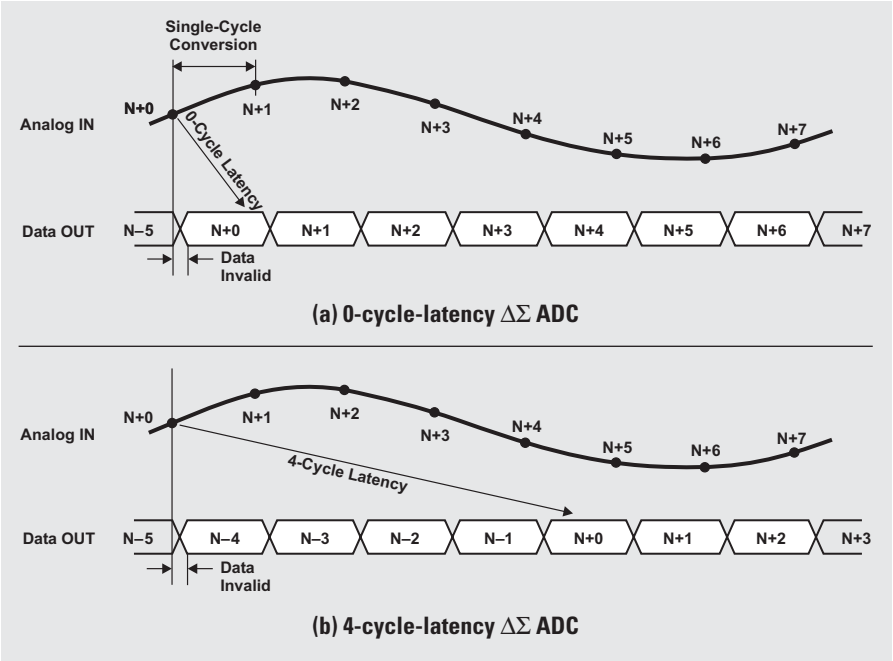
Figure 1. Example multiplexed sensor system



ADC cycle latency

For ADCs, cycle latency is the number of *complete* data cycles between the initiation of the input-signal conversion and the availability of the corresponding output data (see Figure 2). The unit of measure for this definition of latency is N-cycle latency, where N is a whole number. Figure 2 shows the timing diagrams for a 0-cycle-latency (or zero-latency) ADC and a 4-cycle-latency ADC. In Figure 2(a), with 0-cycle latency, the sampling period of N+0 is initiated. The output data of N+0 is acquired before the sampling period of N+1 is initiated. In Figure 2(b), with 4-cycle latency, the sampling period of N+0 is

Figure 2. Comparison of cycle-latency behavior of two ΔΣ ADCs



initiated. The output data of N+0 is presented after the completion of four conversion cycles.

Figure 3 shows zero-latency ADC behavior graphically. In Figure 3, the input signal is first acquired at t_0. The ΔΣ converter continues to acquire input samples through the sampling period and continually modulates the signal into a noise-shaped representation. The digital low-pass/decimation filter accumulates the noise-shaped signal and generates the output code at the end of the t_0 period. A ΔΣ converter has zero latency if data is available before a new sampling period is initiated. The output code represents the oversampled, filtered-input signal. At t_1 the converter initiates the next sampling period.

The successive approximation register (SAR) ADCs are capable of zero latency as are many ΔΣ converters. The better choice for the application shown in Figure 1 is a high-resolution, zero-latency ΔΣ ADC. Some data sheets for ΔΣ ADCs claim single-cycle conversions. This is another way of saying that a converter has zero latency.

Texas Instruments (TI) offers numerous multiplexed, zero-latency ΔΣ ADCs that provide low-noise, high-resolution solutions (see Figure 4). These ΔΣ converters are capable of masking the filter action and providing a fully settled signal before the end of one cycle. As an example, TI's 16-channel, 24-bit ADS1258 has an internal, fifth-order, sinc digital filter followed by a programmable, first-order averaging filter. When the converter is configured in its auto-scan mode, the cycle latency is zero. In the auto-scan mode, the ADS1258 scans through the selected channels automatically, with break-before-make switching.

ADC latency time

Latency time is typically viewed as the time required for an ideal step input to converge, within an error margin, to a final digital output value. This error band can be expressed as a predefined percentage of the total output-voltage step. The latency time of a conversion is the time between the beginning of the signal acquisition and the time when data is available to download from the converter. In contrast to the cycle-latency specification, the latency time (or settling time) is never equal to zero.

Figure 5 compares the latency-time performance of various multiplexed ΔΣ ADCs. The latency time of a zero-latency ΔΣ ADC varies from device to device, depending on the system clock and the order of the converter's digital filter. A requirement for larger applications is that the multiplexed ADC must quickly cycle through the channels. The latency time for these types of applications can be critical.

Figure 3. Typical input and output of zero-latency ΔΣ ADC

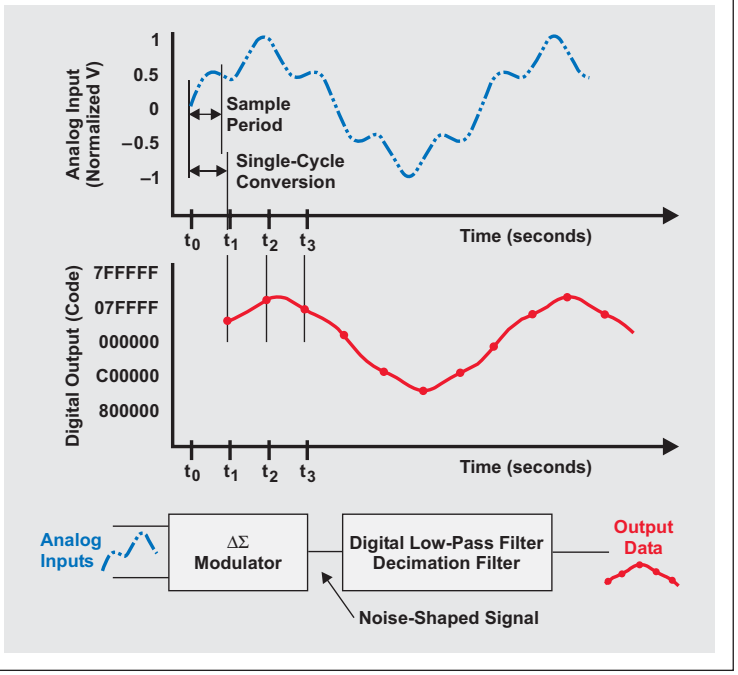


Figure 4. TI's multiplexed zero-latency ΔΣ ADCs

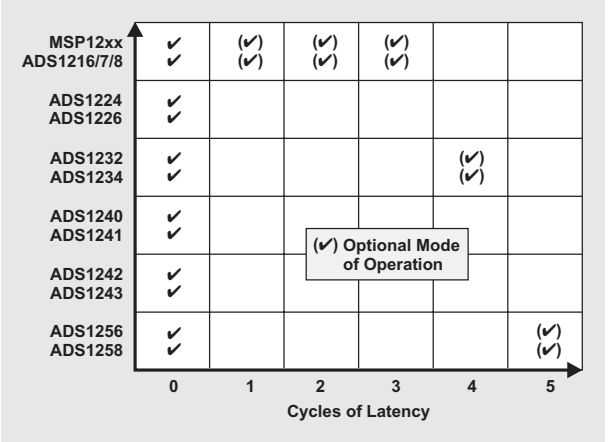
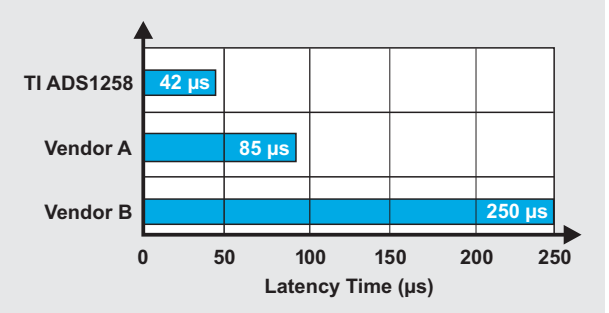


Figure 5. Latency-time comparison of ΔΣ ADCs



When the ADS1258 (Figure 6) is configured in its auto-scan mode (zero latency), the output data is fully settled at the end of each conversion. The minimum latency time in the ADS1258's auto-scan mode is 42 µs.

It is possible to reduce the throughput time of a zero-latency ΔΣ ADC if the intermediate or masked digital filter results are available. In this mode, the digital output results are not necessarily fully settled. For these devices the throughput time is always less than the latency time. Reduction of throughput time best suits sensors that produce small voltage changes at a slow rate (such as temperature sensors, pressure sensors, or load cells). With these types of sensors it might be advantageous to acquire several conversions and perform post-processing on the data.

When the ADS1258 is configured in its fixed-channel mode, the intermediate results from the fifth-order digital filter are available to the user. In the ADS1258 fixed-channel mode, the converter is no longer automatically cycling from channel to channel, and the output data may or may not be fully settled. The minimum throughput time of the ADS1258 in fixed-channel mode is 8 µs (⅕ of the fully settled latency time).

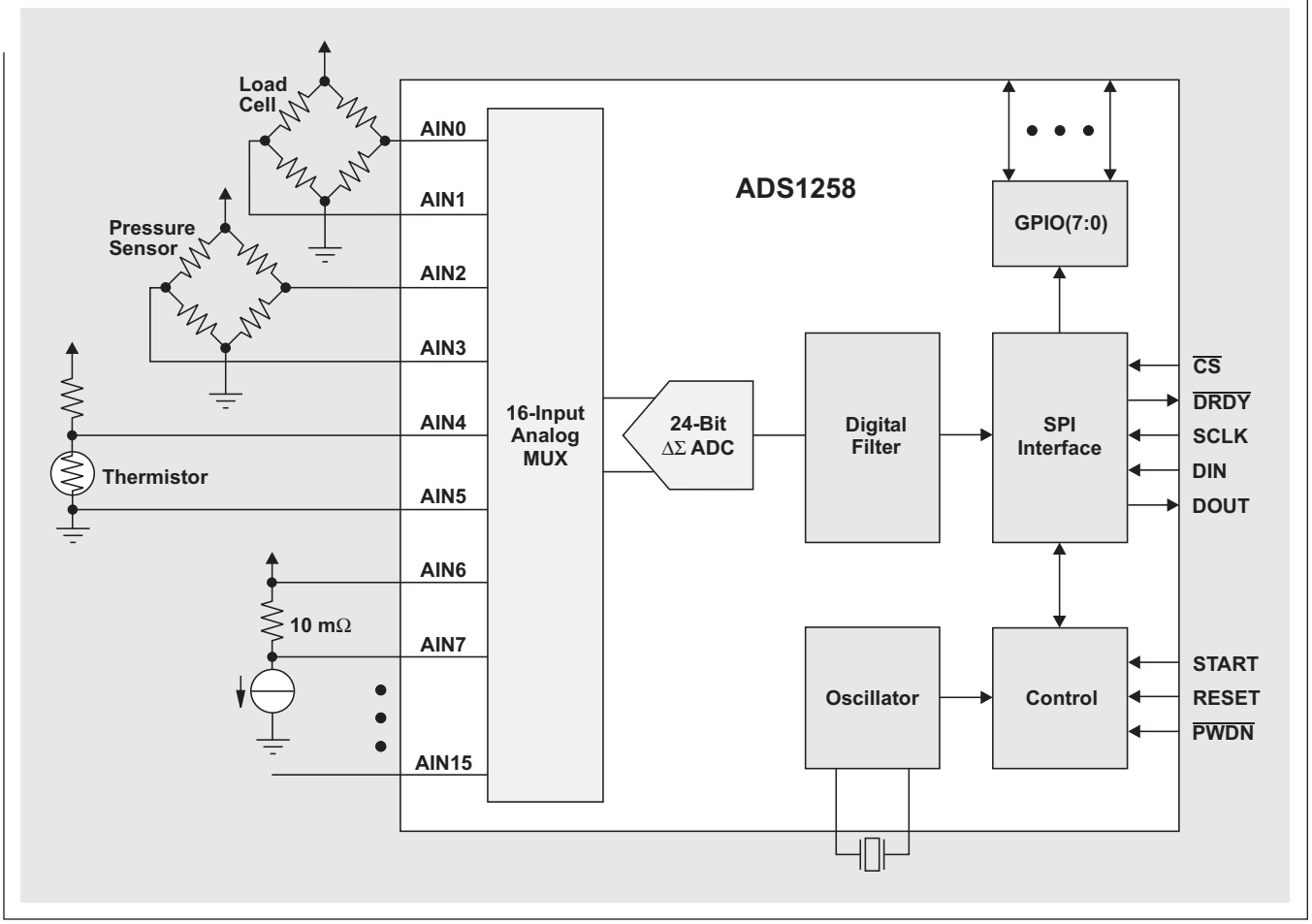
Conclusion

The economy and efficiency of using multiplexed ΔΣ ADCs for applications with multiple sensors must be weighed against possible problems caused by ADC conversion latency and any latency introduced by external processing. The TI ADS1258 offers 16-channel, 24-bit conversions with low noise and zero latency. The device's single-cycle, low-latency-time capability provides fully settled data at the end of each conversion cycle. In auto-scan mode, the ADS1258 can complete a conversion for all 16 channels in under 700 µs. Cycle latency and the total conversion time must be evaluated for each ADC considered to be sure the device will perform as intended.

Related Web sites

dataconverter.ti.com
www.ti.com/sc/device/ADS1258

Figure 6. The ADS1258, a 16-channel, zero-latency, 24-bit ΔΣ ADC



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