

Synchronizing non-FIFO variations of the THS1206

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Data Acquisition Applications

Introduction

The THS1007, THS1009, THS1207, and THS1209 are non-FIFO variations of the popular THS1206, four-channel, 6-MSPS, simultaneous-sampling ADC. These devices are used in high-speed, cost-sensitive systems that do not require the ADC to furnish an interrupt to the host processor. This article explains the steps required to synchronize the data output from these 10- and 12-bit, two- and four-channel, simultaneous-sampling data converters.

Part details

The THS1007 and THS1207 are 6-MSPS parallel devices with four analog inputs. The inputs can be configured for either two-channel differential or four-channel single-ended operation. The THS1009 and THS1209 are 8-MSPS parallel devices with two analog inputs that can act as one differential channel or two single-ended channels. As their names imply, the resolution of these devices is 10 and 12 bits.

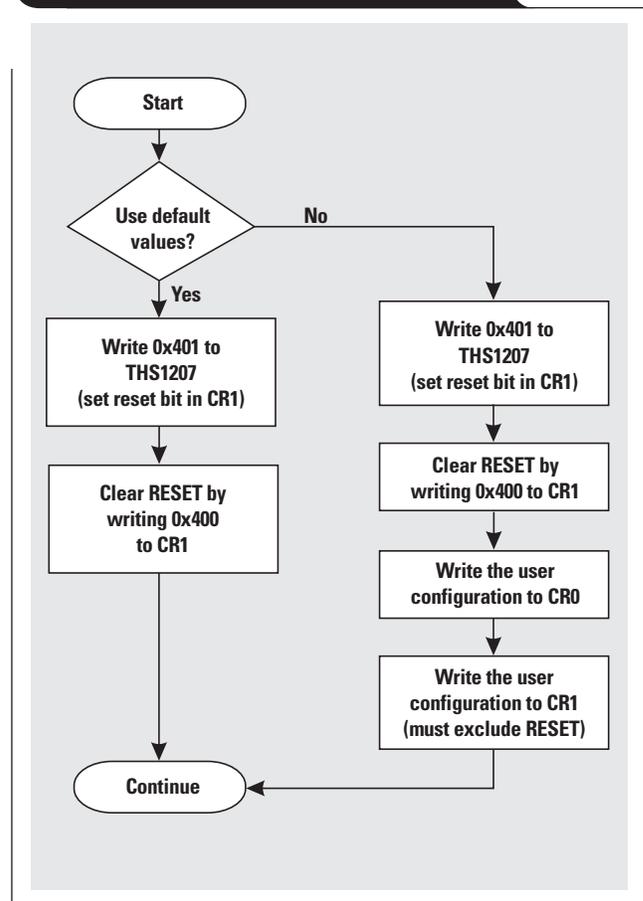
All four devices offer Auto-Scan modes, low-power operation, and a 3- to 5-Vdc digital interface for direct connection to digital signal processors. One of the major differences between these devices and their FIFO-enabled counterparts is that they operate only in continuous conversion mode. The conversion clock signal (CONV_CLK) cannot act as a conversion start pulse (CONVST) as it can in the THS10064, THS1206, THS10082, and THS12082 devices. The CONV_CLK signal needs to be maintained at a 50% duty cycle with a minimum frequency of 100 kHz.

Another major difference is that the data available (DATA_AV) signal found in the THS10064, THS1206, THS10082, and THS12082 devices is replaced with a signal referred to as "SYNC." The DATA_AV pulse on the FIFO devices acts as an interrupt source to the host controller. This allows the controller to perform other functions while the ADC is gathering data. The user has the ability to set a trigger level on the internal FIFO so that, when the trigger level is reached, the DATA_AV pulse is issued and the host processor reads out the acquired data from the ADC.

The SYNC output signal from the non-FIFO devices is not intended to act as an interrupt source to the host processor. The SYNC signal is merely an indication that data from channel 1 is available. The SYNC signal is active only in multi-channel modes; SYNC is disabled when single-channel operation is selected.

When two or more channels of the ADC are selected for operation, the SYNC signal indicates when channel 1 data is available to the data bus by bringing the SYNC pin low for an entire CONV_CLK cycle. To ensure that the SYNC pulse is properly aligned with channel 1, the "SYNC generator" within the device must be reset.

Figure 1. Example configuration flow



Resetting the SYNC generator

Bit 1 of control register 1 (CR1) can be considered the SYNC generator reset bit (SRST). This is similar to the THS1206's use of this bit to reset the FIFO. Writing a 1 to CR1, bit 1, during the configuration sequence of the THS1007, THS1009, THS1207, and THS1209 resets the SYNC generator and aligns the SYNC signal with channel 1.

Figure 1 shows the initialization sequence of the THS1207. After power-up, it is necessary to perform a device reset by writing hex values 0x401 and 0x400 to the device. If the default configuration values are desired, there is no need to perform any additional writes to the ADC. On the non-FIFO devices, the default value for control register 0 (CR0) is 0x020. The default value for CR1 is 0x030.

Table 1. Bit definitions for control registers CR0 and CR1 of the THS1207

REG	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CR0	TEST1	TEST0	SCAN	DIFF1	DIFF0	CHSEL1	CHSEL0	PD	RES	VREF
CR1	RBACK	OFFSET	BIN/2's	R/W	RES	RES	RES	RES	SRST	RESET

Because the default configuration values select single-channel operation, the SYNC pulse is disabled and there is no need to reset the SYNC generator.

If multiple-channel operation is desired, it is necessary to set the SRST bit as part of the user configuration write to CR1 (CR1 bit 1 = 1). It is not necessary to clear the SRST bit once it has been set.

A popular debug feature of the 12-bit ADCs in this device family is the register readback function. It allows the user to verify the contents of both the CR0 and CR1 registers (see Table 1) by performing two successive reads from the data bus. Shown as “RES” in the 10-bit data sheets, bit 9 of CR1 provides the same functionality on the THS10xx devices when combined with some simple software intervention. The 10-bit parts perform an internal “shift right by two” that requires the user to shift the resultant data 2 bits to the left. Bit 4 will appear set on register readback, indicating that the SYNC signal is at an active-low, static level. Note that the SYNC pulse is not available during register readback operations.

Reading data

Proper data readings depend on the proper application of the read signal. As with their FIFO-enabled counterparts, the THS1007, THS1009, THS1207, and THS1209 can be configured with independent, active-low read-and-write strobes. Active-low CS0 and active-high CS1 provide chip selection to the device and can be tied to static levels if desired.

With the non-FIFO devices, it is necessary to issue a read strobe after each CONV_CLK. As mentioned earlier,

it is not appropriate to consider the SYNC pulse as an interrupt source to the host processor. The SYNC pulse is merely an indication that data currently available is the data acquired from channel 1.

Recall that the SYNC pulse is not available when the device is configured for single-channel operation. This is true for the two-channel THS1009 and THS1209 as well as for the four-channel THS1007 and THS1207. The SYNC pulse is active only when two or more channels are selected for conversion.

Data setup times are listed in the data sheets as “ $t_{SU}(CONV_CLKL_READL)$.” The read strobe should be applied after this setup time but before the subsequent falling CONV_CLK edge. Failure to read the data bus within each conversion cycle, or multiple reads during the same conversion cycle, can cause the SYNC pulse of the THS1007, THS1009, THS1207, and THS1209 to behave erratically. Setting bit 1 of CR1 will clear erratic SYNC pulse behavior.

Figures 2 and 3 show the result of setting the SRST bit. In both cases, a THS1207 was configured for three single-ended analog inputs, using SCAN mode to read the data. The /RD strobe was disabled. The conversion clock is intentionally stretched when channel 1 is active to indicate where the SYNC pulse should be. Figure 2 shows the results of writing 0x090 to CR0 and 0x4C0 to CR1. Figure 3 shows the results of writing 0x090 to CR0 and 0x4C2 to CR1.

As shown in Figure 2, the SYNC signal appears erratic. By setting SRST = 1 in CR1, the SYNC signal goes active low on the falling edge of the conversion clock, indicating the position of channel 1 conversion data.

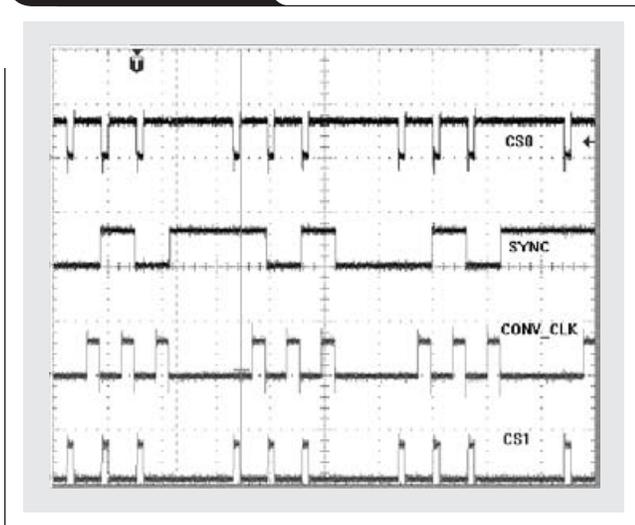
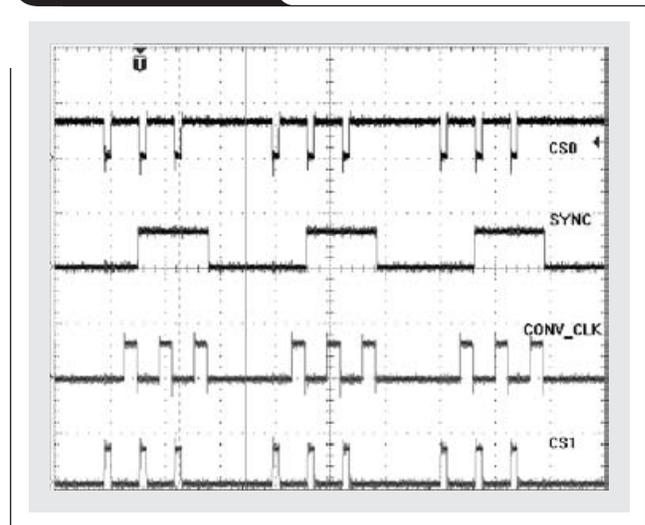
Figure 2. SRST = 0**Figure 3. SRST = 1**

Figure 4 shows the relative timing of the SYNC signal in two-, three-, and four-channel modes. The SYNC signal will appear at half the CONV_CLK frequency in two-channel mode, one-third the CONV_CLK frequency in three-channel mode, and one-quarter the CONV_CLK frequency in four-channel mode. As related to Figures 2 and 3, the READ strobe shown in Figure 4 is the logical combination of CS0 and CS1 (valid chip select conditions).

Understanding the behavior of the SYNC signal plays a vital role in the development of a low-cost data acquisition system using the THS1007, THS1009, THS1207, and THS1209. The same 32-pin TSSOP package and common

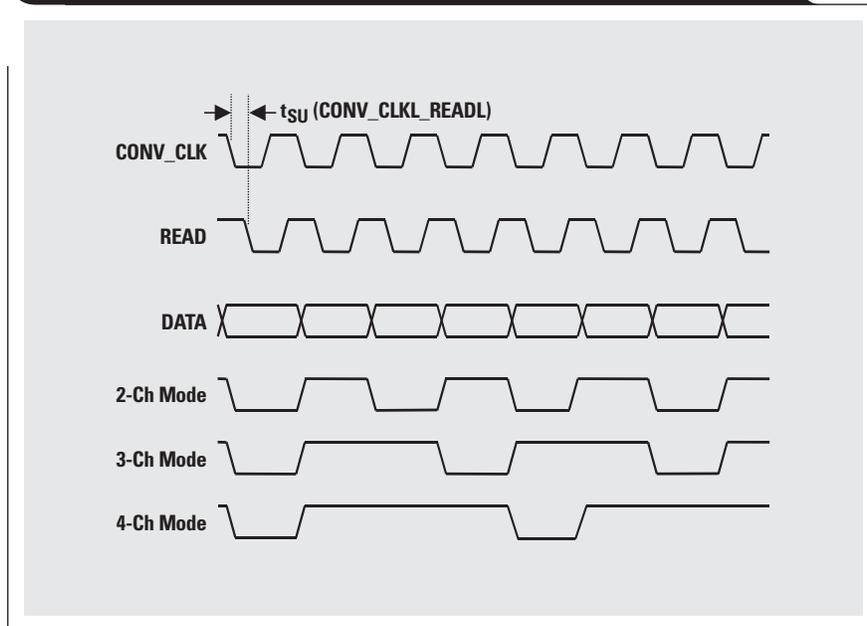
pinout throughout the two- and four-input converters provide the ability to upgrade to the FIFO-enabled THS10064, THS10082, THS1206, and THS12082 devices without costly hardware changes. For the latest data sheets and additional application information, please visit the Texas Instruments Web site.

Related Web sites

www.ti.com/sc/device/partnumber

Replace *partnumber* with THS1007, THS1009, THS1206, THS1207, THS1209, THS10064, THS10082 or THS12082

Figure 4. SYNC pulse in two-, three-, and four-channel modes



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