Clocking high-speed data converters

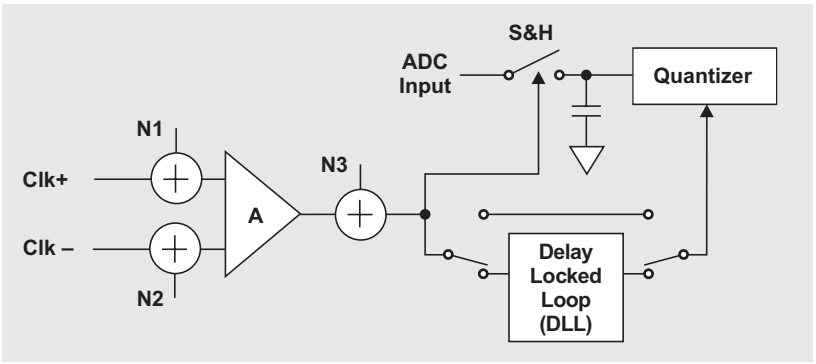
By Eduardo Bartolome, *High-Speed ADC Systems and Applications Manager* (Email: e-bartolome1@ti.com),
Vineet Mishra, *High-Speed ADC Design Engineer* (Email: vineetm@ti.com),
Goutam Dutta, *High-Speed ADC Test Engineer* (Email: g-dutta2@ti.com),
and David Smith, *High-Speed ADC Test Engineer* (Email: w-smith13@ti.com)

Introduction

In circuit design that involves the use of a high-performance, high-speed analog-to-digital converter (ADC) such as the ADS5500, one of the main careabouts is the clocking scheme. Questions about the type of clock to be used (sinusoidal or square), the voltage levels, or the jitter are common. The purpose of this article is to explain the general theory to support the circuit designer in making the right choices.

Figure 1 shows a simplified model of the clock circuit inside a high-speed ADC like the ADS5500. Although not all ADCs have exactly the same internal blocks in their clock distribution, this diagram can be modified to fit your particular ADC. Since nowadays most of the circuits sold as ADCs include a front sample-and-hold (S&H), for the purpose of this article we will differentiate between them. The circuit that takes an instantaneous analog snapshot of the input signal will be called the S&H; and the ADC itself, which converts the analog value being held by the S&H into quantized digital output, will be called the quantizer. Analyzing what parameters of the internal clock are important for these two circuits will help us understand the main careabouts in our external clock design.

Figure 1. Simplified model of clock circuit in high-speed ADC

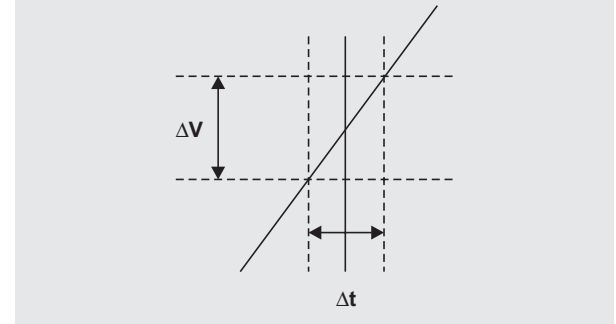


Errors in the sampling instant

The conversion process starts when a clock signal tells the S&H to take the sample. Up to that instant, the internal switch on the S&H circuit has been closed, allowing the voltage across the capacitor to track the input signal (which is why other literature more properly calls this circuit "track and hold"). One of the edges of the input clock then indicates when to open this switch, and the capacitor holds the voltage at that instant in time. This instant is represented in Figure 2 by a vertical solid line. Any error in that instant (Δt) will translate as an error in voltage (ΔV) dependent on the input signal slope. The error in that instant is what we will call jitter.

A mathematical estimation of the best-case signal-to-noise ratio (SNR) (without other noise sources), given a certain amount of jitter, can be extracted from Figure 2. Given a sinusoidal input of amplitude A and frequency f_{IN} (1/T), the uncertainty of the sampled voltage at a given point will be proportional to the slope of the input signal at that instant and to the uncertainty of the sampling instant (jitter, which is the rms value of that variation,

Figure 2. Voltage error relation to sampling jitter



uncorrelated with the input level). The total uncertainty is the addition of all the uncertainties at each point of the sinusoid weighted by the probability of sampling each of the points:

$$\sigma^2_{Jitter} = \frac{1}{T}\int_0^T \left(Slope(\tau)\times Jitter\right)^2 d\tau = \frac{1}{T}\int_0^T \left[\frac{d\left(A\sin\frac{2\pi\tau}{T}\right)}{d\tau} Jitter\right]^2 d\tau$$

$$= \frac{1}{T} Jitter^2 \int_0^T \left(\frac{2\pi A\cos\frac{2\pi\tau}{T}}{T}\right)^2 d\tau = \left\langle a = \frac{2\pi\tau}{T}, \frac{da}{d\tau} = \frac{2\pi}{T}\right\rangle$$

$$= \frac{T}{2\pi}\left(\frac{2\pi A}{T}\right)^2 Jitter^2 \frac{1}{T}\int_0^{2\pi} (\cos^2 a)da = \frac{T}{2\pi}\left(\frac{2\pi A}{T}\right)^2 Jitter^2 \frac{1}{T}\frac{1}{2}(a+\sin a\times\cos a)\Big|_0^{2\pi}$$

$$= \frac{T}{2\pi}\left(\frac{2\pi A}{T}\right)^2 Jitter^2 \frac{1}{T}\pi = \frac{1}{2}\left(\frac{2\pi A}{T}\right)^2 Jitter^2$$

The theoretical limitation of the SNR due to jitter is given by

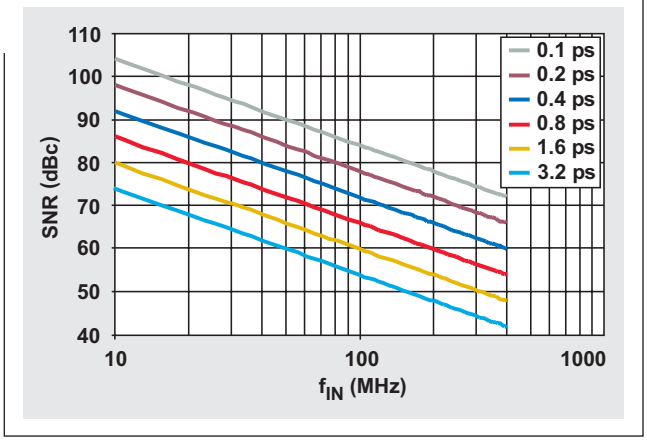
$$SNR\,(dBc) = \frac{S}{N} = 10\log_{10}\left[\frac{\frac{A^2}{2}}{\frac{1}{2}\left(\frac{2\pi A}{T}\right)^2 Jitter^2}\right] = -20\log_{10}(2\pi f_{IN}\,Jitter). \quad \textbf{(1)}$$

Figure 3 shows this limitation as a function of the input frequency.

Observe that increasing or decreasing the input amplitude (A_{IN}) has no effect on the SNR component coming from jitter. In other words, as we decrease the input amplitude, the amount of error due to the jitter also becomes smaller. Nevertheless, there are other sources of error, like thermal noise, that do not get smaller. Assuming all these sources of noise are uncorrelated, the total noise is the addition of a noise term independent of input frequency and a noise term dependent on input frequency (jitter):

$$SNR\,(dBc) = 10\log_{10}\left[\frac{\left(\frac{A}{\sqrt{2}}\right)^2}{Thermal + Quantization + \frac{1}{2}\left(\frac{2\pi A}{T}\right)^2 Jitter^2}\right] \quad \textbf{(2)}$$

Figure 3. Limitation of the SNR due to jitter as a function of input frequency



For a given ADC, below a certain input amplitude, the SNR is dominated by those other sources and jitter becomes irrelevant. One way of showing this is plotting the noise floor in dBFS with respect to the A_{IN}. Figure 4 shows a real noise-floor example of the ADS5542 operating at 78 MSPS and 230-MHz input.

Note that the theoretical trace, computed by adding the effect of 250 fs of jitter and about 1 LSB of thermal noise (idle channel noise; i.e., noise floor with no ADC input), very closely follows the measured performance. This effect is especially important when we compute the theoretical effects of jitter in our system and try to choose the right ADC and clocking. Specifically, it shows that for certain systems, ADC data taken at –1 dBFS may give us too pessimistic a result, as the signal may seldom reach those levels.

Figure 5 (extracted from Reference 1) shows the SNR versus input and sampling frequencies. This measured plot correlates with Equation 2. How can we explain the degradation observed in the SNR as input frequency (f_{IN}) increases for a fixed sampling frequency (f_S)? Assume that a full-scale sinusoid at low input frequencies is unaffected by jitter and that, as we increase the frequency of that sinusoid, the SNR will be degraded exclusively by clock jitter. In that case, for a given f_S, we can estimate a value for clock jitter. Table 1 shows the measured SNR for f_S = 60 MSPS (see the red horizontal dashed line in Figure 5) versus the estimated SNR using Equation 2 and assuming a jitter of 200 fs.

So Equation 2 seems to model variation in the SNR versus f_{IN} very well. What about SNR variation versus f_S? Does the jitter effect on the noise floor depend on the f_S/f_{IN} ratio? In other words, given a certain amount of phase noise in our clock, will its effect be much worse in the case of 65-MSPS/150-MHz input frequency than in the case of 125-MSPS/150-MHz input frequency? From Equation 2 it is obvious that f_S has nothing to do with SNR jitter. Nevertheless, we observe that as we decrease f_S (following the blue vertical dashed line in Figure 5), the SNR degrades, which seems counterintuitive.

We know that by increasing the input waveform's number of hits per cycle, even with the same likelihood of error on each sample, we will "average out" the bigger portion of the noise. In other words, as we get more samples, each

Figure 4. ADS5542 typical noise-floor measurement

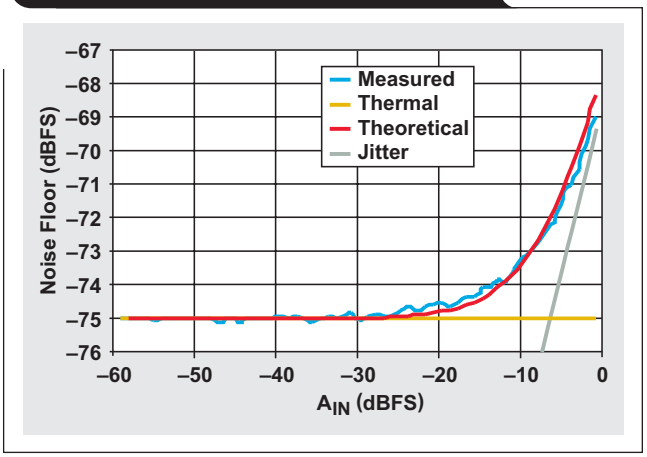
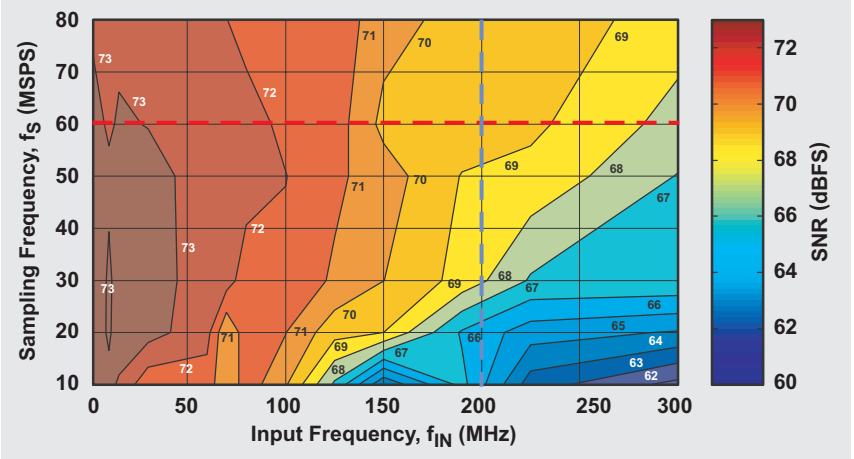


Table 1. Measured vs. estimated SNR

f_{IN} (MHz)	2.00	10.01	15.51	30.00	60.04	70.04	80.01	100.00	125.01	150.00	190.04	225.03	300.02
Measured SNR (dBFS)	73.35	72.84	73.13	72.96	72.75	72.54	72.55	71.68	71.50	69.72	69.61	69.22	67.63
Estimated SNR (dBFS)	73.35	73.34	73.32	73.22	72.85	72.68	72.49	72.08	71.49	70.88	69.86	68.99	67.25

Figure 5. SNR with digital phase lock loop off



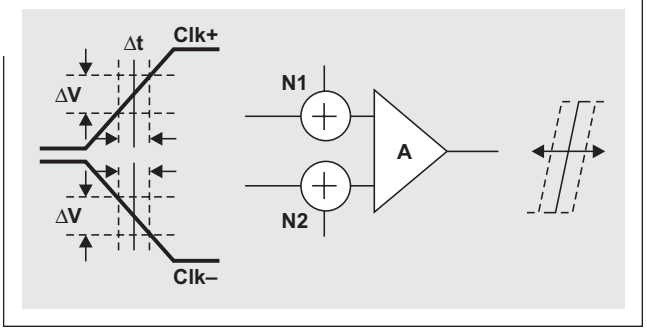
one with the same amount of error, the "average" of those will be more precise. This is no different than the standard concept of process gain. Considering the frequency domain, an increase in the sampling frequency will spread the same amount of noise over a bigger bandwidth, effectively reducing the noise floor. Usually we care about the in-band noise in our signal. Doubling the frequency of our clock will reduce the noise floor by half (i.e., 3 dB). Nevertheless, when we compute the SNR, we integrate all the noise; so this does not explain the SNR degradation that occurs as we decrease f_S. For an explanation we have to introduce a new factor, a new jitter that will not be the same for different sampling frequencies. A further look at Figure 1 will help us understand this SNR degradation.

Note that so far we have been talking about jitter generically as a total jitter budget allocated to our system. The sources for jitter can be external (such as a clock provided by the user) or internal in the ADC. Jitter is a form of simplification ("integration") of a more specific parameter called phase noise. The relationship between jitter and phase noise is explained in References 2 and 3. Disregarding those details, ADC users should at least be aware that not all phase noise in the clock will affect the system equally. Phase noise very close to the carrier reflects slow variation in the sampling instant, which may not be relevant in systems with a "short" observation time. Phase noise for larger offsets away from the carrier may be more important but at the same time easier to filter out. It is important to note that currently ADCs do not provide any mechanism to reject any incoming jitter. On the contrary, the clock chain inside the ADC adds to the jitter degradation. There will always be a delay between initiation of the clock signal and the time when the S&H goes into the hold mode. While the mean of that delay, commonly referred to as "aperture delay," does not produce a nondeterministic error, the variation in that delay will create an error. Some of that variation will come from noise sources inside the ADC (represented as N3 in Figure 1), which the user cannot influence except by modifying some of the external conditions such as temperature or supply. Nevertheless, there are some techniques the user can apply to minimize the influence of other internal sources of noise (N1 and N2). We will center the discussion around this topic.

As shown in Figure 1, the first stage in the internal clock chain is an amplifier. Texas Instruments usually includes such a circuit to present a more clock-friendly interface to the user, with the following features:

- High input impedance to reduce clock driver load.
- Differential amplifier that supports either differential or single-ended inputs.
- Amplifier to support smaller clock swings.

Figure 6. Evaluating the clock rising edge



- "Squares" the input clock signal (if sinusoidal) to generate the internal digital clocks. The amplifier is usually followed by logic circuits to distribute the clock to the internal blocks of the ADC.

Although ADC designers optimize this circuit to minimize jitter, there are always limitations set by the process, power, and other trade-offs. ADC users can model this circuit knowing that it adds a certain noise voltage to the input clock before amplification takes place.

In Figure 6 we represent only the rising edge of the clock, assuming that this is the edge used to open the switch on the S&H circuit (i.e., the edge indicating when to hold the sample). Note that the jitter on the other edge theoretically has no effect on the SNR. For simplicity we are also assuming that the slopes of the edge on the positive (Clk+) and negative (Clk–) lines of the clock are the same (which may not be true, but this has no effect on the following reasoning).

Although the sources of noise are internal (N1, N2), their final effect on performance can be minimized by the user. Specifically, if the input clock has infinite slope, the addition of any (voltage) noise to that edge will not affect the time position of the edge. As the edge becomes slower, the effect of adding any voltage noise will produce a bigger variation in time. In the case where the clock is a sinusoidal signal, increasing the amplitude or the sampling frequency will increase the slope of the edge. We should have the same jitter when we double the sampling frequency as when we double the clock amplitude. All this can be expressed in the following equation:

$$(\text{Jitter}_{\text{Total}})^2 = (\text{Jitter}_{\text{External}})^2 + (\text{Jitter}_{\text{N3}})^2 + (\text{Jitter}_{\text{N1,N2}})^2$$
$$= (\text{Jitter}_{\text{External}})^2 + (\text{Jitter}_{\text{N3}})^2 + \left[\frac{\text{K(N1,N2)}}{\text{Clk\_slope}}\right]^2, \quad (3)$$

where K(N1, N2) represents the input amplifier jitter contribution and is constant for each ADC.

Let's take a look at Figure 7 (adapted from Figure 17 in Reference 4). This figure really shows how to squeeze the last dB from the SNR at high input frequency. In line with the previous discussion, one of the first things that catches our attention is that as we increase the clock amplitude, the SNR improves. We are just minimizing the effect of the third term of Equation 3, improving the SNR to a point where the jitter coming from external sources and from N3 will be dominant and any further improvement in the third term will be irrelevant. Fitting the results from this model to the measured data (in this case, for differential clocking with 3.3-V OV_{DD}, using the curve labeled "SNR Diff 3.3"), we can obtain the constants for Equation 3:

- Adding terms 1 and 2 (we cannot distinguish between them unless other measuring techniques are applied) will give us a total jitter of 300 fs. Given the purity of our sources in the lab, we can assume that all this jitter is coming from the ADS5413 and thus from N3.
- K(N1,N2) will be 160 µV.

The final equation will be

$$(\text{Jitter}_{\text{Total}})^2 = (300\ \text{fs})^2 + \left(\frac{160\ \mu\text{V}}{\text{Clk\_slope}}\right)^2. \qquad \textbf{(4)}$$

Figure 8 and Table 2 compare the result of Equation 4 with the real data.

Note that a clock slope of about 1 V/ns—i.e., a CMOS edge of 3.3 ns—will be sufficient to obtain the maximum performance from our ADC. If the clock is sinusoidal, we will require a peak-to-peak differential clock of about 4 V. With a single-ended clock, 3.3 V_{PP} will be about the maximum we can provide without exceeding the supply rails and turning on the internal protections. Using a differential clock will let us increase the clock amplitude to double that amount. This is one of the advantages of using differential clocking. The other is the rejection of common-mode noise signals. Nevertheless, observe that in Figure 7 the performance of the single-ended clock for small amplitudes is actually slightly better than that of the differential clock. Besides a possible repeatability error between measurements, this could also be due to an imbalance between the two clock lines (a different N1 versus N2), so that the differential clock performance is actually an average of the independent single-ended performances. Another trend to observe is that when the digital output voltage is increased, in this case from 1.8 V to 3.3 V, more switching noise is produced that seems to couple to the clock circuit, as the degradation seems to be smaller at lower input frequencies (see Figure 9, which was adapted from Figure 19 in Reference 4). Finally, note that the clock amplitude has little or no effect on the distortion spurious-free dynamic range.

Figure 7. AC performance vs. clock level

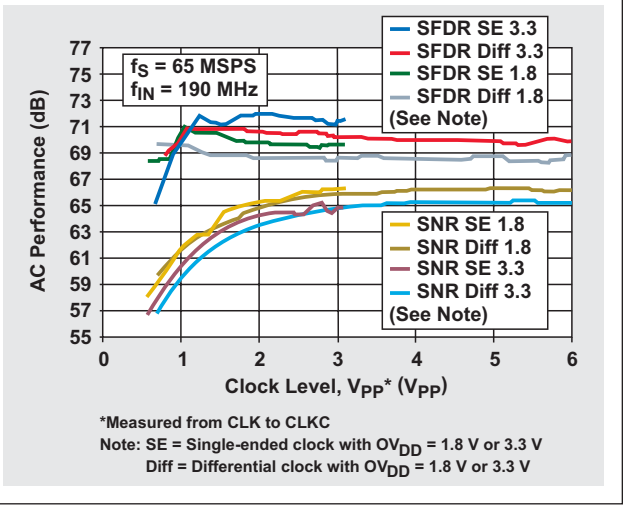


Figure 8. Measured SNR vs. SNR estimated with Equation 4

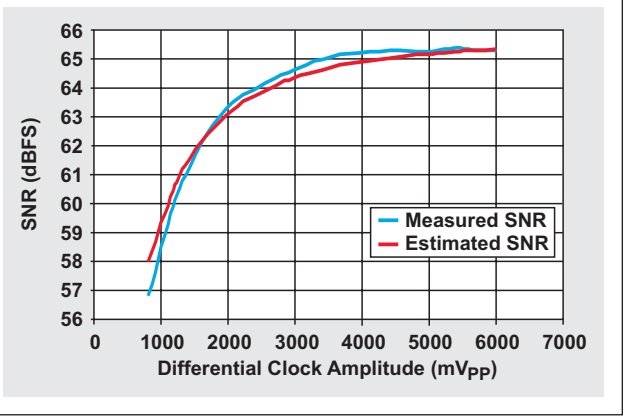


Table 2. Measured SNR vs. SNR estimated with Equation 4

CLOCK (mV_{PP})	MEASURED SNR (dBFS)	ESTIMATED JITTER (ps)	ESTIMATED SNR (dBFS)	SLOPE (V/ns)
820	56.79	1	58.00	0.17
1180	59.95	0.73	60.44	0.24
1380	60.97	0.64	61.35	0.28
1700	62.44	0.55	62.40	0.35
2070	63.47	0.48	63.23	0.42
2400	63.96	0.44	63.74	0.49
2720	64.34	0.41	64.10	0.56
3000	64.59	0.4	64.35	0.61
3420	65	0.38	64.62	0.70
3970	65.21	0.36	64.87	0.81
4570	65.28	0.34	65.06	0.93
5050	65.24	0.34	65.17	1.03
5390	65.39	0.33	65.23	1.10
5680	65.26	0.33	65.27	1.16
6020	65.26	0.33	65.32	1.23

With this new piece of information, we can now go back to Figure 5 and see if we can estimate the SNR degradation as we decrease the sample rate. Using a process similar to the one we used before, we can estimate the coefficients for Equation 3 that will predict the SNR across sampling and input frequencies with less than 1 dB of error:

$$(\text{Jitter}_{\text{Total}})^2 = (250\text{ fs})^2 + \left(\frac{40\ \mu\text{V}}{\text{Clk\_slope}}\right)^2 \quad (5)$$

The result of applying this model can be seen in Figure 10a. Figure 10b shows the original data from Figure 5 for easy comparison.

Following are some implications from this model:

- The SNR degradation at lower f_S seen in Figure 5 occurred because the plot was taken with a fixed 3-V_{PP} sinusoidal clock that reduced the slope on its edges as we decreased its frequency.
- A direct implication of this is that the data sheet actually shows worse performance than what a user could obtain with a different clocking scheme.

Figure 9. SNR vs. input frequency

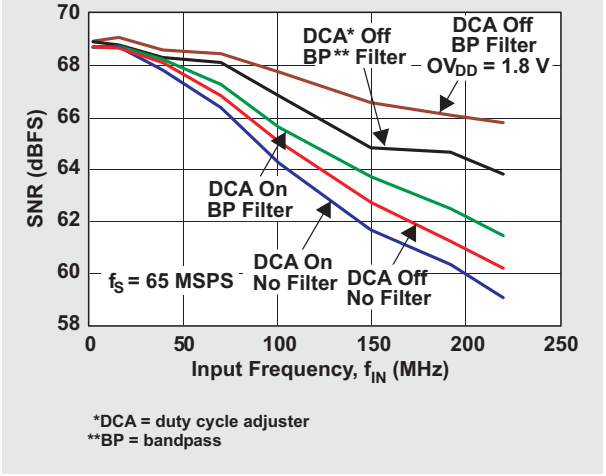
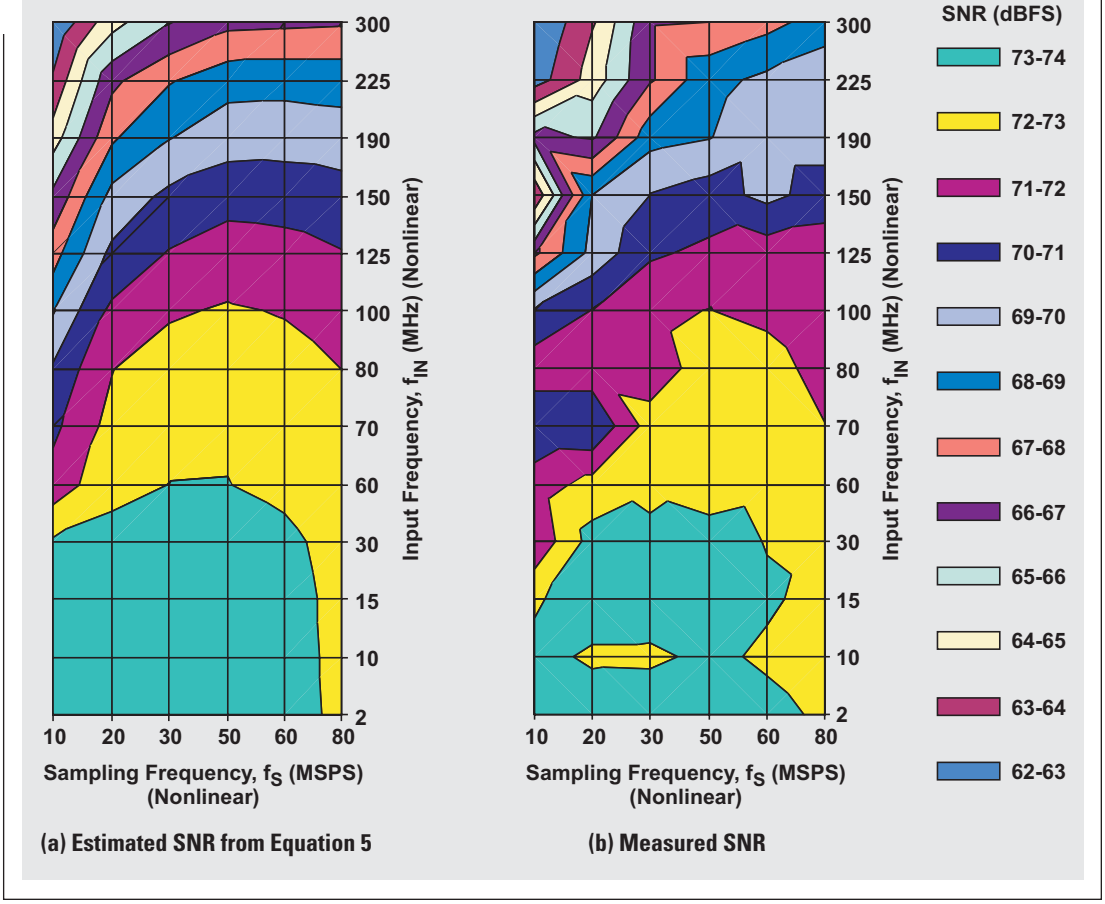


Figure 10. Measured SNR vs. SNR estimated with Equation 5



- A first possible approach is to use a step-up transformer to increase the slope of the sinusoidal clock signal. A pair of clipping diodes (for example, MAX3X71600LCT-ND) can be used to limit the amplitude and avoid exceeding the supply rails of the ADC. This is a clean way of generating a square-like clock signal.
- Another method to square the sinusoidal clock signal is to use an external gate (like a PECL device) acting as a comparator. This minimizes the effect of N1 and N2 but transfers the problem to the equivalent N1 and N2 at the input of the comparator. Many of these commercial circuits have very good jitter numbers, but these numbers stem from the assumption that the input is square; so important degradation could be seen if a sinusoidal clock were used. In many cases the input of the ADC will be a much better squaring circuit than the external gate.
- Ideally we would like to use a very low-jitter clock source with square outputs. One good approximation is the use of a voltage-controlled crystal oscillator (VCXO) with the CDC7005. The use of that circuit will be limited, in principle, by the phase noise quality of the VCXO and some degradation that the CDC7005 may add. Also, this circuit will save a transformer to generate the differential clocking.
- Using an external bandpass filter[3,5] will clean up the jitter on the clock. Nevertheless, the insertion loss of the filter will attenuate the amplitude of the clock, reducing the slope and increasing the effects of N1 and N2. Further amplification (prior to filtering) or a step-up transformer can be used to minimize this attenuation.
- So far we have been estimating jitter indirectly from the SNR degradation, but there could be other reasons for SNR degradation. A method to measure jitter directly on an ADC is described in Reference 5.

Errors in the quantizer

The quantizer will, after the sample-and-hold, take the voltage across the capacitor and convert it into a digital code. As the S&H is holding the signal steady, the exact time to clock the quantizer is not critical. Nevertheless, other problems arise that are related not to jitter but just to pure timing.

One problem is that in a pipeline ADC, usually both phases of the clock (clock high and clock low) are used. Each stage performs a task during half of the clock and another task during the other half. Both tasks are equally important and require at least a minimum time for accurate execution; so the user has to provide a minimum clock duty cycle. Duty-cycle specifications are usually included on the data sheet of the device. Also, some ADCs (such as the ADS5413) have an internal duty-cycle stabilizer that, when enabled, creates the right internal duty cycle from any external clock duty cycle within a certain range.

Another problem, as ADCs become faster and faster, is to squeeze the maximum performance from the timing design. Open-loop designs of the internal clock circuit tend to leave some margin for supply and temperature variations, which at high clock rates means that time that could be used to settle the stage is being left just for a margin. To optimize the timing, closed-loop designs, like delay locked loop (DLL)-based clocks, can be employed. Many users wonder if the jitter of the DLL will affect the performance. Notice in Figure 1 that the DLL is not in the path of the S&H. Nevertheless, the issue is that basic DLL designs have a range of frequencies of operation; so, if they are designed for the higher clocking rates, they will not be able to operate properly at the lower ones. Also, use of the DLL means that the clock is synchronous—i.e., periodic, not burst or pulsed. For applications requiring lower clock rates or asynchronous clocking, the ADS5500 includes the possibility of bypassing the DLL.

References

For more information related to this article, you can download an Acrobat Reader file at www-s.ti.com/sc/techlit/*litnumber* and replace *"litnumber"* with the **TI Lit. #** for the materials listed below.

Document Title	TI Lit. #
1. "14-Bit, 125MSPS Analog-to-Digital Converter," ADS5500 Data Sheet, p. 17	sbas303
2. A. Zanchi, A. Bonfanti, S. Levantino, and C. Samori, "General SSCR vs. cycle-to-cycle jitter relationship with application to the phase noise in PLL," *Proceedings of the 2001 IEEE Southwest Symposium on Mixed-Signal Design* (Austin, TX, Feb. 25–27, 2001), pp. 32–37.	—
3. Alfio Zanchi, "How to Calculate the Period Jitter σ_T from the SSCR $L(f_n)$ with Application to Clock Sources for High-Speed ADCs," Application Note	slwa028
4. "Single 12-Bit, 65-MSPS IF Sampling Analog-to-Digital Converter," ADS5413 Data Sheet, p. 9	slws153
5. A. Zanchi, I. Papantonopoulos, and F. Tsay, "Measurement and Spice prediction of sub-picosecond clock jitter in A/D converters," *Proceedings of the 2003 IEEE International Symposium on Circuits and Systems* (Bangkok, Thailand, May 25–28, 2003), Vol. 5, pp. V-557–V-560.	—

Related Web sites

analog.ti.com

www.ti.com/sc/device/*partnumber*

Replace *partnumber* with ADS5413, ADS5500, ADS5542, or CDC7005

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products	
Amplifiers	**amplifier.ti.com**
Data Converters	**dataconverter.ti.com**
DSP	**dsp.ti.com**
Interface	**interface.ti.com**
Logic	**logic.ti.com**
Power Mgmt	**power.ti.com**
Microcontrollers	**microcontroller.ti.com**
Applications	
Audio	**www.ti.com/audio**
Automotive	**www.ti.com/automotive**
Broadband	**www.ti.com/broadband**
Digital control	**www.ti.com/digitalcontrol**
Military	**www.ti.com/military**
Optical Networking	**www.ti.com/opticalnetwork**
Security	**www.ti.com/security**
Telephony	**www.ti.com/telephony**
Video & Imaging	**www.ti.com/video**
Wireless	**www.ti.com/wireless**

TI Worldwide Technical Support

Internet

TI Semiconductor Product Information Center Home Page
support.ti.com

TI Semiconductor KnowledgeBase Home Page
support.ti.com/sc/knowledgebase

Product Information Centers

Americas

Phone	+1(972) 644-5580	Fax	+1(972) 927-6377
Internet/Email	support.ti.com/sc/pic/americas.htm		

Europe, Middle East, and Africa

Phone			
Belgium (English)	+32 (0) 27 45 54 32	Netherlands (English)	+31 (0) 546 87 95 45
Finland (English)	+358 (0) 9 25173948	Russia	+7 (0) 95 7850415
France	+33 (0) 1 30 70 11 64	Spain	+34 902 35 40 28
Germany	+49 (0) 8161 80 33 11	Sweden (English)	+46 (0) 8587 555 22
Israel (English)	1800 949 0107	United Kingdom	+44 (0) 1604 66 33 99
Italy	800 79 11 37		
Fax	+(49) (0) 8161 80 2045		
Internet	support.ti.com/sc/pic/euro.htm		

Japan

Fax			
International	+81-3-3344-5317	Domestic	0120-81-0036
Internet/Email			
International	support.ti.com/sc/pic/japan.htm		
Domestic	www.tij.co.jp/pic		

Asia

Phone			
International	+886-2-23786800		
Domestic	Toll-Free Number		Toll-Free Number
Australia	1-800-999-084	New Zealand	0800-446-934
China	800-820-8682	Philippines	1-800-765-7404
Hong Kong	800-96-5941	Singapore	800-886-1028
Indonesia	001-803-8861-1006	Taiwan	0800-006800
Korea	080-551-2804	Thailand	001-800-886-0010
Malaysia	1-800-80-3973		
Fax	886-2-2378-6808	Email	tiasia@ti.com
Internet	support.ti.com/sc/pic/asia.htm		ti-china@ti.com

C011905

Safe Harbor Statement: This publication may contain forward-looking statements that involve a number of risks and uncertainties. These "forward-looking statements" are intended to qualify for the safe harbor from liability established by the Private Securities Litigation Reform Act of 1995. These forward-looking statements generally can be identified by phrases such as TI or its management "believes," "expects," "anticipates," "foresees," "forecasts," "estimates" or other words or phrases of similar import. Similarly, such statements herein that describe the company's products, business strategy, outlook, objectives, plans, intentions or goals also are forward-looking statements. All such forward-looking statements are subject to certain risks and uncertainties that could cause actual results to differ materially from those in forward-looking statements. Please refer to TI's most recent Form 10-K for more information on the risks and uncertainties that could materially affect future results of operations. We disclaim any intention or obligation to update any forward-looking statements as a result of developments occurring after the date of this publication.

Trademarks: All other trademarks are the property of their respective owners.

Mailing Address: Texas Instruments
Post Office Box 655303
Dallas, Texas 75265