Application Brief

Solving Power Sequencing Challenges for Ethernet RGMII Communications

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Introduction

Ethernet technology has become the backbone of modern communication and connectivity. This technology is widely used in consumer, industry and automotive domains today. Ethernet is a baseband LAN technology with data transmission rates up to 1 Gbps, so Ethernet can satisfy the need for high-speed communications. There are many types of gigabit Ethernet MII interfaces, among which RGMII is commonly used for its lower pin count and higher bandwidth.

Multiple cores (PHYs, MCUs) in the network are more and more common to enable higher-speed communications. For example, the zone architecture trend in automotive industries accelerates the adoption of Ethernet and has necessitated new requirements to group electronic control units (ECUs) and cabling together into specific domains, as shown in Figure 1. However, power sequencing of multiple power rails for RGMII communications is one of the most critical issues facing multi-core applications, such as a MAC to PHY, multi-PHYs or multi-MACs system.

This paper discusses conventional methods to solve the power sequencing challenges, along with the advantage of using the TI Ethernet RGMII translator TXV0106 and TXV0108 to isolate the power and improve system-level safety and reliability.

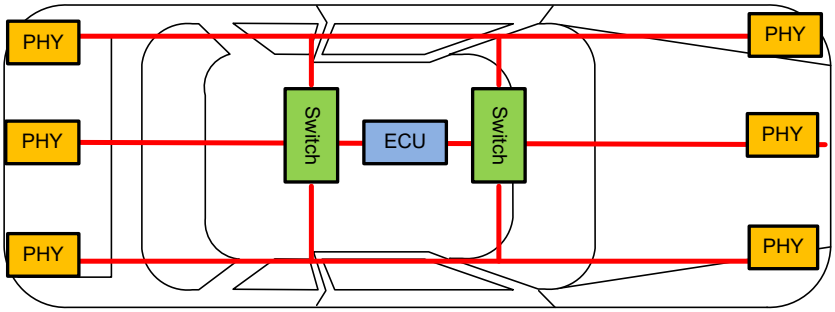

Figure 1. MultiPHY Zone Architecture

Power Sequencing for RGMII

Figure 2 illustrates an example of an Ethernet switch where multiple MACs and PHYs are communicating at the same time. In this kind of multi-core system, starting up or powering down the rails of each domain in a specific order or timing sequence is difficult and often requires additional monitoring and supervising circuit design. Similar challenges also exist in power-consumption sensitive applications where the system designers need selectively power down some cores using load switches when not in use.

During all of these power sequencing events, the IO rails can be powered up before the core blocks or the multichip IO rails are not powered up monotonically. Therefore, the voltage on the IO pins can exceed the supply rails and turn on internal ESD protection diodes, causing in-rush current during power-up. Or in some cases, the forward biased diode can even back-power the supply causing system false turn-on, bus contention or other malfunctions.

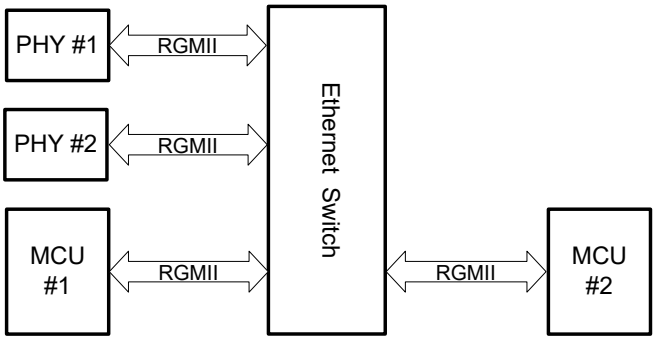

Figure 2. Multicore RGMII Communication

Power Sequencing Solutions

- **Switch-Based Solution**

Figure 3 shows how to use a signal switch to isolate a MCU that is always transmitting and waking up the PHY. The analog switch isolates the signal between MCU and PHY through the power-off control signal of the external LDO. When the PHY is in power-off mode, the switch is OFF and shuts off the signal path. This solution protects the PHY from seeing the input signal before it fully wakes up. However, this option adds cost and size due to routing multiple switches and the extra power-off signal. In addition, it is hard to meet RGMII stringent timing requirements due to part-to-part variations, board routing parasitics, and the tradeoff with turn-on switch resistance.

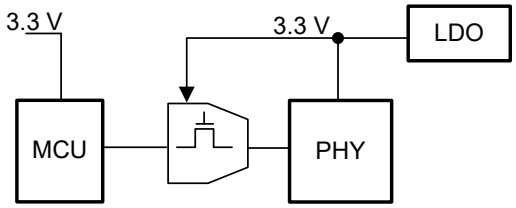

Figure 3. Switch-Based Solution

- **Delay-Based Solution**

Another common solution is to add in an extra delay between two supplies to make sure the supply is always stable before IOs are applied. There are several methods to implement the delay to reduce in-rush current, such as soft start, RC delay, logic gate control, PMIC and so on. Figure 4 shows an example of using a simple RC circuit to create a delay between Power Supply 1 and Power Supply 2.

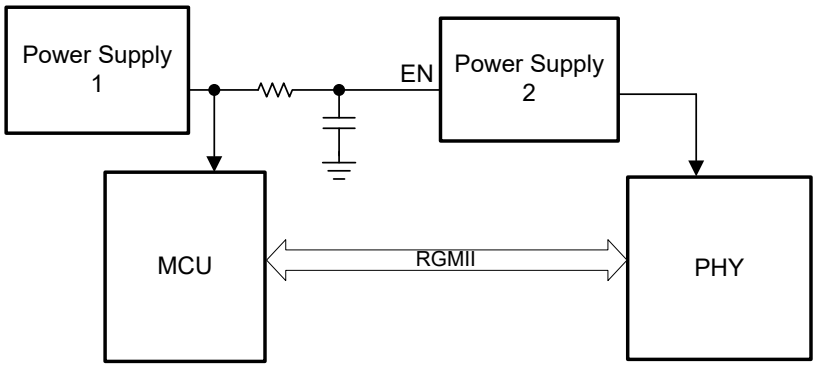

Figure 4. RC Delay-Based Solution

One of the drawbacks of this solution is that the delay accuracy is not assured due to the large variance of discrete R and C components. Another drawback is that the system has to tolerate extra current to charge/

discharge the capacitor at each power-up/power-down cycle. Additionally, all data signals under Power Supply 2 are "forced" to follow the same RC delay, which in some cases is not acceptable.

- **Voltage Translation Solution Using TXV010x**

Voltage translator is well known for level shifting between different IO voltages. However, in many cases, voltage translator is a cost-effective and reliable solution to provide power isolation during power sequencing. For example, the TI TXV010x family (TXV0106 and TXV0108) not only meets strict RGMII 2.0 timing specs (that is, Ch-ch skew, rise/fall time and duty cycle distortion), but also solves the power sequencing challenges with three built-in features.

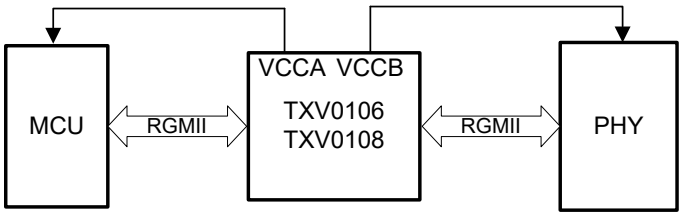

Figure 5. Voltage Translation Option (TXV Family)

1. IOFF

IOFF feature (also called "partial-power-down" or "back-drive protection") ensures that all I/O pins enter a high-impedance state when any of the supplies (VCCA or VCCB) is held at 0 V. This feature eliminates leakage current even if I/O voltage goes higher than the supply voltage, and reduces the system-level static current when some of the PHYs or MACs enter Standby mode. This static-current limitation also allows the insertion or removal of a PHY into a multicore Ethernet system without interrupting the host core.

2. VCC Disconnect

The VCC disconnect feature further improves the system roboustness. It ensures that if any supply floats after ramping to high, the device brings it to the ground and makes the output Hi-Z. This feature protects the system from uncontrolled current flowing due to floating supplies.

3. Glitch-free power up/down

The glitch suppression feature removes power-up and power-down IO glitches before the IO cells are fully activated. TXV010x family has glitch suppression circuitry and IO Hi-Z circuitry controlled by a power-on reset (POR) block. This feature maintains that the IO ports are in high impedance until both supplies have reached a certain threshold required for operation. The POR design has built-in hysteresis to avoid oscillations during a slow ramp to further improve reliability at various power sequencing events. Extensive power sequencing for various power-up and power-down scenarios, which are typically expected in the system, are tested for the TXV010x family to provide reliable operation.

Conclusion

Today’s complex Ethernet systems have the MAC/FPGA/PHY operating at multiple voltage nodes that require power isolation during sequencing. In this application brief, different power sequencing solutions are discussed. TI’s latest RGMII translators (TXV0106 and TXV0108) have the partial-power–down (IOFF) feature, the VCC disconnect feature and the glitch-free power-up and power-down feature. These features provide system-level flexibility and safety under various sequences by avoiding in-rush current, a back-power fault, glitches and excessive IO leakage current. Using the TXV010x family solves power sequencing challenges for high-speed RGMII communications while achieving a cost, size and performance optimized system-level design.

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