User's Guide

Input Resistance Error for Current Sense Amplifiers

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ABSTRACT

Resistive loading at the input pin (IN+ and IN-) and bias or reference pins (REF) of current sense amplifiers (CSA) can create significant error (e_{EXT}) in the output measurement; however, this error can be calculated and managed to acceptable levels for low-accuracy, low-cost, or small form factor applications.

In this guide, CSAs with resistance at input and reference pins are designed, and tested over temperature. Two types of devices are tested. One device is a standard linear CSA (INA185) and the other device is a capacitively-coupled, high-input impedance CSA (INA191). Both devices are tested with and without input resistance over temperature to determine and verify the error generated solely from the input resistance.

Table of Contents

Trademarks

1 Introduction

Most current sense amplifiers (CSA) have input resistances much lower than similarly closed-loop instrumentation (in-amps) and difference amplifiers. This is primarily because of the non-isolated connections to the inputs pin, but also due to the input bias stage in between input pins. Thus, CSAs ideally should have little to no external input resistances (R_{EXT} < 10Ω) at input pins; however, certain applications may require higher R_{EXT} and thus it becomes crucial to understand and calculate worst-case error to see if circuit still meet system requirements.

In recent years, capacitively-coupled input current sense amplifiers (for example, INA190 or INA191) can present much higher effective differential resistances in the range to 2MΩ to 5MΩ over temperature.

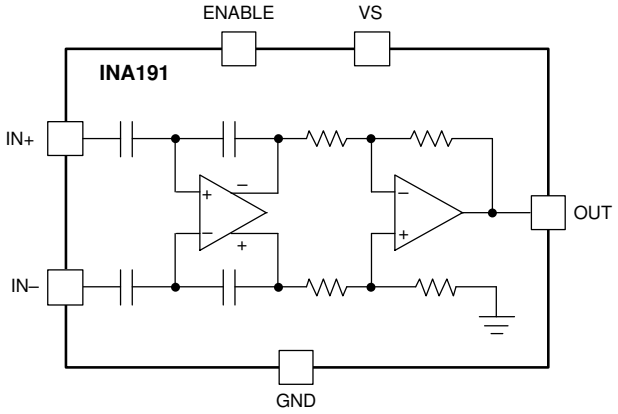


Figure 1-1. Simplified INA191 Functional Block Diagram

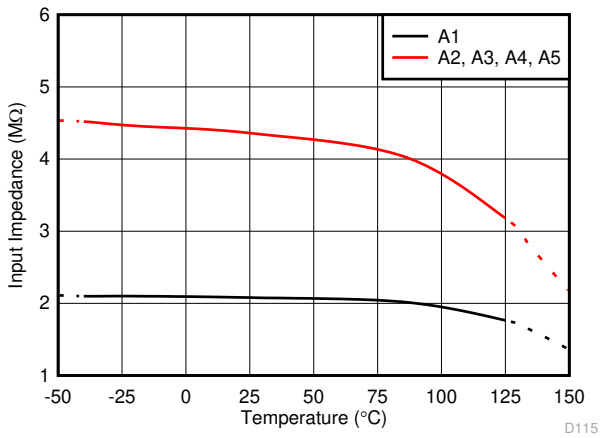


Figure 1-2. INA191 Differential Input Resistance Over Temperature

These devices can easily measure lower current in the micro-Amps range and also maintain high accuracy with larger input resistors. Note that capacitively-coupled input amplifiers often require some differential input capacitance at the input pins whenever significant external impedance is present. This is to help provide charge to internal switching capacitors.

The other important input loading resistance for most CSAs and difference amplifiers is the reference voltage source resistance (R_{EXT3}). Reference (REF) pins allow the output of bidirectional CSAs to be biased to voltage when the measuring 0-V differentially. System design cost and complexity can be reduced by simply driving REF pins with a resistor divider as opposed to a low-impedance source. However, all error sources and loss of dynamic range must be considered and bounded. For a detailed analysis of error generated from loading REF pins, refer to *Driving Voltage Reference Pins of Current-Sensing Amplifiers*, application note.

Overall, higher input impedance devices can be more accurate with external loading; however with only a few specifications of process variation, a system designer using a CSA with R_{EXT} >10Ω can achieve manageable error targets in low-accuracy, but low-cost and small PCB systems. This document shows how to calculate the bounds of this input resistance over temperature. In many cases a one-point, offset calibration is most practical.

2 CSAs and Input Bias Stage

The input bias stage allows CSAs to operate with supply voltages (V_S) independent of input common-mode voltage (V_{CM}). For most devices, the input bias stage has a resistance (R_{BIAS}) in between input pins ranging from 2kΩ to 72kΩ. This resistances creates an effective differential bias current ($I_{B,\ Differential}$) that is proportional to the input differential shunt voltage.

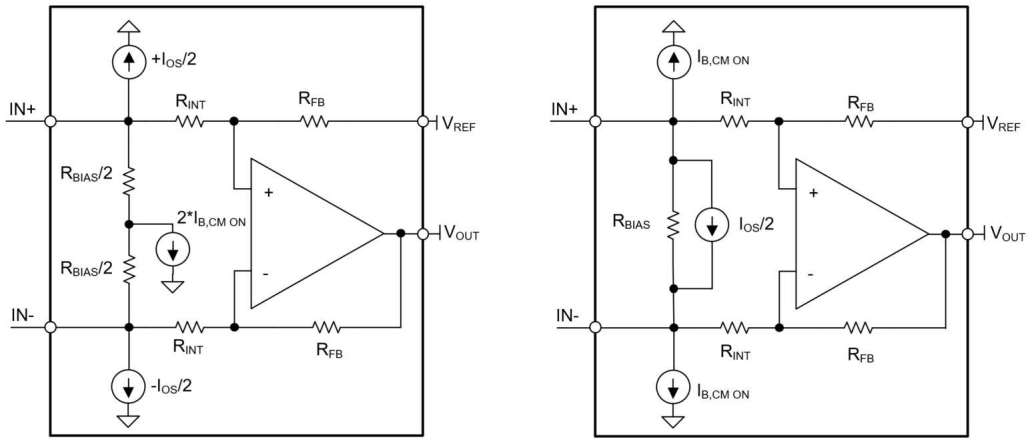


Figure 2-1. Simplified Equivalent Models of Single Stage Current Sense Amplifier With Input Bias Stage

Within the input bias stage is circuitry that monitors the V_{CM} to appropriately turn on a bias current ($I_{B,\ CM\ ON}$). This usually occurs when V_{CM} exceeds V_S or some proportional value (check data sheet). For example with the single-stage CSA, INA185, a large jump in total input bias current occurs when V_{CM} exceeds the 5V supply voltage.

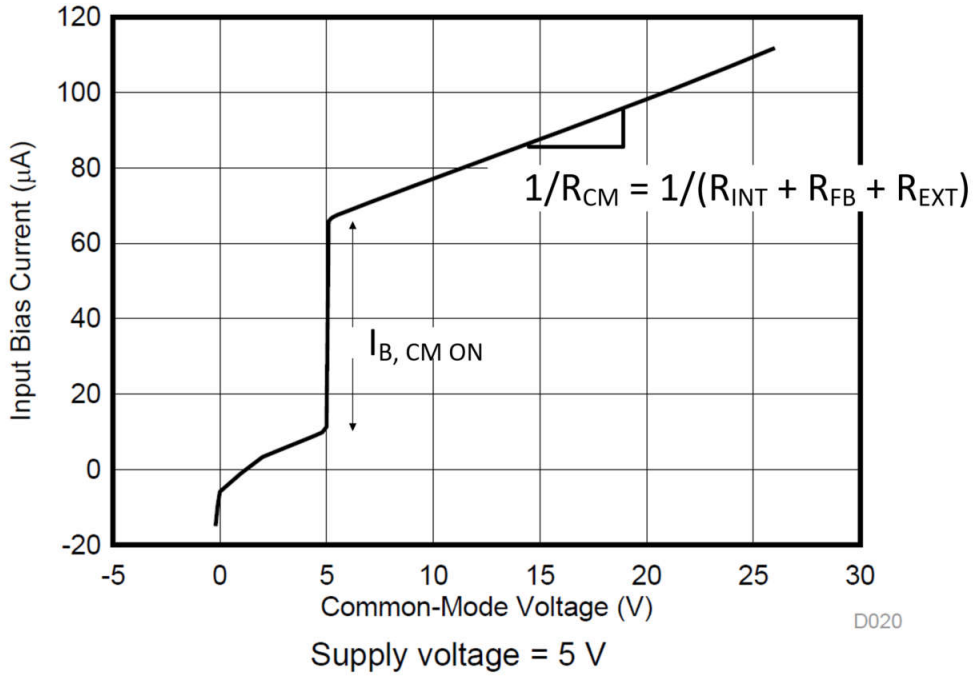


Figure 2-2. Input Bias Current vs Input Common-Mode Voltage for INA185

Aside from this shift, the total $I_{B,\ CM}$ is the general leakage current ($I_{B,\ Leakage}$) from bus voltage at input pins to the reference voltage at REF pin. Thus the total input bias current for each input pin is the summation of common-mode leakage from bus to reference, $I_{B,\ CM\ ON}$, and the differential current through R_{BIAS}.

$$I_{B,\,Leakage} = \frac{V_{CM} - V_{REF/BIAS}}{R_{INT} + R_{FB} + R_{EXT}} \quad (1)$$
$$I_{B,\,Total} = I_{B,\,Leakage} + I_{B,\,Differential} + I_{B,\,CM\,ON}$$

Note for two-stage CSAs, the $I_{B,\,Leakage}$ is determined by difference between V_{CM} and the internal bias voltage (V_{CM2}) in between first and second stage; however, please defer to the input bias current data plots in data sheets as current pathway can be more complex.

Understanding input bias currents is important as input bias determine offset error from external input resistance ($V_{OS,\,EXT}$).

3 CSA and Gain Error Factor

The typical device gain shown in data sheets for a single-stage, differential CSA is simply the matched ratio of R_{FB} over R_{INT} as shown in Equation 2.

$$Gain_{typical} = {}^{R_{FB,\,typical}}/_{R_{INT,\,typical}} \quad (2)$$

When using input resistors ($R_{EXTERNAL}$ or R_{EXT}), the total shunt voltage gain ($Gain_{TOTAL}$) becomes predictably attenuated due to a Gain Error Factor (GEF) that is less than 1. This new attenuated gain can be theoretically calculated using Equation 3. This total shunt voltage gain is now the new typical gain of the circuit. Note equations for a device's GEF are usually provided in data sheet.

$$Gain_{Total,\,typical} = Gain_{typical} \times GEF_{Typical} \quad (3)$$

When introducing an input GEF, there is a new way to reference input offset voltages. Normally, the initial offset error specified in the data sheet (V_{OSI}) is referred to the input (RTI), but to refer it to the shunt (RTS), you need to divide by the GEF. This also applies to the derivation of $V_{OS,\,EXT\,RTI}$ shown at end of document.

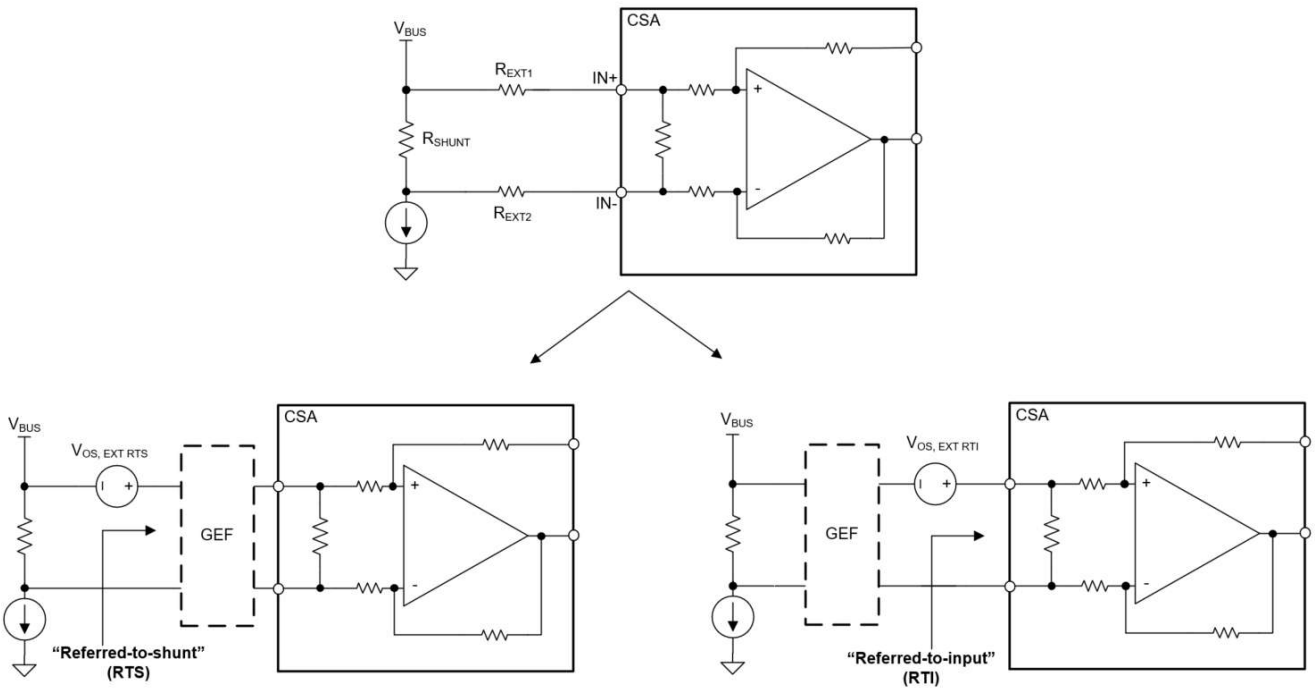


Figure 3-1. RTI (Referred-to-input) and RTS (Referred-to-shunt) for CSA with Input Resistors

$$V_{OS\,EXT\,RTS} = {}^{V_{OS\,EXT\,RTI}}/_{GEF} \quad (4)$$
$$V_{OSI\,RTS} = {}^{V_{OSI\,RTI}}/_{GEF}$$

Once the new typical total gain is determined, the designer can shift (calibrate) the shunt voltage gain in system hardware or software. However, there can be a significant increase in gain error variation ($E_{G, EXT}$) over system population due to the fact that internal resistors are designed to achieve accurate ratios (Device Gain = R_{FB}/ R_{INT}), not accurate absolute values.

For most CSAs, conservative evaluations put the absolute process variation (PV) of these resistors at ±20% and with temperature coefficients (PV_TC) of ±30 ppm/°C. These are based upon the specifications of the process technology. Furthermore, error analysis is simplified by the fact that all internal resistors for a single device can inherently have the same PV and PV_TC. With these PV specifications defined, a designer can calculate the bounds of external resistance loading error (e_{EXT}).

4 Applications for Resistance at Input Pins of Current Sense Amplifiers

Table 4-1 is a non-comprehensive list of applications and reasons why a system needs resistors at the input pins (IN+ and IN-) for a current sense amplifier.

Table 4-1. Applications for Using Current Sense Amplifier (CSA) with Input Resistors

Application Type	Application Benefits
Input differential (V_{SHUNT}) filtering with input C_{DIFF} capacitor as shown in Figure 4-1	1. Filters out current noise and/or transient spikes 2. Allows for use of low-distortion NPO/C0G C_{DIFF} capacitor, thus a more precise cutoff frequency (f_C)
Input common-mode voltage (V_{CM}) filtering (with input C_{CM} capacitors). See Figure 4-2.	1. Attenuates a periodic bus or fast V_{CM} transient, which reduces device output error/ disturbances. 2. Using higher R_{EXT} (thus lower C_{CM}) helps reduce capacitive load on the bus rail. 3. Note: When using C_{CM} on input pins, the advise is to also use a C_{DIFF}>10*C_{CM} to help reduce C_{CM} settling imbalances. 4. Note: This is not recommended for PWM applications requiring high BW and fast settling times. Using a CSA with enhanced PWM rejection circuitry (for example, INA241 or INA240) is the recommended amplifier for these applications.
Input current limiting for input V_{CM} violation events: ESD fast-transient or DC electrical overstress (EOS). See Figure 4-3.	1. Protects device from damage by limiting current of amplifier input ESD cell activation and/or input latch up pathway 2. Limits current of external protection clamping diodes, which reduces required diode power dissipation. 3. *Transient Robustness for Current Shunt Monitor*, reference design.

For Figure 4-1, the input filter cutoff frequency is $f_{C,differential} = 1 / (2 \times PI \times 2 \times R_{FILTER} \times C_{DIFF})$.

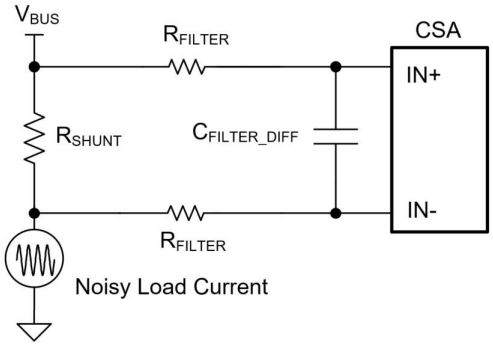


Figure 4-1. Current Sense Amplifier with Input Differential Filter

For Figure 4-2, the input filter cutoff frequency is $f_{C,differential} = 1 / (2 \times PI \times 2 \times R_{FILTER} \times (C_{DIFF} + C_{CM} / 2))$.

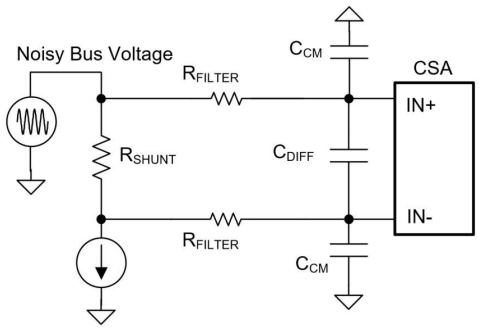


Figure 4-2. Current Sense Amplifier With Input Common-Mode Filter

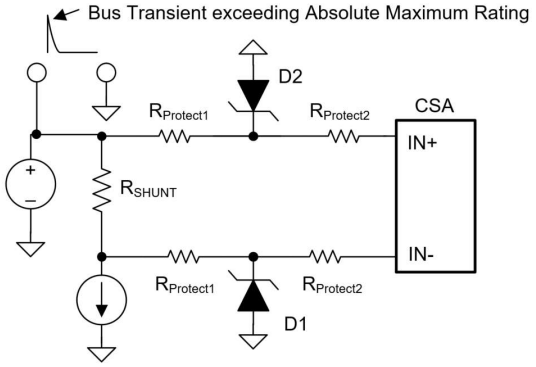


Figure 4-3. Current Sense Amplifier With Input Protection Diode Clamps and Resistors

4.1 Input Resistance Design Considerations

Whenever using large input resistance (>10-Ω) at CSA input pins, the system engineer can determine what the maximum allowable errors are at the minimum and maximum sense current levels, calculate the theoretical error with input resistors, and then make following considerations:

1. Is the new (attenuated) typical circuit gain sufficient?
2. Is the new gain error range within maximum allowable error over temperature?
3. Is the new offset error within maximum allowable error at I_{LOAD_MIN}?
4. If error at I_{LOAD_MIN} is too high, can offset error be calibrated out with 1-point calibration?
   a. Can a small V_{REF} (approximately 100mV) be used to simplify this calibration?
   b. Is there enough dynamic range left when providing this V_{REF}?
5. If the error from input resistance is still too high, can a high-input impedance device such as the INA190, INA191, or INA186 be used instead?

5 Applications for Input Resistance at Reference Pins of Current Sense Amplifiers

5.1 Bidirectional CSA and Applications

As an overview, any CSA that has a reference (REF) pin is considered bidirectional. The majority of applications that require a bidirectional CSA are shown in Table 5-1.

Table 5-1. Applications that Require CSA Reference Pin

Application Type	Application Benefit for V_{REF}>0
Load current is bidirectional (positive and negative)	Allows for measurement of entire positive and dynamic range.
Load current is unidirectional and pulse-width modulated (PWM)	V_{OUT} remains in linear region when load is at 0A, thus avoiding output delays and/or distortion.
System requires a fast one-point offset calibration procedure	V_{OUT} remains in linear region when load is at 0A, thus calibration procedure can occur when load is disabled (0A).

While the primary purpose of biasing a CSA output is to measure bidirectional current, another important application is the fast acquisition of unidirectional pulse-width modulated (PWM) currents that start at 0A. When any amplifier is starting from 0mV input or lower and V_{REF}=0, then V_{OUT} is starting the response in saturation, which can cause output distortion, overload recovery delays, and slow down amplifier response and settling times. Simply providing a small reference voltage (usually ≥ 100mV) to position the output into linear operating region can restore the device BW into specification at the expense of losing some output dynamic range.

The other important purpose for providing a reference voltage is to simplify a one-point offset calibration. One-point offset calibration procedures require one point of data and the easiest data point to use is when signal current = 0A (load disabled). Negating offset error can significantly reduce low current sensing error and thus increase accurate dynamic range.

A host's single-ended ADC can record and store into memory V_{OUT} when load is off to calibrate out the tolerance of V_{REF} as well as device offset.

A differential or pseudo-difference ADC can measure the output differentially ($V_{OUT, differential}$), which is V_{OUT} with respect to the reference pin (V_{REF}). This allows system to negate error in V_{REF} without needing to perform calibration because the resulting output measurement is the differential input multiplied by device gain. Error can be further minimized by performing a one-point calibration to calibrate the amplifier's offset.

5.2 Driving CSA Reference Pin With High-Resistance Source Voltage

Normally, the reference pins are driven with low-impedance (< 10Ω) voltage sources or buffers to prevent loading down the resistor feedback network. However, certain system applications can require external loading resistance as listed in Table 5-2.

Table 5-2. Applications for Driving Reference Pin with High-Resistance Source Voltage

Application Type	Application Benefit
Using a resistor divider off a voltage supply rail (usually V_S)	Reduces system cost and BOM
Using an RC low-pass filter to reduce noise or overshoot of reference voltage source	Reduces measurement noise, especially for single-ended ADC measurements. Reduces capacitive loading onto the V_{REF} source

Input resistance at device reference/bias pins can create significant single-ended error, but much of the error can be negated simply by measuring the differential output voltage ($V_{OUT, differential}$), which is V_{OUT} with respect to the reference pin (V_{REF}), and/or performing a one-point system calibration. For a detailed analysis of the error generated from loading REF pins, refer to this *Driving Voltage Reference Pins of Current-Sensing Amplifiers* application note.

5.3 Input Resistance at Reference Pin Design Considerations

Whenever using large input resistance (>10-Ω) at CSA reference pins, the system engineer can follow Section 8 and make following considerations:

1. Is the reduced dynamic range large enough for required system dynamic range?
2. If ADC must be single-ended, can system perform 1-point offset calibration to negate V_{REF} tolerance and CSA input offset?
3. Can ADC make a differential/pseudo-differential measurement to negate V_{REF} variation without need for 1-point calibration?
   a. Furthermore, can differential ADC and system perform a 1-point calibration to negate CSA input offset error?
4. How much can the input V_{CM} change? For single-stage CSAs, as V_{CM} changes so can the effective V_{REF} voltage since current can flow from V_{CM} through input pins and to the REF pin. Thus, a fluctuating V_{CM} of even a few volts can further reduce dynamic range.

6 Design Procedure and Error Calculation for External Input Resistance on CSA

When using a single-stage, difference CSA and determining input external resistance error, follow the procedure below.

1. Determine what the system's maximum and minimum ambient temperatures is and use Equation 6 to determine worst-case temperature change from the standard 25°C testing condition ($\Delta T_{A, MAX}$).
2. Using data sheet information determine the typical (or nominal) values of the internal resistors for CSA's first stage (R_{BIAS}, R_{INT}, and R_{FB}).
   a. Note that typical process values assume T_A = 25°C and PV = 0%
3. Also identify values for bias turn on currents ($I_{B, CM\ ON}$) and input offset current (I_{OS}).
   a. $I_{B, CM\ ON}$ can be determined by calculating the vertical shift in $I_{B, CM}$ as shown in Figure 2-2.
   b. Assuming ±20% variation in this values is a conservative approximation.
4. Using Equation 8 and Equation 3, calculate the new typical attenuated gain ($Gain_{TOTAL, typical}$) assuming typical process variation (PV = 0%) for R_{BIAS}, R_{INT}, and R_{FB}, nominal tolerance (e_{REXT} = 0%) for R_{EXT}, and nominal device gain error (E_G = 0%).
   a. Note: Equation for GEF is usually provided in the data sheet.
5. Calculate the worst-case maximum and minimum resistance values of all resistors using Equation 7 and Equation 9.

a. Note that the tolerance error for any internal resistance (e.g., R_{FB}) is the process variation (PV) value. Additionally, the temperature coefficient (TC) for any internal resistance is the process value's temperature coefficient (PV_TC).
b. Note for the calculation of R_{INT} with Equation 9, incorporating the maximum device's internal gain error ($E_{G, MAX}$) generates a very conservative total gain error approximation. However, given the statistical independence between resistor matching (E_G) and resistor tolerance (PV), it is also fair to simply let E_G = 0%, but add $E_{G, MAX}$ later during a final root sum square error calculation, $E_{G,\,Total} = \sqrt{E_{G,MAX}{}^2 + E_{G,EXT}{}^2}$.
   i. To simply calculate the gain error caused by the external resistors ($E_{G, EXT}$), set E_G =0% for equation Equation 9.

6. Calculate the total maximum (positive) gain ($Gain_{MAX}$) and minimum (negative) gain ($Gain_{MIN}$) at 25° (ΔT_A = 0°) using equation set Equation 10 where the inputs and conditions for function Equation 8 are noted.
   a. Maximum gain occurs when:
      i. R_{BIAS}, R_{INT}, and R_{FB} are maximum (positive) tolerance and drift
      ii. R_{EXT} is at minimum (negative) tolerance and drift
   b. Minimum gain occurs when:
      i. R_{BIAS}, R_{INT}, and R_{FB} are minimum (negative) tolerance and drift
      ii. R_{EXT} is at maximum (positive) tolerance and drift
7. Using equation set Equation 11, calculate the new maximum and minimum gain errors at 25°C *relative to the new attenuated shunt voltage gain* determined in step 4.
8. Calculate maximum and minimum gains ($Gain_{Total, MAX}$ and $Gain_{Total, MIN}$) at the maximum temperature swing ($\Delta T_A = \Delta T_{A, MAX}$) using equation set Equation 10.
   a. Calculate the gain errors relative to the $Gain_{Total, typical}$ using Equation 11
9. Calculate gain error drift $E_{G, EXT\ drift}$ in parts per million per degrees Celsius (ppm/°C) using equation Equation 12.
   a. Note that gain error drift cannot remain constant over process variation.
   b. Note that these equations can use any two temperatures for T_{A1} and T_{A2}, although choosing them at 25°C and 25°C+$\Delta T_{A, MAX}$ is most convenient given these gain errors have already been calculated.
10. Calculate the maximum (positive) offset ($V_{OS\_EXT, MAX\ RTI}$) and minimum (negative) possible offset ($V_{OS\_EXT, MIN\ RTI}$) due to R_{EXT} at 25°C (ΔT_A = 0°) using Equation 13 with conditions defined by Equation 14.
    a. Using the same conditions, calculate the GEF using Equation 16 and convert RTI offsets into RTS using Equation 4.
    b. See Section 11 at end of this document on how this equation was derived.
11. Calculate the maximum (positive) offset ($V_{OS\_EXT, MAX\ RTI}$) and minimum (negative) possible offset ($V_{OS\_EXT, MIN\ RTI}$) due to R_{EXT} at maximum temperature swing ($\Delta T_A = \Delta T_{A, MAX}$) using function Equation 13 with conditions defined by Equation 14.
    a. Using the same conditions, calculate the GEF using Equation 16and convert RTI offsets into RTS using Equation 4.
12. Calculate input offset drift due to R_{EXT} using Equation 15
13. Calculate total system error
    a. $$E_{Total} = \sqrt{E_{G,MAX}{}^2 + E_{G,EXT}{}^2 + \left(\frac{V_{OS,\,Device}}{V_{SHUNT}}\right)^2 + \left(\frac{V_{OS,\,EXT}}{V_{SHUNT}}\right)^2 + \left(\frac{V_{OS,\,Device\,Drift}}{V_{SHUNT}}\right)^2 + \left(\frac{V_{OS,\,EXT\,Drift}}{V_{SHUNT}}\right)^2} \quad (5)$$
    b. Note that device's input offset (V_{OSI}) and drift specification are referred to the input (RTI). Thus these values need to be referred to the shunt using Equation 4.
    c. If a one point calibration is performed, then offset components at 25°C can be removed.

Error Equations for Resistance at Input Pins of Single-Stage Current Sense Amplifier

$$\Delta T_{A,\,max} = MAX\{T_{A,\,high} - 25°C,\ 25°C - T_{A,\,low}\} \quad (6)$$

$$R_{MAX} = R_{NOMINAL}\left(1 \pm e_{tolerance}\right)\left(1 \pm \Delta T_{A,MAX} \times TC_R\right) \quad (7)$$

$$GEF = \frac{\frac{R_{BIAS}}{2} \times R_{INT}}{\frac{R_{BIAS}}{2} \times R_{EXT} + \frac{R_{BIAS}}{2} \times R_{INT} + R_{EXT}} \quad (8)$$

$$R_{INT,\,MAX} = \frac{R_{FB,\,MAX}}{Gain_{Device,\,typical} \times \left(1 + E_{G,\,MAX}\right)} \quad (9)$$

$$R_{INT,\,MIN} = \frac{R_{FB,\,MIN}}{Gain_{Device,\,typical} \times \left(1 + E_{G,\,MIN}\right)}$$

$$GEF_{MAX} = GEF\begin{cases} PV = maximum \;\; (e.g., \;\; +20\,\%) \\ PV\_TC = maximum \;\; (e.g., \;\; +30 \;\; ppm/^{\circ}C) \\ e_{R_{EXT}} = minimum \;\; (e.g., \;\; -1\,\%) \\ TC_{R_{EXT}} = minimum \;\; (e.g., -50 \;\; ppm/^{\circ}C) \\ E_G = typical \;\; (e.g., \;\; 0\,\%) \end{cases} \quad (10)$$

$$GEF_{MIN} = GEF\begin{cases} PV = minimum \;\; (e.g., \;\; -20\,\%) \\ PV\_TC = minimum \;\; (e.g., \;\; -30 \;\; ppm/^{\circ}C) \\ e_{R_{EXT}} = maximum \;\; (e.g., \;\; +1\,\%) \\ TC_{R_{EXT}} = maximum \;\; (e.g., +50 \;\; ppm/^{\circ}C) \\ E_G = typical \;\; (e.g., \;\; 0\,\%) \end{cases}$$

$$Gain_{Total,\,MAX} = \left(Gain_{Device} = \frac{R_{FB}}{R_{INT}}\right) \times \left(GEF_{MAX}\right)$$

$$Gain_{Total,\,MIN} = \left(Gain_{Device} = \frac{R_{FB}}{R_{INT}}\right) \times \left(GEF_{MIN}\right)$$

$$E_{G,\,EXT\,MAX} = \frac{Gain_{Total,\,MAX} - Gain_{Total,\,typical}}{Gain_{Total,\,typical}} \quad (11)$$

$$E_{G\,EXT,\,MIN} = \frac{Gain_{Total,\,MIN} - Gain_{Total,\,typical}}{Gain_{Total,\,typical}}$$

$$E_{G\,Drift,\,EXT\,MAX} = \frac{E_{G,\,MAX\,T_{A,2}} - E_{G,\,MAX\,T_{A,1}}}{T_{A,2} - T_{A,1}} \times 10^6 \quad (12)$$

$$E_{G\,Drift,\,EXT\,MIN} = \frac{E_{G,\,MIN\,T_{A,2}} - E_{G,\,MIN\,T_{A,1}}}{T_{A,2} - T_{A,1}} \times 10^6$$

$$V_{OS,\ EXT\ RTI} = \frac{\left(V_{REF} - V_{BUS}\right)\left(1 - C_{EV}\right) + I_{B,CM\ ON}\left(R_{SH} + R_{EXT2} - R_{EXT1}C_{EV}\right) - \frac{I_{OS}}{2}\left(R_{SH} + R_{EXT2} + R_{EXT1}C_{EV}\right)}{1 + \left(R_{SH} + R_{EXT2}\right)\left(\frac{1}{R_{INT}} + \frac{1}{R_{BIAS}}\right) + \frac{R_{EXT1}C_{EV}}{R_{BIAS}}} \quad (13)$$

$$C_{ev} = \frac{1 + \frac{R_{SH} + R_{EXT2}}{R_{FB} + R_{INT}}}{1 + \frac{R_{EXT1}}{R_{FB} + R_{INT}}}$$

$$V_{OS,\ EXT\ MAX} = V_{OS,\ EXT}\begin{cases} PV,\ PV\_TC = minimum \\ I_{B,CM\ ON},\ V_{CM} = maximum \\ V_{REF} = minimum \\ I_{OS} = minimum \\ R_{EXT2} = maximum \\ R_{EXT1} = minimum \end{cases} \quad (14)$$

$$V_{OS,\ EXT\ MIN} = V_{OS,\ EXT}\begin{cases} PV,\ PV\_TC = minimum \\ I_{B,CM\ ON},\ V_{CM} = maximum \\ V_{REF} = minimum \\ I_{OS} = maximum \\ R_{EXT2} = minimum \\ R_{EXT1} = maximum \end{cases}$$

$$V_{OS,\ EXT\ Drift\ MAX} = \frac{V_{OS,\ EXT\ MAX\ at\ T_{A,2}} - V_{OS,\ EXT\ MAX\ at\ T_{A,1}}}{T_{A,2} - T_{A,2}} \quad (15)$$

$$V_{OS,\ EXT\ Drift\ MIN} = \frac{V_{OS,\ EXT\ MIN\ at\ T_{A,2}} - V_{OS,\ EXT\ MIN\ at\ T_{A,1}}}{T_{A,2} - T_{A,2}}$$

$$Let\ \ C_{EG} = \frac{R_{EXT1}}{R_{FI} + R_{EXT1}} \quad (16)$$

$$\frac{V_{OS,\ EXT\ RTI}}{V_{SH}} = GEF = \frac{1}{\left(1 + \frac{R_{EXT2}}{R_{INT}}\right) + \frac{R_{EXT1} + R_{EXT2}}{R_B} - \frac{C_{EG}\left(R_{EXT1} - R_{EXT2}\right)}{R_B}}$$

$$V_{OS,\ EXT\ RTS} = \frac{V_{OS,\ EXT\ RTI}}{GEF}$$

6.1 Calculating e_{EXT} for INA185A4 With 110Ω Input Resistors

Use the previous equations to perform an analysis on a hypothetical circuit with the INA185A4 with 110Ω resistors (R_{EXT}) at input pins. Consider the following circuit parameters:

Table 6-1. Required Device and Circuit Parameters To Calculate e_{EXT}

Parameter	Nominal Value	Tolerance	Drift (ppm/°C)
V_S	5V	0%	0
V_{CM}	12V	0%	0
$T_{A, Max}$	100°C	N/A	N/A
R_{SH}	1mΩ	0.1%	± 50ppm/°C
R_{EXT}	110Ω	0.1%	± 20ppm/°C
R_{FB}	500kΩ	Process Variation (PV) ± 20%	Process Variation Temperature Coefficient = ± 30ppm/°C
R_{INT}	2.5kΩ		
R_{BIAS}	2.5kΩ		
I_{OS}/2 Max	± 225nA	0	± 10
$I_{B, CM ON}$	58µA	20%	± 157ppm/°C
$Gain_{Device}$	200V/V	0.25%	± 8ppm/°C
$Gain_{Total, Typical}$	176.67844523V/V	Variable	Variable

Most of the fundamental circuit parameters needed are found in data sheet. However there is some calculation and estimation needed for I_{OS} and $I_{B, CM ON}$.

Typical I_{OS} is usually very small; however, this can increase for any ratio mismatch between the R_{BIAS}/2 resistors seen in Figure 2-1 and mismatch between the R_{INT} and R_{FB} resistors on the positive (non-inverting) and negative (inverting) branches of the internal amplifier network.

As stated previously, matching of resistors ratios is very small, but can be conservatively approximated by device's typical gain error of ±0.25%. Using this information, one can simulate the ideal amplifier network and measure maximum I_{OS} by setting all resistors in one branch to +0.25% and in the other branch set to -0.25%. For V_{CM} = 16V, I_{OS} is 450µA. Since all resistors will have the same drift, I_{OS} drift will be fairly low and simply approximated as 10ppm/°C. If a one-point calibration is performed, then error from I_{OS} will be negated. Please contact TI support for more information if necessary.

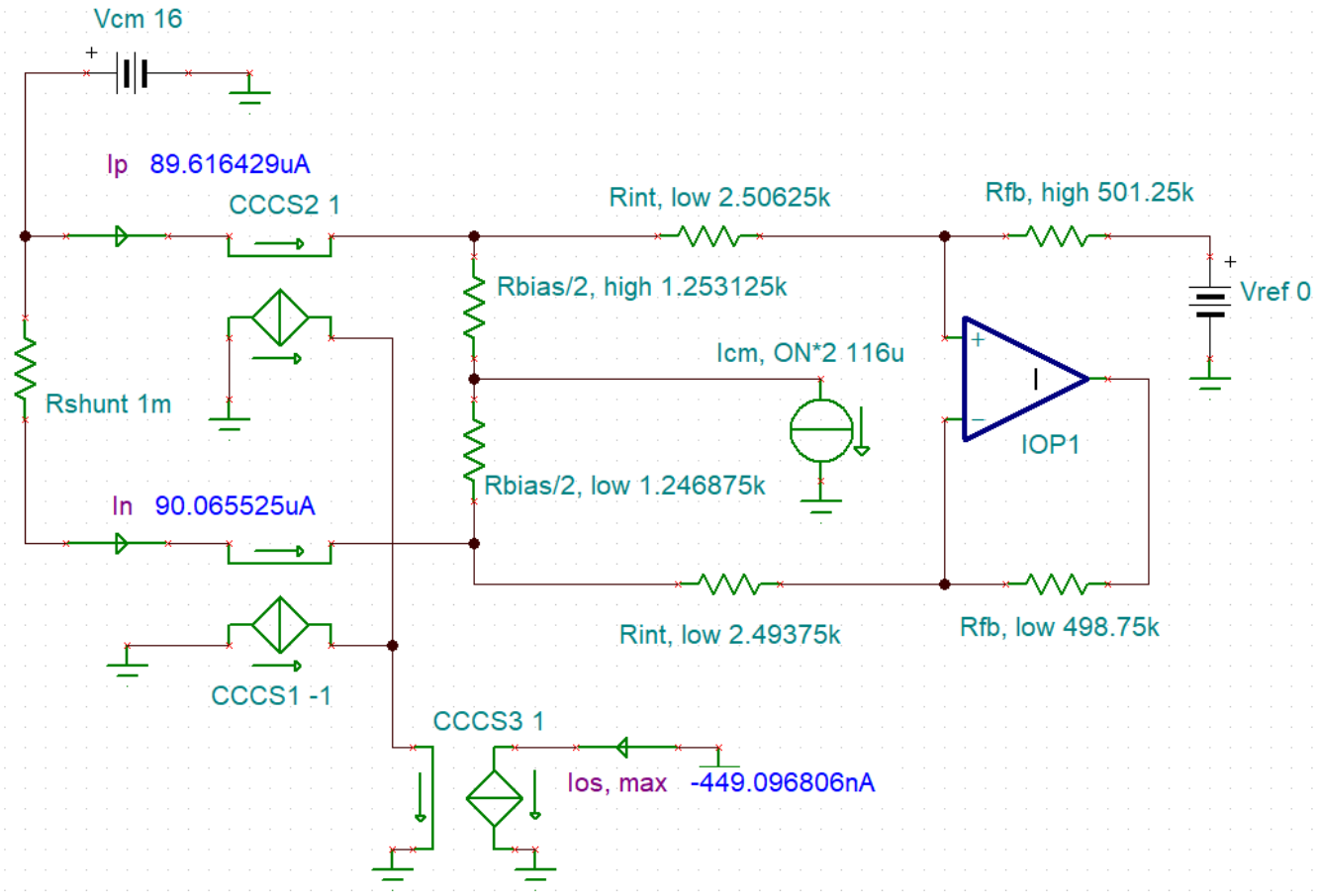


Figure 6-1. Worst-Case I_{OS} For Single-Stage CSA

For $I_{B, CM\ ON}$, the typical value is simply the jump in $I_{B, CM}$ as shown in Figure 2-2. Tolerance can be approximated as process variation. Drift can be deduced by $I_{B, CM}$ versus temperature data plots in data sheet. For the INA185, the data sheet shows a 2µA change in $I_{B, CM}$ from -40°C to 125°C. Assume this value is 3µA and you can determine drift in ppm/°C as:

$$I_{B,\ CM\ ON}\ \ Drift\ = \pm 10^6 \times \frac{\Delta I_{B,\ CM} \times 0.5}{\Delta T_A} \times \frac{1}{I_{B,\ CM\ ON}} \tag{17}$$

Lastly temperature dependencies in V_S and especially V_{CM} need to be considered as these can add to the offset drift, which cannot be calibrated.

The calculated e_{EXT} values at 25° and maximum ambient temperature are shown in Table 6-2.

Offset Values are Referred-to-Shunt (RTS) Using Worst-Case GEF at 125°C

Table 6-2. Maximum Offset and Gain Errors and Drift for INA185A4 with 110Ω (0.1%, 20ppm/°C) Input Resistors at V_{CM} = 12V and V_{REF}=140mV

	T_A (°C)	High	Low
$V_{OS,\ EXT\ Max}$ (µV)	25 °C	71.45	-71.25
	125 °C	115.82	-115.62
$E_{G,\ EXT\ Max}$	25 °C	1.99209%	-2.84638%
	125 °C	2.04245%	-2.91539%
$E_{G\ EXT,\ Drift}$ (ppm/°C)		5.057	-6.902
$V_{OS\ EXT,\ Drift}$ (µV/°C)		0.442	-0.444
$V_{OS,\ EXT\ Calibrated,\ 25°C}$ (µV)		44.37	-44.37

Note that worst-case $V_{OS, EXT}$ occurs when PV = -20%.

Table 6-3 shows offset values for both RTI and RTS along with the GEF used to convert them. The RTI values match the V_B measurement in simulation of the circuit as well shown in Figure 6-2.

Table 6-3. $V_{OS, EXT\ Max}$ Value in Both RTI and RTS with GEF

	T_A	High	Low
$V_{OS, EXT\ Max\ RTS}$	25 °C	71.45	-71.25
	125 °C	115.82	-115.62
$V_{OS, EXT\ Max\ RTI}$	25 °C	61.32	-71.25
	125 °C	99.36	-99.21
GEF	25 °C	0.85832855	0.85840965
	125 °C	0.85788132	0.85812512

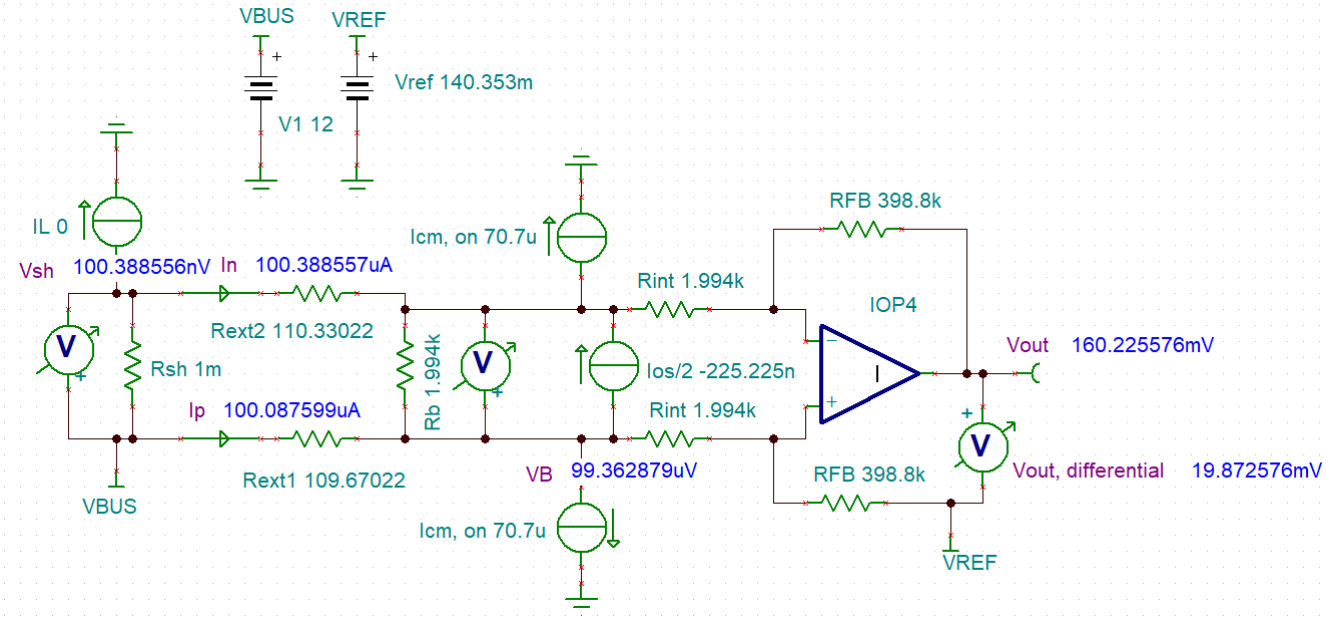


Figure 6-2. Simulation of Example at 125°C

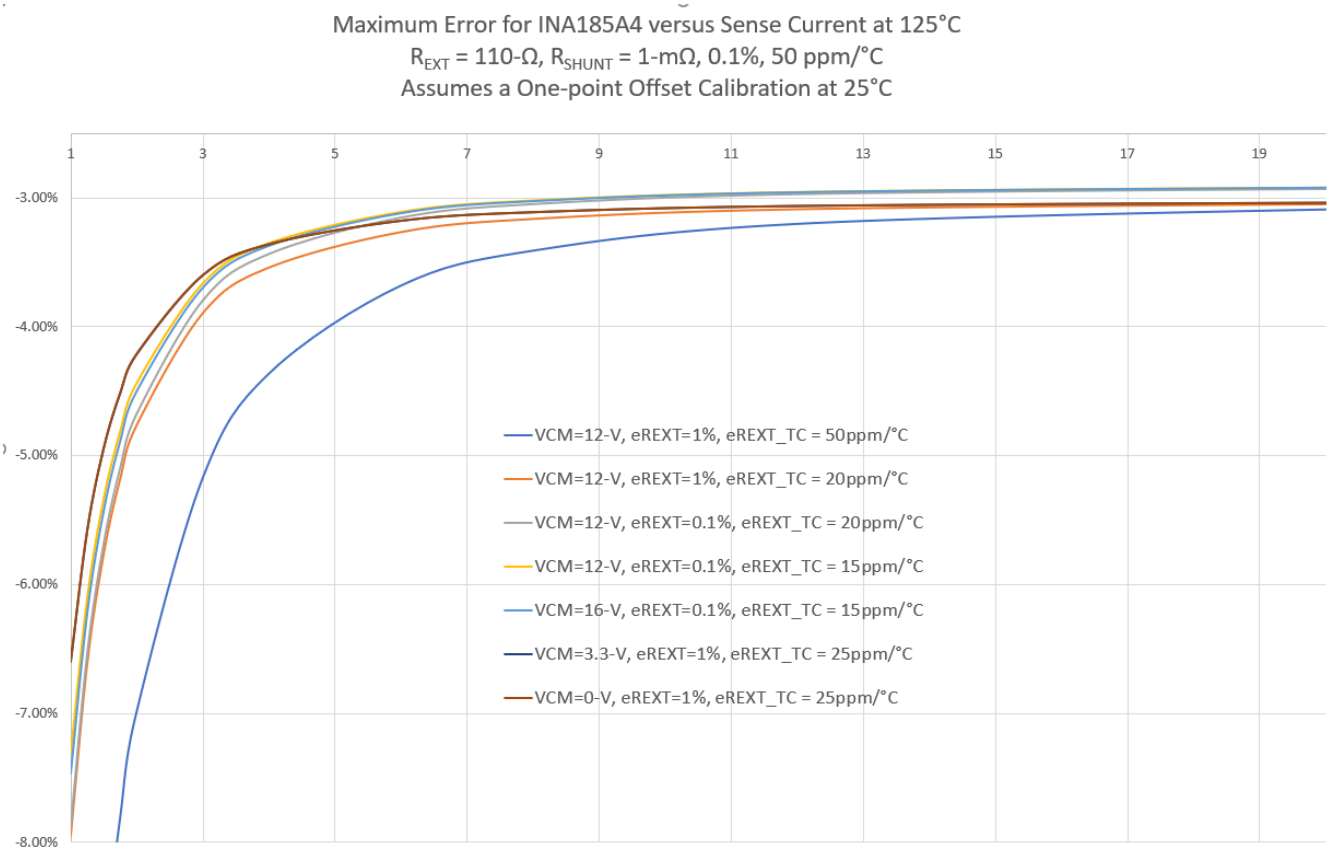


Figure 6-3. Total Error Comparisons with One-Point Offset Calibration at 25°C

7 Design Procedure for Input Resistance on Capacitively-Coupled Current Sense Amplifier

When using R_{EXT} >100-Ω with the INA190 or similar CSA with capacitive-coupled input, the procedure for determining the error is outlined in the following.

1. Based upon the maximum possible operating temperature, determine the input differential resistance (R_{DIFF}) values at the nominal operating temperature (25°C) and maximum ($T_{A, high}$) and minimum temperatures ($T_{A, low}$).
   a. This data plot (for example, Figure 1-2) can be available in the data sheet.
2. Calculate GEF for each temperature using the equation provided in data sheet as shown in Equation 18.
   a. Calculate $E_{G, EXT}$ at each temperature as 1-GEF
3. Using values from step 2, calculate the drift in external loading gain error using Equation 19.
   a. Note $E_{G, EXT}$ can decrease significantly at increasing temperatures so try to choose two values that correspond linearly the best with the roll-off in gain.
4. The new typical circuit gain at 25°C needs to be calculated using Equation 3.

$$GEF_{Capacitive-Coupled} = \frac{R_{DIFF}}{R_{DIFF} + R_{SH} + 2 \times R_{EXT}} \quad (18)$$

$$E_{G\,Drift,\,EXT\,High-Nominal} = \frac{E_{G\,EXT,\,T_{A,\,High}} - E_{G\,EXT,\,T_{A,\,Nominal}}}{T_{A,\,High} - T_{A,\,Nominal}} \times 10^6 \quad (19)$$

$$E_{G\,Drift,\,EXT\,Low-Nominal} = \frac{E_{G\,EXT,\,T_{A,\,Low}} - E_{G\,EXT,\,T_{A,\,Nominal}}}{T_{A,\,Low} - T_{A,\,Nominal}} \times 10^6$$

7.1 Bench Verification of Input e_{EXT} for Capacitively-Coupled Current Sense Amplifiers

Determining input resistive loading error, especially for offset and drift is not currently a theoretical procedure and does require a bench verification due to the highly non-linear impedance of internal switching capacitors. The general procedure is straightforwad, in that the engineer can sweep V_{OUT}/V_{IN} over temperature without and with R_{EXT} (and a stabilizing C_{DIFF}) and calculate total gain, offset and drift errors using standard linear interpolation. The error generated solely from R_{EXT} is calculated by calculating the change in total errors.

There are two methods a designer can use to understand the realistic error to expect.

Method 1 - Sweep Input with Precision Differential Voltage Source

This method requires emulating the shunt resistor's voltage drop (V_{SHUNT}) with a precision DC voltage source (V_{IN}) capable of accurately driving milli-volts. Additionally, this source can have a 4-wire force and sense capability.

While this can seem the simplest approach, there is a downside concerning the inductance of long input wires going into the CSAs input pins (IN+ and IN-). As noted, a capacitively-coupled CSA can have complex capacitive switching network at it front end. These capacitors can be constantly charging and discharging with current supplied from the bus. The average current is small (nano-Amps), but the peak transient input bias current can be larger.

Any input inductance can load down these capacitors and create delays causing significant device error. Usually this is not a problem because the input traces from R_{SHUNT} to CSA input pins is not long enough to generate significant inductance. Additionally, inductive loading can be negated with a small input differential capacitor (C_{DIFF}) as shown in Figure 4-1.

Overall, if using this method make sure the V_{IN} source is a 4-wire force and sense connection and that CSA has a C_{DIFF} > 1-nF potentially more depending on how long cabling is and how high the ambient temperature is.

Method 2- Sweep Input with a Monitored Current Source and Calibrated Shunt Resistor

This method is the actual sensing of current across a soldered down shunt resistor with soldered down CSA circuit. It requires more effort up front, but can achieve more precise results. Also, it does not require negating input pin cable inductance because input traces can be small on realistic PCB.

The downsides with this method is it requires knowing the approximate shunt resistor (R_{SHUNT}) to be used in system and being able to solder it onto the CSAs EVM or prototype system PCB.

Another challenge is having an accurate ammeter to measure load directly. If testing requires larger currents, consider using precision shunt that is temperature controlled and monitored with accurate voltmeter.

Load current can be controlled simply with a variable resistor or rheostat pulling current from a stand voltage source emulating the bus voltage. Electric current sources, which can be more precise, can be used if desired and available

One convenient advantage with this method is that the shunt resistor does not need to be measured for gain calibration because external loading error (e_{EXT}) is delta in error from R_{EXT}=0-Ω to R_{EXT}>0-Ω.

If engineer chooses to measure R_{SHUNT} over temperature for gain calibration and accurate understanding of circuit error, then R_{SHUNT} can first be soldered down onto the PCB and measured with a precision 4-wire, Ohm-meter at the nominal, maximum, and minimum operating system ambient temperatures. Care needs to be taken for measurements to settle. Additionally, any resistance in parallel (including the CSA can be removed/ negated) so the R_{SHUNT} measurement is not affected. Once R_{SHUNT} is calibrated, you can negate its tolerance by calculating .

$$V_{IN} = R_{SHUNT,\ CAL} \times Load_{Measured} \quad (20)$$

8 Design Procedure for Input Resistance at CSA Reference Pins

When CSAs have external input resistance at the REF pin, the designer must confirm that the reduced dynamic range of CSA output can still meet system requirements. This requires considering all possibilities of resistor tolerance, CSA process variation, bus voltage variation, and supply voltage (Vs), if using a resistor divider of Vs pin.

1. Before the analysis, understand what are the maximum and minimum bounds of the linear operating range of V_{OUT}, as well as, how are these bounds are further constrained by device output voltage noise.
   a. $V_{OUT, MAX} = V_{OUT, MAX\ linear} – V_{OUT, noise\ pk\text{-}pk}/2$
   b. $V_{OUT, MIN} = V_{OUT, MIN\ linear} + V_{OUT, noise\ pk\text{-}pk}/2$
      i. Usually $V_{OUT, MAX\ linear}$ can be 100mV below output's swing to supply voltage.
      ii. Usually $V_{OUT, MIN\ linear}$ can be 100mV above output's swing to ground.
2. For each PV corner, examine all 4 possible worst-case Ra and Rb combination at maximum temperature swing (assume the PV corner can have both PTC and NTC).
   a. Calculate the designed for reference voltage value $V_{REF\_x} = V_S \times R_a || R_b$
   b. Calculate the effective input resistance (Rx = Ra||Rb).
3. For each combination, calculate the effective reference voltage ($V_{REF\_EFFECTIVE}$) using Equation 21 as shown outlined in the following *Driving Voltage Reference Pins of Current-Sensing Amplifiers*, application note.
   a. $$V_{OUT\_error} = m\left(-V_{REF\_x} + V_{CM} + {V_{DIFF}}/{2}\right)$$ (21)
      $$V_{REF,\ EFFECTIVE\ Predicted} = V_{REF\_x} + V_{OUT\_error}$$
   b. Note that if the CSA has external input resistors at input pins, then R_{EXT} needs to be added to in-series with R_{INT}.
   c. Assume maximum possible V_{CM}.
4. Determine the worst-case maximum and minimum $V_{REF\_EFFECTIVE}$
   a. Maximum $V_{REF\_EFFECTIVE}$ usually occurs at -PV, -PV_TC, minimum Ra, and maximum Rb.
   b. Minimum $V_{REF\_EFFECTIVE}$ usually occurs at +PV, +PV_TC, maximum Ra, and minimum Rb.
5. Confirm the circuit's measurable dynamic range at maximum temperature swing. For each PV corner:
   a. Determine the worst-case total RTI offset $\pm(V_{OS, EXT\ RTI} + V_{OS, RTI})$
   b. Calculate the device's worst-case gain error.
   c. Calculate the worst-case V_{OUT} at no load (V_{OUT_0A}) with $V_{OUT\_0A} = \pm V_{OS, total} * Gain + V_{REF\_EFFECTIVE, MAX/MIN}$
      i. Usually the maximum $V_{OUT\_0A, MAX}$ occurs at minimum PV/PV_TC, maximum $V_{OS, Total}$, and maximum $V_{REF\_EFFECTIVE}$.
      ii. Usually the minimum $V_{OUT\_0A, MAX}$ occurs at maximum PV/PV_TC, minimum $V_{OS, Total}$, and minimum $V_{REF\_EFFECTIVE}$.
   d. Determine measurable current assuming a differential measurement of output
      i. $I_{Measurable, low} = (V_{OUT, MIN} - V_{OUT\_0A, MIN})/(Gain_{Typical} * R_{SHUNT})$
      ii. $I_{Measurable, high} = (V_{OUT, MAX} - V_{OUT\_0A, MAX})/(Gain_{Typical} * R_{SHUNT})$

9 Input Resistance Error Test with INA185 Over Temperature

A characterization of the INA185A4 was performed to quantify and verify the error generated by input resistance at both input pins (e_{EXT}) and reference pins ($e_{REF,EXT}$) over temperature.

9.1 Schematic

An INA185A4 evaluation module (EVM) was used along with high temperature cables, precision instrumentation, and an insulated temperature chamber. The test setup is shown in Figure 9-1.

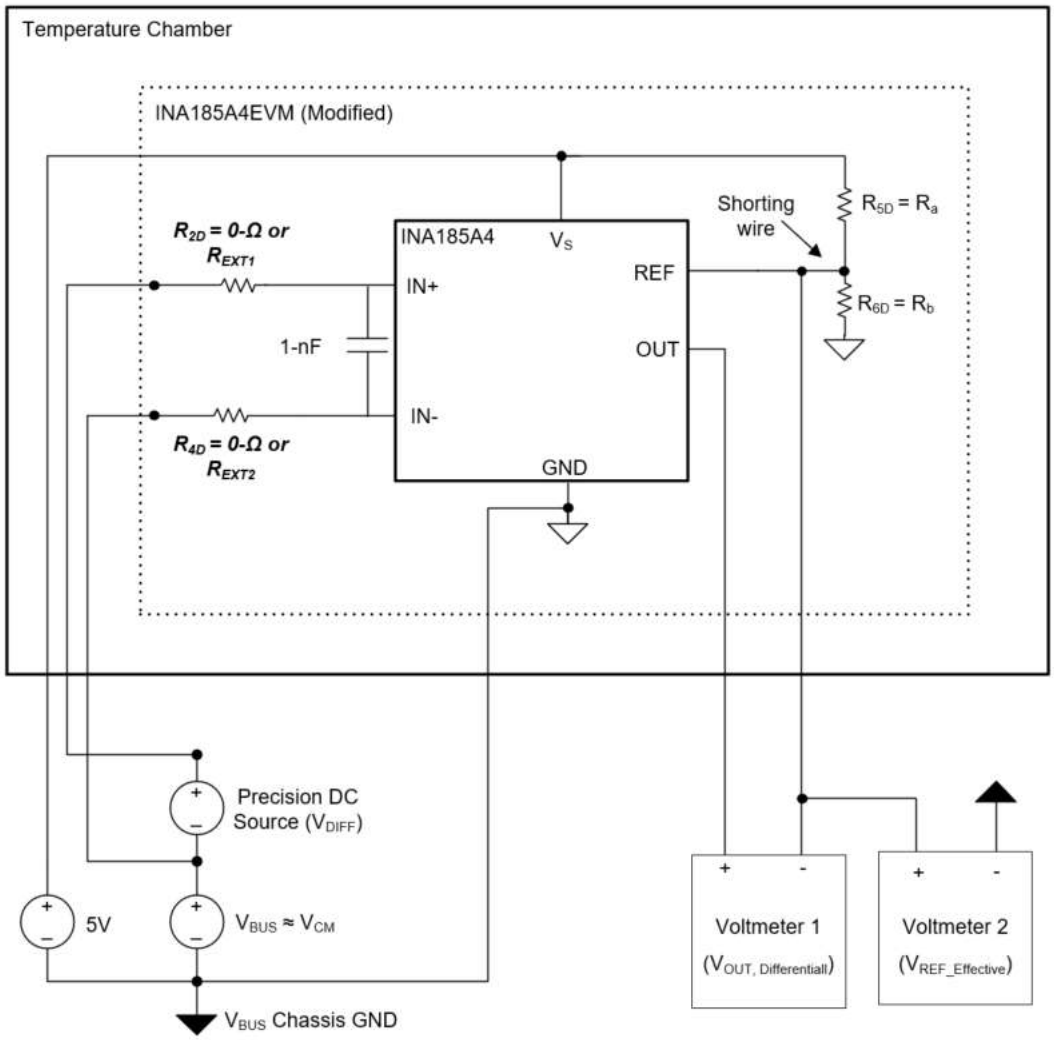


Figure 9-1. Test Setup to Measure External Resistance Error with INA185A4

9.2 Methods

The input resistors chosen for the input pins (R_{EXT1} at IN+ and R_{EXT2} at IN-) were 110Ω resistors along with a differential 1nF input capacitor (C_{DIFF}). For the references pins, an approximate 150mV reference voltage was generated with a 49.9kΩ (Ra) and 1.5kΩ (Rb) resistor divider off the V_S pin as shown in Table 9-1.

Table 9-1. BOM for INA185A4EVM Modifications

Name (EVM Designator)	Value	Tolerance	Drift	Package
C_{DIFF} (C5D)	1nF	1%	C0G, NP0	0603
R_{EXT1} (R2D), R_{EXT2} (R4D)	110Ω	1%	50ppm/°C	0603
Ra (R5D)	49.9kΩ	1%	50ppm/°C	0603
Rb (R6D)	1.5kΩ	1%	50ppm/°C	0603

Errors generated from input resistance and reference resistance were distinguished from each other by measuring differential output along with monitoring reference voltage simultaneously.

Input-Output sweeps were run on the EVM at -40°C, 25°C, and 125°C ambient temperatures first with R_{EXT} = 0Ω and then with R_{EXT} = 110Ω. V_{OUT} was monitored to remain with device's linear output operating region. Linear output region for INA185 is defined at 0.75V < V_{OUT}<4.9V. Additionally, at 125°C, the V_{CM} was swept to measure common-mode rejection (CMR).

Data analysis begins by calculating the total shunt voltage gain using a best-fit line method on all of the $V_{OUT, Differential}$ and the V_{DIFF} values within the designated linear output region. For each V_{DIFF}, an input offset is calculated using linear interpolation with the calculated gain. The final V_{OS} chosen for analysis is the average of all individual offsets pertaining to designated linear output region.

Exact external input resistance errors ($E_{G, EXT}$, $V_{OS, EXT}$, $E_{G\ DRIFT, EXT}$, $V_{OS\ Drift, EXT}$, and $CMRR_{EXT}$) quantified by simply calculating the error difference with and without input resistances.

The loading error to the REF pin ($e_{REF, EXT}$) is also considered. The measured reference pin ($V_{REF\_EFFECTIVE}$) is compared against a theoretical value using Equation 21 from related *Driving Voltage Reference Pins of Current-Sensing Amplifiers*, application note. Review this note for more understanding on how these equations were derived.

Errors are compared against a predicted model that uses equations found in Section 6.

9.3 Theoretical Model

Data is checked against a potential theoretical model of the device using equations from Section 6. Although, nearly impossible to back calculate internal device parameters from measured data given many possible combination of error sources, data checks were performed here to verify equations.

First, circuit conditions and all resistors tolerances and drifts were set as shown in Table 9-2.

Table 9-2. Circuit and Device Parameters for Prediction Model

	Value	Tolerance	ppm/°C
$I_{B, CM\ ON}$ (A)	5.80E-05	3.00%	300
I_{OS} (A)	-5.00E-08	-3.00%	10
PV (%)	0%	-0.45%	-25
R_{EXT1} (Ω)	110	0.23%	33
R_{EXT2} (Ω)	110	0.12%	30.3
Ra (Ω)	4.99E+04	-0.200%	30
Rb (Ω)	1500	0.300%	25

Next, theoretical values of resistors and constants were calculated for each temperature. All values were calculated using equations from Section 6. The total predicted gain ($G_{Total, predicted}$) was calculated by multiplying the GEF of modeled internal resistors and the measured device gain. Note that the GEF found in Equation 22 was used.

$$G_{Total,\ predicted} = \left(Gain_{CSA,\ Measured} = \frac{R_{FB}}{R_{INT}}\right) \times GEF \quad (22)$$

Table 9-3. Prediction Model Resistors and Constants Over Temperature

T_A (°C)	-40	25	125
R_{EXT1} (Ω)	110.0165073	110.253	110.6168349
R_{EXT2} (Ω)	109.915095	110.132	110.4657
R_{BIAS} (Ω)	2492.794219	2488.75	2482.528125
R_{INT} (Ω)	2493.504306	2490.022268	2483.970779
R_{FB} (Ω)	498558.8438	497750	496505.625
I_{OS} (A)	-4.8468E-08	-4.8500E-08	-4.8549E-08
$I_{B, CM\ ON}$ (A)	5.8575E-05	5.9740E-05	6.1532E-05

Table 9-3. Prediction Model Resistors and Constants Over Temperature (continued)

T_A (°C)	-40	25	125
$G_{Device, Measured}$(V/V)	199.9430451	199.8978107	199.883843
CEG	0.000219523	0.000220352	0.000221633
$G_{Total, predicted}$(V/V)	176.5801647	176.4662982	176.3379943
CEV	0.999999798	0.999999758	0.999999697
$V_{OS, EXT predicted}$	-2.64999E-06	-4.18505E-06	-6.62529E-06

Lastly, the prediction model was finished by calculating variable external resistances at the REF pin. Error constants c and m are dependent upon R_{EXT} and thus two values are calculated for each R_{EXT}. The parameters here have the same terminology and follow the same equations as this *Driving Voltage Reference Pins of Current-Sensing Amplifiers*, application note.

Table 9-4. Prediction Model Parameters for $e_{EXT, REF}$

T_A (°C)	-40	25	125
Ra (Ω)	49703.08961	49800.2	49949.6006
Rb (Ω)	1502.055188	1504.5	1508.26125
Rx (Ω)	1457.993799	1460.38084	1464.053195
Vref_x (V)	0.146670339	0.146623994	0.146553043
c	0.002909863	0.00291936	0.002934036
m	0.00290142	0.002910862	0.002925452
c (R_{EXT} = 110Ω)	0.002909224	0.002918717	0.002933385
m (R_{EXT} = 110Ω)	0.002900785	0.002910223	0.002924806

Note that this theoretical models only assume linear resistor temperature coefficients; when realistically the temperature coefficient can be highly non-linear. Thus the model was tuned to get best matching to the data for change in ambient temperature from 25°C to 125°C.

9.4 Data for INA185A4 with 110Ω Input Resistors

V_{CM} = 12V

Table 9-5. Input-Output Sweep with INA185A4 and R_{EXT} = 0Ω

V_{DIFF} (mV)	V_{REF} (V)			$V_{OUT, Differential}$ (V)		
	-40°C	25°C	+125°C	-40°C	25°C	+125°C
-0.5	0.18129	0.18114	0.18094	-0.10265	-0.102	-0.10124
0	0.18129	0.18114	0.18094	-0.00266	-0.002	-0.00131
12	0.18133	0.18118	0.18998	2.397	2.396	2.397
23	0.18136	0.18121	0.18101	4.596	4.595	4.596
23.5	0.18136	0.18121	0.18101	4.696	4.696	4.696
23.75	0.18136	0.18121	0.18101	4.745	4.745	4.7459

Table 9-6. V_{OUT} versus V_{CM} with INA185A4 and R_{EXT} = 0Ω at 125°C

V_{DIFF} (mV)	V_{CM} (V)	V_{REF} (V)	$V_{OUT, Differential}$ (V)
23	15	0.18988	4.59534
23	9	0.17213	4.59674
23	25	0.21948	4.59294
23	0	0.14555	4.59945

V_{CM} = 12V

Table 9-7. Input-Output Sweep with INA185A4 and R_{EXT} = 110Ω

V_{DIFF} (mV)	V_{REF} (V)			$V_{OUT, Differential}$ (V)		
	-40°C	25°C	+125°C	-40°C	25°C	+125°C
-0.8	0.18132	0.18115	0.18096	-0.14397	-0.1438	-0.14342
-0.75	0.18132	0.18115	0.18097	-0.13515	-0.1349	-0.13463
-0.6	0.18131	0.18115	0.18097	-0.1087	-0.1085	-0.10818
-0.5	0.18132	0.18115	0.18097	-0.09107	-0.0909	-0.09054
-0.25	0.18132	0.18115	0.18097	-0.04695	-0.0468	-0.04649
0	0.18132	0.18115	0.18097	-0.00287	-0.003	-0.00246
12	0.18135	0.18119	0.181	2.11373	2.1138	2.112353
23	0.18138	0.18122	0.18104	4.05395	4.0539	4.05098
23.5	0.18138	0.18122	0.18104	4.142144	4.1421	4.139073
23.75	0.18139	0.18122	0.18104	4.186265	4.1862	4.183144
24	0.18138	0.18122	0.18104	4.23035	4.2303	4.2272
25	0.18139	0.18122	0.18104	4.406736	4.4067	4.403448
26	0.18139	0.18123	0.18105	4.583117	4.5831	4.579667
26.5	0.18139	0.18123	0.1805	4.671308	4.6713	4.667844
27	0.18139	0.18123	0.18105	4.759506	4.7595	4.755963

Table 9-8. V_{OUT} versus V_{CM} with INA185A4 and R_{EXT} = 110Ω at 125°C

V_{DIFF} (mV)	V_{CM} (V)	V_{REF} (V)	$V_{OUT, Differential}$ (V)
26.1	12	0.18104	4.59735
26.1	15	0.18991	4.5966
26.1	9	0.17217	4.59804
26.1	25	0.21945	4.59397
26.1	0	0.14555	4.60547

9.4.1 Data Calculations

Table 9-9. Typical (Nominal) Shunt Voltage Gain vs. R_{EXT} at IN+ and IN-

R_{EXT}	$G_{Total, typical}$ (V/V)
0Ω	200
110Ω	176.6784452

Table 9-10. Calculated Total Gain Using Best Fit Line

T_A (°C)	-40	25	125
R_{EXT} = 0	199.9430451	199.8978107	199.883843
R_{EXT} = 110Ω	176.3839626	176.3770096	176.2355055

E_G is calculated relative to the typical gain as shown in Table 9-11

Table 9-11. Calculated Total Gain and Offset Error

T_A (°C)		-40	25	125
E_G (%)	R_{EXT} = 0	-0.028%	-0.051%	-0.058%
	R_{EXT} = 110Ω	-0.167%	-0.171%	-0.251%
V_{OS} (µV)	R_{EXT} = 0	-13.0103	-11.2788	-6.8169
	R_{EXT} = 110Ω	-16.2581	-15.4507	-13.8660

Table 9-12. Calculated and Predicted External Input Resistance Error (e_{EXT})

T_A (°C)		-40	25	125
$E_{G, EXT}$ (%)	Measured	-0.138%	-0.120%	-0.193%
	Predicted	-0.056%	-0.120%	-0.193%

Table 9-12. Calculated and Predicted External Input Resistance Error (e_{EXT}) (continued)

T_A (°C)		-40	25	125
$V_{OS, EXT}$ (µV)	Measured	-3.248	-4.172	-7.049
	Predicted	-2.65	-4.19	-6.63

Table 9-13. Calculated Total Gain and Offset Error Drift

Temperature Coefficient Calculation Range		Δe/(25°C- -40°C)	Δe/(125°C- -40°C)	Δe/(125°C- 25°C)
$E_{G\ Drift}$ (ppm/°C)	R_{EXT} = 0	-3.5	-1.8	-0.7
	R_{EXT} = 110Ω	-0.6	-5.1	-8.0
$V_{OS\ Drift}$ (nV/°C)	R_{EXT} = 0	26.639	37.536	44.619
	R_{EXT} = 110Ω	12.422	14.498	15.847

Table 9-14. Calculated and Predicted External Input Resistance Error Drift ($e_{EXT\ Drift}$)

Temperature Coefficient Calculation Range		Δe/(25°C- -40°C)	Δe/(125°C- -40°C)	Δe/(125°C- 25°C)
$E_{G\ Drift, EXT}$ (ppm/°C)	Measured	2.87	-3.30	-7.31
	Predicted	-9.9	-8.3	-7.3
$V_{OS\ Drift, EXT}$ (nV/°C)	Measured	-14.22	-23.04	-28.77
	Predicted	-23.62	-24.09	-24.4

Table 9-15. Measured Input Offset and Calculated $V_{OS, EXT}$ over V_{CM} at 125°C

V_{CM} (V)		0	9	12	15	25
V_{OS} (µV)	R_{EXT} = 0	10.31	-3.25	-6.65	-10.26	-22.26
	R_{EXT} = 110Ω	32.47	-9.71	-13.59	-17.86	-32.78
$V_{OS, EXT}$ (µV)		22.16	-6.47	-6.94	-7.59	-10.53

Table 9-16. Measured Input CMRR and Calculated $CMRR_{EXT}$ at 125°C

Calculation Method		Two Point		Best Fit	
Units		µV/V	dB	µV/V	dB
CMRR RTI	R_{EXT} = 0	-1.30	-117.70	-1.29	-117.77
	R_{EXT} = 110Ω	-2.61	-111.67	-2.51	-111.99
$CMRR_{EXT}$		-1.31	6.04	-1.22	5.78

Table 9-17. Measured and Predicted $V_{OS, EXT}$ over V_{CM} at 125°C

V_{CM} (V)		0	9	12	15	25
$V_{OS, EXT}$ (µV)	Measured	22.16	-6.47	-6.94	-7.59	-10.53
	Predicted	4.78	-5.82	-6.63	-7.43	-10.10

V_{SENSE} = 23-mV, T_A = 125°C

Table 9-18. $V_{REF\_EFFECTIVE}$ (V) over V_{CM}

V_{CM} (V)		0	9	12	15	25
R_{EXT} = 0	Measured	0.14555	0.17213	0.18101	0.18988	0.21948
	Predicted	0.146157952	0.172487021	0.181263378	0.190039734	0.219294255
	Prediction Error	-6.08E-04	-3.57E-04	-2.53E-04	-1.60E-04	1.86E-04
R_{EXT} = 110Ω	Measured	0.14555	0.17217	0.18104	0.18991	0.21945
	Predicted	0.146158039	0.17248129	0.181255707	0.190030124	0.219278181
	Prediction Error	-6.08E-04	-3.11E-04	-2.16E-04	-1.20E-04	1.72E-04

Table 9-19. $V_{REF, EFFECTIVE}$ (V) over Temperature

T_A (°C)		-40	25	125
R_{EXT} = 0	Measured	0.18136	0.18121	0.18101
	Predicted	0.18110	0.18116	0.18126
	Prediction Error	2.65E-04	4.90E-05	-2.53E-04
R_{EXT} = 110Ω	Measured	0.18138	0.18122	0.18104
	Predicted	0.18109	0.18115	0.18126
	Prediction Error	2.92E-04	6.66E-05	-2.16E-04

9.5 Analysis

The determined data nicely follow the predictive model and thus easily fall within maximum possible error, which is unlikely to measure.

One notable difference between measurements and predictions occur at -40°C as seen with gain errors in Table 9-12 and Table 9-14. This can mostly be because the model's parameters assumed linear temperature coefficients; however, R_{EXT} can easily have non-linear, even parabolic, temperature coefficients that changed polarity going cold. Best efforts was made to get lowest prediction errors and future efforts can employ non-linear temperature coefficients. Tradeoffs were made so that prediction model at least matched the 125°C range.

The other high prediction error occurred with the $V_{OS, EXT}$ at V_{CM}=0-V in Table 9-17. This can be a result of the change in $I_{B, CM}$ slope when $V_{CM} < V_S$, which can be seen in Figure 2-2. If accurate leakage input bias current is required at this level please post an inquiry on our public forum for more information.

10 Input Resistance Error Test with INA191 Over Temperature

A characterization of the INA191A4 was performed to quantify and verify the error generated by input resistance at input pins (e_{EXT}).

10.1 Schematic

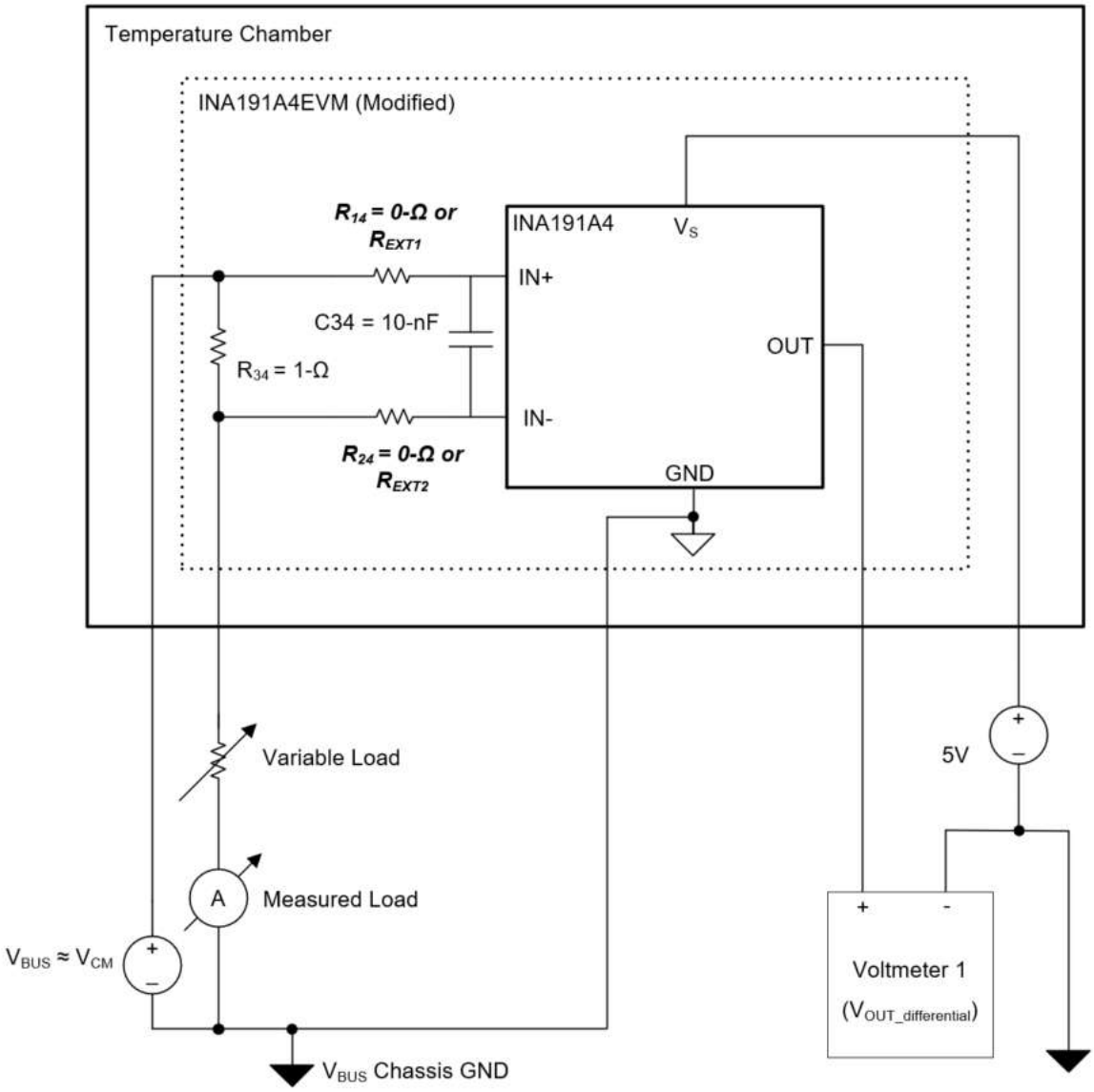


Figure 10-1. Test Setup to Measure External Resistance Error with INA191A4EVM

For testing, non-temperature compliant components were removed.

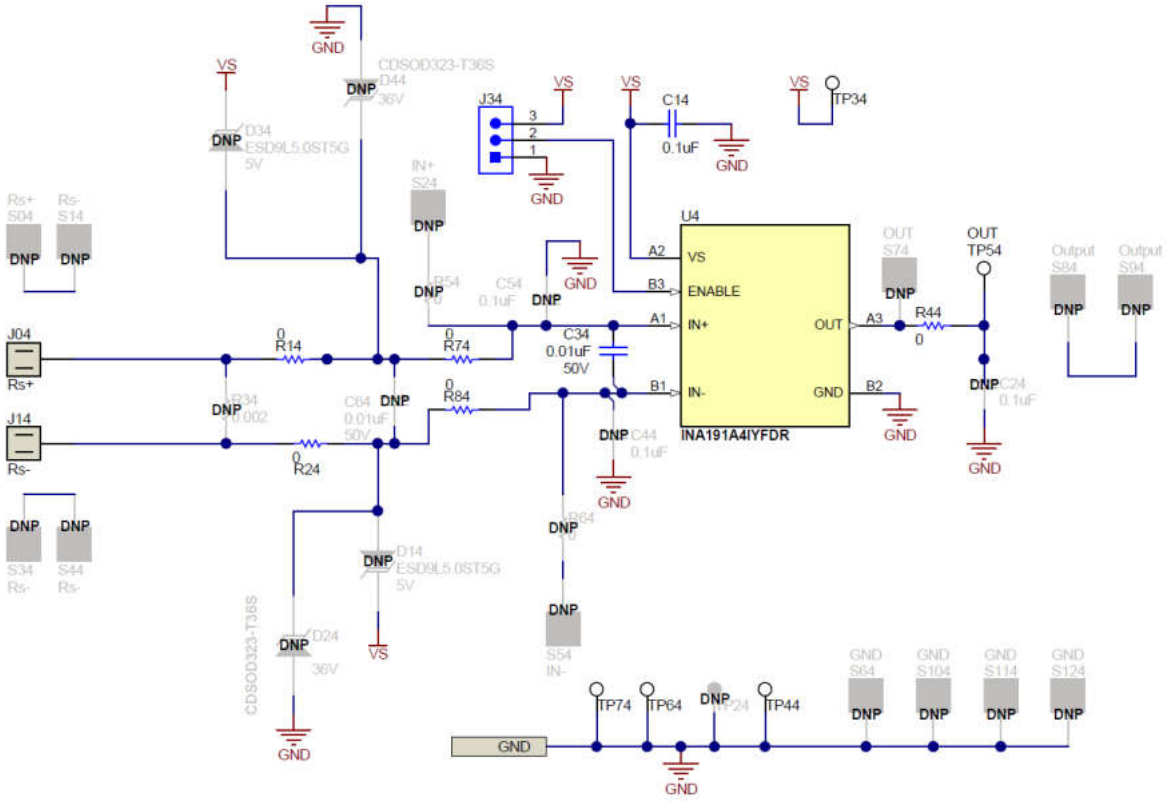


Figure 10-2. INA191A4EVM Schematic

10.2 Methods

EVM shunt resistor pads were populated a 1Ω shunt resistor, which was measured with a 4-wire force and sense Ohm meter inside a temperature chamber at -40°C, 25°C, and 125°C. The input resistors chosen for the input pins (R_{EXT1} at IN+ and R_{EXT2} at IN-) were 2.2kΩ resistors along with a differential 10nF input capacitor.

Table 10-1. BOM for INA191A4EVM Modifications

Name (EVM Designator)	Value	Tolerance	Drift (ppm/°C)	Package
R_{SHUNT} (R34)	1Ω	1%	200ppm/°C	1206
R_{EXT1} (R74), R_{EXT2} (R84)	2.2kΩ	1%	25ppm/°C	0603
C_{DIFF} (C34)	10nF	5%	C0G, NP0	0603

Input-Output sweeps were run on the EVM at -40°C, 25°C, and 125°C ambient temperatures first with R_{EXT} = 0Ω and then with R_{EXT} = 2.2kΩ. Load current was controlled by a power rheostat and monitored a precision, 8-digit Ammeter. Approximate current sweep range was from 0.48µA to 240mA. V_{OUT} was measured by a >5.5 -digit voltmeter and monitored to remain with device's linear output operating region. Linear output region for INA191 was defined at 0.9V < V_{OUT} < 4.9V.

Data analysis began by calculating the total shunt voltage gain using a 2-point line method on all of the V_{OUT} and the V_{DIFF} values within the designated linear output region. For each V_{DIFF}, an input offset is calculated using linear interpolation with the calculated gain. The final V_{OS} chosen for analysis was the average of all individual offsets pertaining to designated linear output region. Data analysis using gain calculated from a best-fit line was also performed as a check for any major dissimilarities.

Exact external input resistance errors ($E_{G,\ EXT}$, $V_{OS,\ EXT}$, $E_{G\ DRIFT,\ EXT}$, $V_{OS\ Drift,\ EXT}$) quantified by simply calculating the error difference with and without input resistances. Note that the same e_{EXT} error can be calculated even if shunt resistor was not calibrated.

10.3 Theoretical Model

For CSA with capacitive-coupled inputs, the best way to calculate error is to determine R_{DIFF} at each operating temperature using data sheet plots and then use the GEF equation to understand how gain can attenuate. Section 7.

A theoretical model was considered using parameters below. The R_{DIFF} values from the data sheet and the device's measured gain ($G_{Device,\ measured}$) at each temperature were entered. The predicted total gain ($G_{Total,\ predicted}$) was calculated using:

$$G_{Total,\ predicted} = \left(Gain_{CSA,\ Measured}\right) \times GEF \quad (23)$$

Table 10-2. Prediction Model Parameters Over Temperature

T_A (°C)	-40	25	125
R_{SH} (Ω)	0.99789	1.00116	1.0015
R_F (Ω)	2.20E+03	2.20E+03	2.20E+03
$R_{DIFF,\ Typical}$ (Ω)	3.20E+06	2.75E+06	2.55E+06
$E_{G,\ EXT}$ (%)	-0.137%	-0.160%	-0.172%
$E_{G,\ EXT\ Drift}$ (ppm/°C)	-3.45	-2.12	-1.25
$G_{Device,\ measured}$	199.66932	199.86724	200.23399
$G_{Total,\ predicted}$	199.3950856	199.547887	199.8890043
$E_{G,\ EXT\ predicted}$ (%)	0.022%	0%	-0.013%

10.4 Data for INA191A4 With 2.2kΩ Input Resistors

Table 10-3. Calibrated R_{SHUNT} on INA191A4EVM Over Temperature

T_A (°C)	-40	25	125
$R_{SH,\ measured}$ (Ω)	0.99789	1.00116	1.0015
eR_{SH} (%)	-0.211%	0.116%	0.150%
$R_{SH,\ Drift}$ (ppm/°C)	50.307692	21.878788	3.4

Table 10-4. Input-Output Sweep with INA191A4 and R_{EXT} = 0Ω

$V_{DIFF,\ Calculated}$ (mV)			V_{OUT} (V)		
-40°C	25°C	+125°C	-40°C	25°C	+125°C
0.484825	0.485528	0.478769	0.09668	0.09601	0.09280
0.908523	0.909337	0.905151	0.18133	0.18070	0.17772
1.464961	1.462261	1.468486	0.29247	0.29125	0.29058
2.102504	2.110565	2.105797	0.41977	0.42083	0.41828
2.102741	2.109942	2.105788	0.41985	0.42068	0.41834
2.551209	2.558095	2.553090	0.50940	0.51025	0.50795
3.154687	3.160202	2.553106	0.62987	0.63065	0.50789
5.063895	3.161080	3.162842	1.01145	0.63079	0.63000
5.031813	5.008907	4.946338	1.00473	1.00013	0.98736
4.912880	12.613467	4.008277	0.98106	2.52000	0.79956
12.569323	17.832034	8.577695	2.50960	3.56310	1.71460
12.569183	24.050121	8.578369	2.50970	4.80580	1.71480
17.900021		12.524469	3.57410	0.00000	2.50485
2.544290		12.524809	0.50806		2.50500
2.097469		17.676315	0.41884		3.53680
24.021867		23.489411	4.79630		4.70040
		23.485776	0.00000		4.69970
		24.121608			4.82690

Table 10-5. Input-Output Sweep with INA191A4 and R_{EXT} = 2.2kΩ and 10nF C_{DIFF}

$V_{DIFF, Calculated}$ (mV)			V_{OUT} (V)		
-40°C	25°C	+125°C	-40°C	25°C	+125°C
0.476242	0.483633	0.479845	0.09530	0.09593	0.09227
0.892124	0.901249	0.889850	0.17816	0.17928	0.17425
0.902795	1.421182	0.889805	0.18033	0.28319	0.17427
1.464974	1.390352	1.449013	0.29243	0.27700	0.28619
1.464880	1.418044	1.974379	0.29250	0.28255	0.39125
2.102471	2.057876	2.395434	0.41938	0.41041	0.47547
2.549459	2.062634	2.393717	0.50878	0.41130	0.47513
4.988136	2.545354	5.031936	0.99539	0.50763	1.00290
8.515544	2.544886	5.031460	1.69930	0.50756	1.00282
12.582525	3.206893	8.601486	2.51050	0.63973	1.71705
17.666625	4.820948	12.925429	3.52500	0.96205	2.58175
24.045976	8.514315	12.925960	4.79775	1.69960	2.58200
	12.460748	17.395654		2.48755	3.47575
	17.654245	22.840950		3.52445	4.56490
	17.655266	22.847860		3.52465	4.56640
	22.683582	23.739866		4.52860	4.74460
	22.720635			4.53560	
	24.072722			4.80590	
	24.073693			4.80610	

10.4.1 Data Analysis

Table 10-6. Typical (Nominal) Shunt Voltage Gain vs. R_{EXT} at IN+ and IN-

R_{EXT}	$G_{Total, typical}$
0.0	200.0
2.2kΩ	199.6804386

Table 10-7. Calculated and Predicted Total Gains

T_A (°C)		-40	25	125
$G_{Measured}$ (V/V)	R_{EXT} = 0	199.66932	199.8672363	200.23399
	R_{EXT} = 2.2kΩ	199.51201	199.66757	200.01409
$G_{Predicted}$ (V/V)	R_{EXT} = 2.2kΩ	199.395086	199.547887	199.8890043
	Prediction Error	0.0586%	0.0599%	0.0625%

Table 10-8. Calculated Gain and Offsets Errors

T_A (°C)		-40	25	125
E_G (%)	R_{EXT} = 0	-0.165%	-0.066%	0.117%
	R_{EXT} = 2.2kΩ	-0.084%	-0.006%	0.167%
V_{OS} (µV)	R_{EXT} = 0	-0.0639	-5.0446	-15.5430
	R_{EXT} = 2.2kΩ	0.9849	-2.9431	-17.9767

Table 10-9. Calculated Gain and Offset Drift

Temperature Range		Δe/(25°C- -40°C)	Δe/(125°C- -40°C)	Δe/(125°C- 25°C)
$E_{G, Drift}$ (ppm/°C)	R_{EXT} = 0	15.2	17.1	18.3
	R_{EXT} = 2.2kΩ	12.0	15.2	17.4
$V_{OS, Drift}$ (nV/°C)	R_{EXT} = 0	-76.63	-93.81	-104.98
	R_{EXT} = 2.2kΩ	-60.43	-114.92	-150.34

Table 10-10. Calculated and Predicted External Input Resistance Error (e_{EXT})

T_A (°C)		-40	25	125
$E_{G, EXT}$ (%)	Measured	0.081%	0.060%	0.050%
	Predicted	0.022%	0.000%	-0.013%
	Prediction Error	0.0586%	0.0599%	0.0626%
$V_{OS, EXT}$ (µV)	Measured	1.049	2.101	-2.434

Table 10-11. Calculated and Predicted External Input Resistance Error Drift ($e_{EXT, Drift}$)

Temperature Coefficient Calculation Range		Δe/(25°C- -40°C)	Δe/(125°C- -40°C)	Δe/(125°C- 25°C)
$E_{G Drift, EXT}$ (ppm/°C)	Measured	-3.24	-1.87	-0.98
	Predicted	-3.45	-2.12	-1.25
	Prediction error	0.21	0.25	0.27
$V_{OS Drift, EXT}$ (nV/°C)	Measured	16.19	-21.11	-45.35

10.5 Analysis

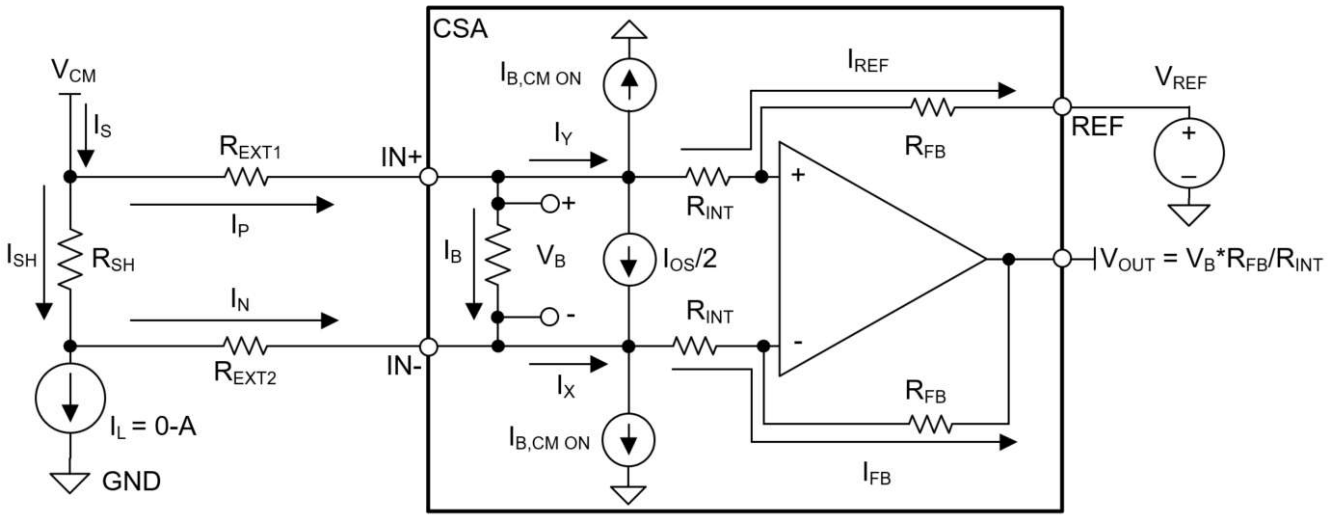
The INA191 performed very closely as expected according to the theoretical calculations. Prediction errors for $E_{G, EXT}$ (approximately 0.06%) and $E_{G, EXT Drift}$ (approximately 0.25ppm/°C) were precise and show little change over temperature. These errors were small enough that the errors can come simply from variation in R_{EXT} and/or ammeter accuracy.

$E_{G, Drift}$ performance for INA191 was outside of its specification of 7ppm/°C, although this does not affect analysis primarily because the critical value of measurement was e_{EXT}, which is a delta measurement with and without R_{EXT}. Certainly, the most probably reason for this large gain error drift was an imperfect calibration of the shunt resistor.

$V_{OS, EXT}$ was reasonable at around 2.4µV at 125°C, but $V_{OS, EXT Drift}$ was significant at -45nV/°C when increasing temperature to 125°C. As expected, $V_{OS, EXT Drift}$ reduces and flips polarity to 16.9nV/°C when decreasing temperature. Further efforts to reduce this drift can by increasing C_{DIFF}.

Considered that the theoretical model used typical R_{DIFF} values over temperature, yet performance was just below model boundaries. This indicates that for future designs, sufficient margin can be established to understand worst-case gain error. Downshifting (or reducing) the R_{DIFF} curve by 30% can provide ample margin.

11 Derivation of $V_{OS, EXT}$ for a Single Stage Current Sense Amplifier (CSA)



This derivation assumes a single-stage, linear CSA. Derivation first begins by determining V_B (bias voltage across bias resistor) when load (I_L) is 0A as this is essentially $V_{OS, EXT\ RTI}$. Then this is divided by gain error factor (GEF) to get the referred-to-shunt offset error ($V_{OS, EXT\ RTS}$). Note that this derivation also requires a more specific equation for GEF which assumes that the R_{EXT} value at each pin can be different.

$$
\begin{aligned}
&Let \quad {}^{I_{OS}}\!/_{2} = I_{OS2} \\
&Let \quad R_{FB} + R_{INT} = R_{FI} \\
&Let \quad I_L = 0 - A \\
&(1) \quad I_{SH} - I_N - I_L = 0 \\
&(2) \quad I_P - I_X - I_B - I_{CM,\,ON} = 0 \\
&(3) \quad I_N - I_Y + I_B - I_{CM,\,ON} = 0 \\
&(4) \quad I_Y + I_{OS2} - I_{FB} = 0 \\
&(5) \quad I_X - I_{OS2} - I_{REF} = 0 \\
&(6) \quad V_{CM} - I_{SH}R_{SH} - I_N R_{F2} - I_{FB}R_{FI} - V_{OUT} = 0 \\
&(7) \quad V_{CM} - I_P R_{EXT1} - I_{REF}R_{FI} - I_{FB}R_{FI} - V_{REF} = 0 \\
&(8) \quad V_{CM} - I_{REF}R_{INT} + + I_{FB}R_{INT} = 0 \\
&(9) \quad V_{OUT} = V_{REF} + V_B\frac{R_{FB}}{R_{INT}} \\
&(10) \quad V_{SH} - I_P R_{EXT1} - V_B + R_{EXT2}I_N = 0
\end{aligned}
\tag{24}
$$

(4) into (3) and (5) into (2)

$$
\begin{aligned}
I_P &= I_{CM,\,ON} + I_B + I_{OS2} + I_{REF} \\
I_N &= I_{CM,\,ON} - I_B - I_{OS2} + I_{FB}
\end{aligned}
\tag{25}
$$

(2) into (7)

$$
I_{REF} = \frac{V_{CM} - V_{REF} - R_{EXT1}\left(I_{CM,\,ON} + I_B + I_{OS2}\right)}{R_{FI} + R_{EXT1}}
\tag{26}
$$

(7) into (8)

$$I_{FB} = \frac{V_{CM} - V_{REF} - R_{EXT1}(I_{CM,\,ON} + I_B + I_{OS})}{R_{FI} + R_{EXT1}} - \frac{V_B}{R_{INT}} \quad (27)$$

(1), (3), and (9) into (6).

$$V_{BUS} - V_{REF} - V_B\left(R_{FB}/R_{INT}\right) + V_B\left(R_{SH} + R_{EXT2}\right)/R_B - \left(I_{CM} - I_{OS2}\right)\left(R_{SH} + R_{EXT2}\right) - I_{FB}\left(R_{FI} + R_{SH} + R_{EXT2}\right) = 0 \quad (28)$$

(8) into (6). Solve for V_B

$$Let\ \ C_{EV} = \frac{R_{FI} + R_{SH} + R_{EXT2}}{R_{FI} + R_{EXT1}} = \frac{1 + \frac{R_{SH} + R_{EXT2}}{R_{FI}}}{1 + \frac{R_{EXT1}}{R_{FI}}} \quad (29)$$

$$V_B = \frac{\left(V_{REF} - V_{BUS}\right)\left(1 - C_{EV}\right) + I_{B,CM\,ON}\left(R_{SH} + R_{EXT2} - R_{EXT1}C_{EV}\right) - \frac{I_{OS}}{2}\left(R_{SH} + R_{EXT2} + R_{EXT1}C_{EV}\right)}{1 + \left(R_{SH} + R_{EXT2}\right)\left(\frac{1}{R_{INT}} + \frac{1}{R_{BIAS}}\right) + \frac{R_{EXT1}C_{EV}}{R_{BIAS}}}$$

$$V_B = V_{OS,\,EXT\,RTI}\ \ when\ \ I_L = 0$$

Determine Gain Error Factor when R_{EXT1} does not equal R_{EXT2}. You can simply remove $I_{CM, ON}$, I_{OS} sources, and set V_{CM} and V_{REF} sources to 0V as these only affect the offset. Gain is constant throughout operational V_{CM}.

(5) into (2)

$$Let\ \ I_{CM,\,ON}\ \ and\ \ I_{OS} = 0 \quad (30)$$
$$Let\ \ V_{CM} = V_{REF} = 0$$
$$I_P = I_B + I_{REF}$$

(2) into (7)

$$I_{REF} = \frac{0 - 0 - R_{EXT1}(I_B + 0 + 0)}{R_{FI} + R_{EXT1}} \quad (31)$$

(2), (8) into (10).

$$V_{SH} - V_B - I_B\left(R_{EXT} + R_{EXT2}\right) - I_R R_{EXT1} + I_R R_{EXT2} - V_B R_{EXT2}/R_{INT} = 0 \quad (32)$$

(7) into (10). Solve for V_B/V_{SH} = GEF

$$Let\ \ C_{EG} = \frac{R_{EXT1}}{R_{FI} + R_{EXT1}} \quad (33)$$

$$\frac{V_B}{V_{SH}} = GEF = \frac{1}{\left(1 + \frac{R_{EXT2}}{R_{INT}}\right) + \frac{R_{EXT1} + R_{EXT2}}{R_B} - \frac{C_{EG}(R_{EXT1} - R_{EXT2})}{R_B}}$$

$$V_{OS,\,EXT\,RTS} = \frac{V_{OS,\,EXT\,RTI}}{GEF}$$

12 Summary

The operational principles and equations for single-stage linear and capacitive-coupled CSAs match up with simulation and test data over temperature. True worst-case error might be statistically small, but are large enough to prompt potential one-point offset calibrations.

Also granted the right applications, using a resistor divider to set V_{REF} can provide substantial system and cost benefits.

13 References

- Texas Instruments, *Driving Voltage Reference Pins of Current-Sensing Amplifiers*, application note.

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