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TI Designs High Speed: CerTIfied™ Design
Direct Down-Conversion System with I/Q Correction

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Design Resources

Design Archive	TSW6011EVM Schematic
MCR Installer	Matlab Compiler Runtime
Installer	TSW6011EVM GUI
TSW6011EVM	Product Folder

Block Description

The I/Q Correction block implemented in the Field Programmable Gate Array (FPGA) of the TSW6011EVM helps users to adopt a direct down-conversion receiver architecture in a wireless system. The I/Q correction block consists of a single-tap blind algorithm, which corrects the frequency-independent I/Q imbalance in a complex zero-IF receiver system. Along with the I/Q correction block, the FPGA includes a digital gain block, a digital power-measurement block, x2 of interpolation block, an I/Q offset correction block, and a quadrature mixing block.

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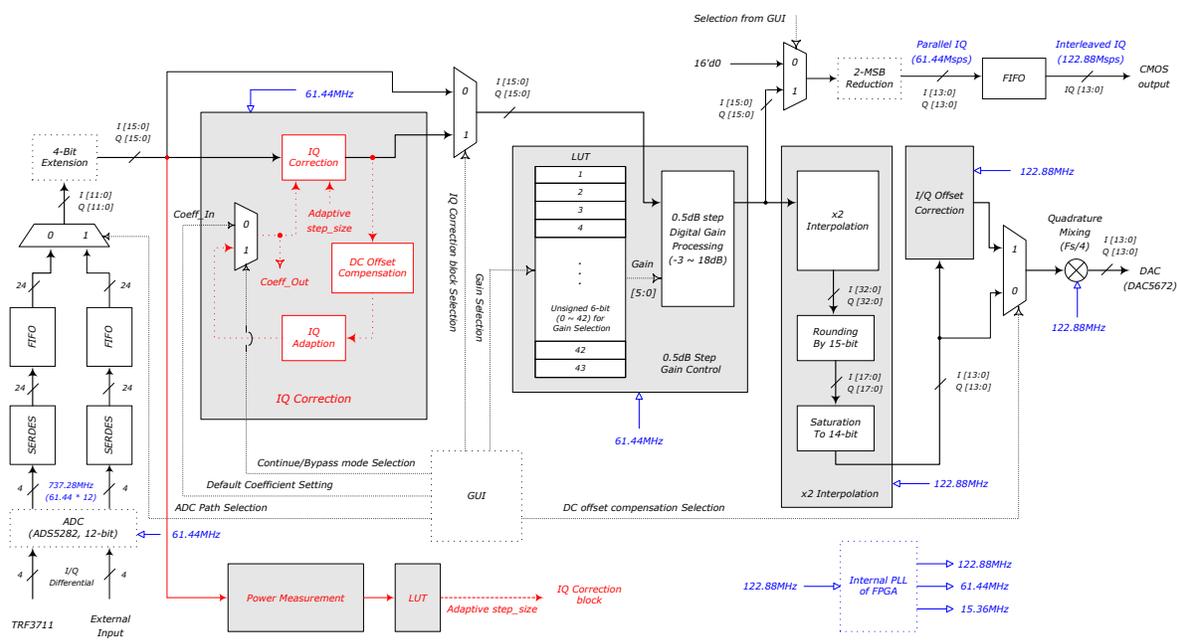
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1 Introduction

This document describes the direct down-conversion (zero-IF) architecture in a wireless receiver system, and the I/Q correction algorithm implemented in a Field Programmable Gate Array (FPGA) of the TSW6011 evaluation module (TSW6011EVM). The benefits of the direct down-conversion and high/low intermediate frequency (IF) architecture system designs are addressed, along with the benefits of I/Q correction processing in a direct down-conversion receiver system. Finally, error vector magnitude (EVM) results are presented as a result of I/Q correction processing in order to compensate for the degradation of signal quality from a direct down-conversion receiver system. Figure 1 shows the block diagram of the TSW6011 Evaluation Module.

Components of the TSW6011EVM

- Altera Cyclone III – FPGA implemented with I/Q Correction and other required algorithms
- TRF371125 – I/Q demodulator up to 4 GHz with on-chip programmable low-pass filter (LPF)
- ADS5282 – octal-channel analog-to-digital converters (ADCs) with maximum 65 Msps of sampling speed
- CDCE62005 – 5 to 10 output clock generators with jitter cleaner
- DAC5672 – 14-bit dual digital-to-analog converter (DAC)
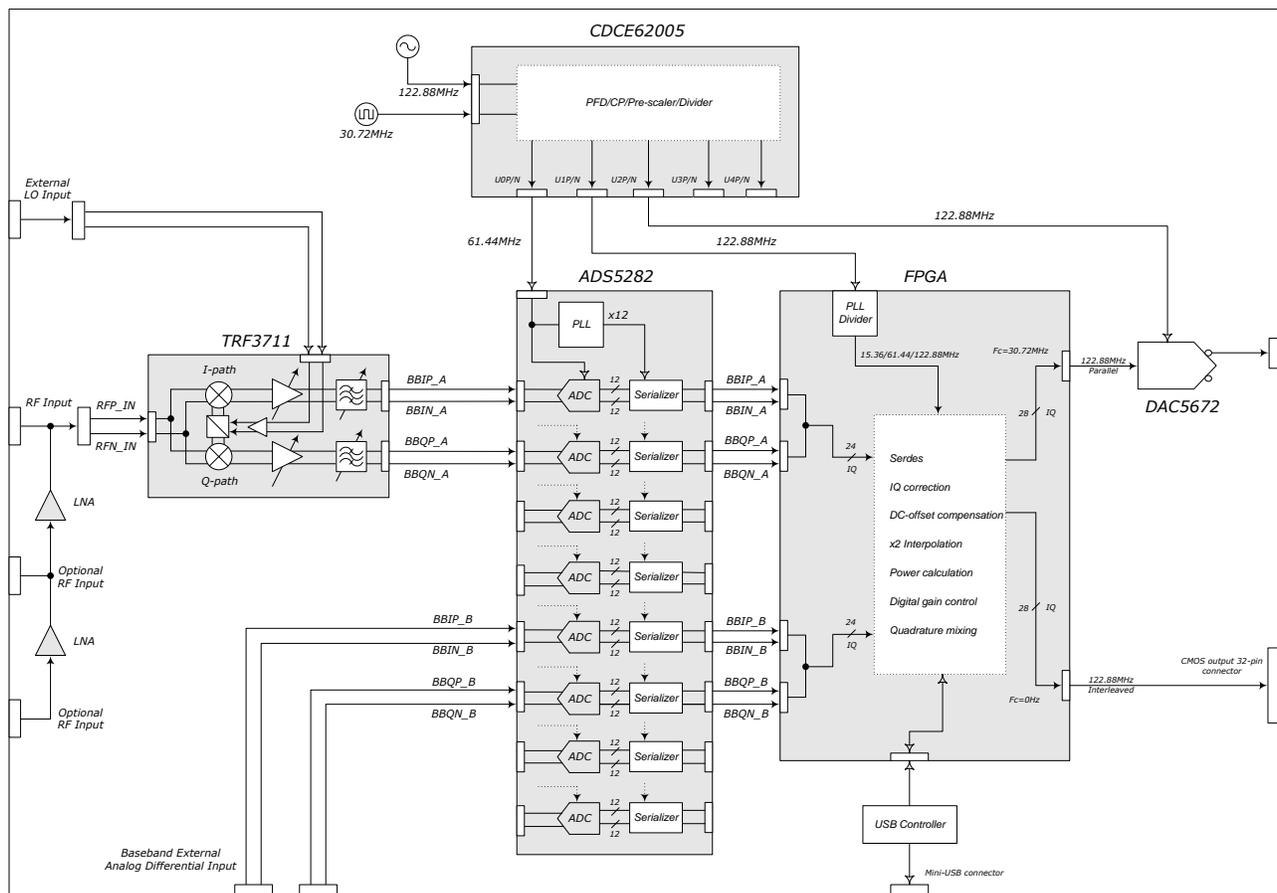
Figure 1. Block Diagram of the TSW6011 Evaluation Module

2   Design Summary

The I/Q imbalance of phase and amplitude causes image interference. This effect severely impacts the overall signal quality such as signal-to-noise ratio (SNR), error vector magnitude (EVM), and sensitivity, while demodulating the complex signal. These impacts are a concern for direct down-conversion architecture designs, although direct down-conversion architecture (zero-IF) provides many other benefits when compared to alternate digital-IF architecture. With the aid of I/Q correction, direct down-conversion is achieved in the receiver system while reducing the complexity, current consumption, and overall size of a receiver system.

Figure 2 and Figure 3, respectively, show –35.66 dB of EVM without I/Q correction processing. The I/Q correction block in the TSW6011 improves the EVM to –51.4 dB.
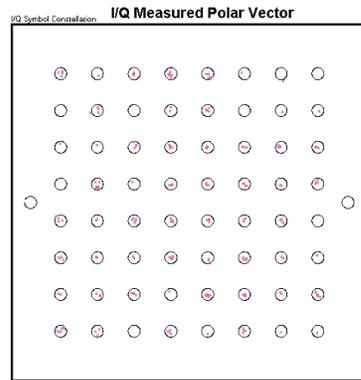
Figure 2. EVM Without LPF (Before I/Q Correction)   **Figure 3. EVM Without LPF (After I/Q Correction)**

Figure 4 illustrates the I/Q imbalance of phase, gain, and offset with and without I/Q correction processing. The RF input signal is temporarily shifted by 4 MHz at the radio-frequency (RF) input. Hence, the composite signal bandwidth is 13 MHz for I/Q correction processing. The blue trace represents the pre-I/Q correction, and the yellow trace represents the post-I/Q processing. The adjacent-channel-leakage ratio (ACLR) shows –64.9 dBc after I/Q correction processing.
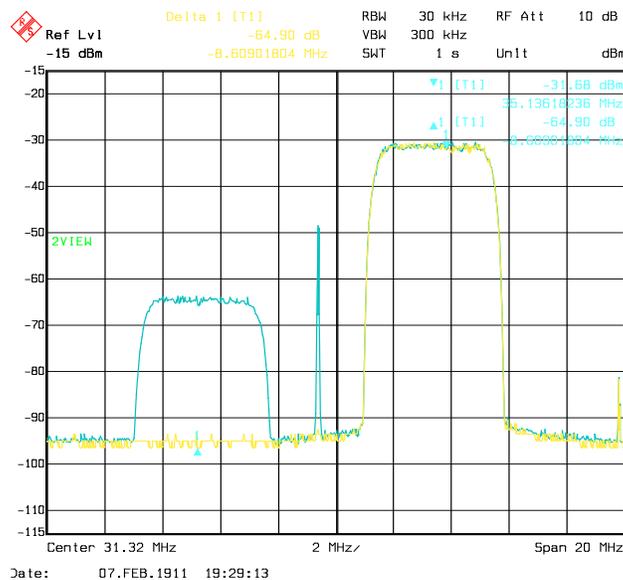
Figure 4. Reference Test Result Using WCDMA Test Signal

3 Theory of Operation

In the analog domain of a direct down-conversion system, a demodulated complex signal inherently includes amplitude-phase imbalance between In-phase (I) and Quadrature-phase (Q) signal paths. This imbalance exists because these signals are not perfectly matched to each other. The I/Q amplitude and phase imbalance produces a sideband image that severely degrades the EVM of the received signal. In wireless receiver architecture, the degradation of received signal quality worsens sensitivity, and possibly causes the system to become out of specification in terms of system operation requirements. The sensitivity of the received signal must be held as high as possible in any wireless system.

The blind estimation algorithm for frequency-independent I/Q imbalance uses the properness (see the following note) of second-order statistics of a complex signal. The I/Q correction algorithm in the TSW6011EVM is based on the second-order statistics of the received signal, which means that complex signals are mutually independent and uncorrelated with each other. As long as a signal is proper (also referred to as circular, see the following note), the average energy of I and Q are equal.

> **NOTE:** A proper signal is always circular, but a circular signal can be improper.

As I/Q imbalance in a direct down-conversion system makes the received complex signal improper and noncircular, the I/Q correction algorithm applies a blind-estimation method to correct this imbalance by using the concept of orthogonality (that is, properness or circularity). This blind-adaptive Digital Signal Processing (DSP) algorithm is implemented with a single-tap equalizer for the wideband input signals in a FPGA onboard the TSW6011EVM.

TSW6011 shows a significant performance improvement from direct down-conversion architecture in a typical wireless-receiver system as well as the benefit of I/Q correction algorithm that corrects both I/Q phase and amplitude imbalance through the use of blind algorithm implemented in FPGA. After I/Q correction processing, the degraded EVM of the received signal is restored to the respective original levels.

3.1 General Overview of Receiver Architecture in WiMAX Transceiver System

3.1.1 Heterodyne Receiver Architecture

In wireless receiver systems, heterodyne architecture implies high/low-IF or digital IF architecture. A direct down-conversion receiver down-converts the received RF signal directly into a complex baseband signal. On the other hand, a heterodyne receiver requires the IF stage to down-convert the RF to IF before demodulating the received analog signal to complex baseband signal (see the following note).

> **NOTE:** A real system is always referred as heterodyne but complex system can be either heterodyne or homodyne.

One of most widely-used heterodyne receivers is digital-IF architecture; Figure 1 shows an example of this design. A time-division duplexing (TDD)-based digital-quadrature-demodulation architecture is equal to the value shown in Equation 1.

$(3 \times Fs / 4)$ MHz of IF

where

- Fs is a sampling frequency for ADC (1)

The received RF signal feeds into the duplexer through an antenna and then is processed by a low-noise amplifier (LNA) to boost the received input signal. After appropriate wideband filtering for RF band selection, a mixer down-converts the RF signal to IF. Examples of some specified bands are 2300 to 2400 MHz, 3300 to 3400 MHz, or 1785 to 1805 MHz in uplink. In the IF stage, the IF channel filter (usually low-pass filter or band-pass filter) removes the sideband image and local oscillator (LO) leakage.

In heterodyne receiver architecture, the sideband image caused by I/Q phase and amplitude mismatch is located at twice the IF distance from the carrier, and therefore the quality of the desired signal is not affected by I/Q imbalance. But the sideband image should be eliminated by appropriate filtering (such as low pass filter or band pass filter) or suppressed enough to maintain the optimum receiver performance. For a discussion of the system requirements for sideband rejection of transmission for optimal digital pre-distortion performance, see the Texas Instruments application report, *Sideband Rejection and FB Isolation Impacts on DPD Performance* (SLWA063). Because every ADC input-frequency component outside the Nyquist bandwidth always folds back into the first Nyquist zone, these components should be filtered or suppressed to obtain the robust receiver performance.
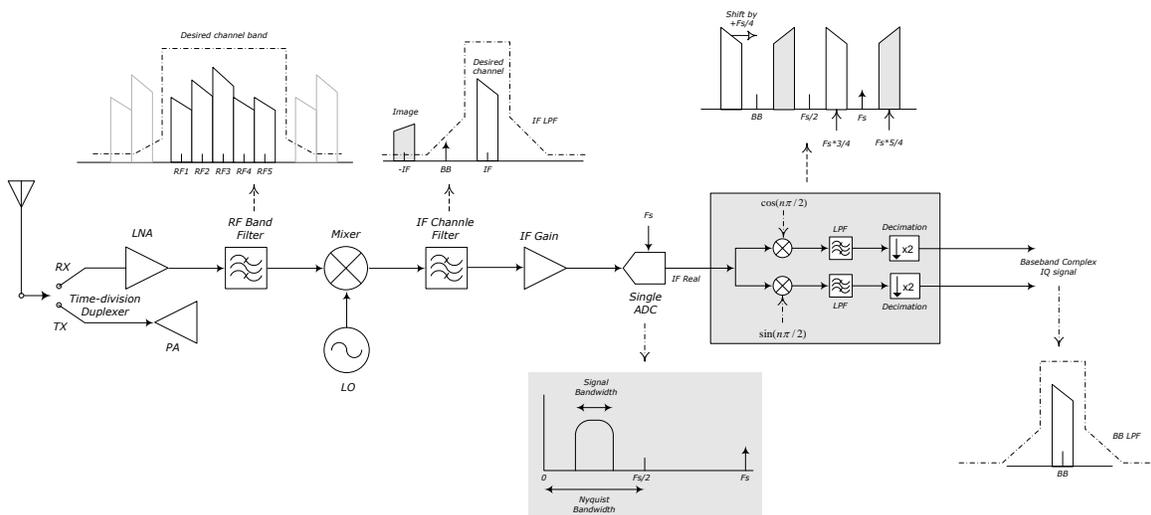
Figure 5. Block Diagram of Heterodyne Receiver Architecture

Chose Equation 1 and as a result, a complex demodulation process is simplified greatly with a digital coarse mixer (see in Figure 5). During the demodulation process, the desired signal located at –Fs / 4 is shifted by +Fs / 4 and passes through a LPF to eliminate the replicated spectra caused by the sampling process. The Nyquist bandwidth in a real-heterodyne receiver system is only half the bandwidth compared to that of complex zero-IF architecture; therefore, twice the sampling frequency for ADC is required to obtain the same Nyquist bandwidth as a direct down-conversion system.

3.1.2   Homodyne Receiver System

Homodyne, zero-IF, and direct-conversion are the same basic topology — LO frequency is equal to the input-carrier frequency in these types of receivers. A direct down-conversion receiver has many benefits compared to Heterodyne architecture, such as hardware simplicity, reduced cost, a smaller transceiver size, and lower-power consumption. Figure 6 shows the basic design of homodyne receiver architecture.
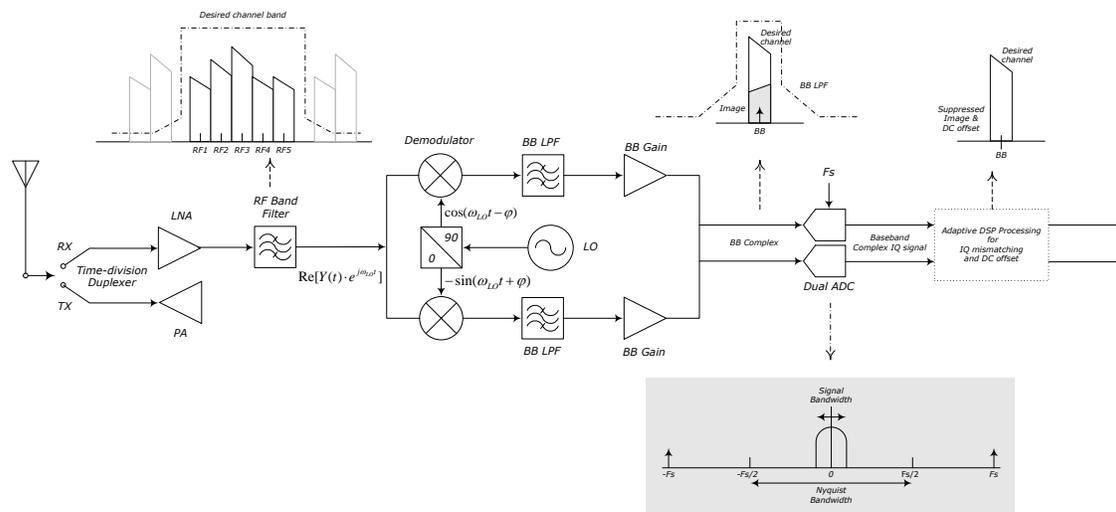
Figure 6. Block Diagram of Homodyne Receiver Architecture

Direct down-conversion architecture does not include IF stages between RF and baseband stages. The RF input signal is received and then directly demodulated into the baseband. This approach clearly implies that the RF input frequency and the LO frequency are the same. Because the sideband image caused by I/Q phase and amplitude mismatch is located at the baseband and overlapped with the desired carrier signal, EVM results are significantly degraded when the receiver system does not have appropriate adaptive digital-signal processing to correct the sideband-image component.

Without I/Q correction processing, the heterodyne receiver is seen as the most reliable architecture because of the superior selectivity and sensitivity over direct down-conversion architecture, despite the complex system design and increased costs of this receiver. For this reason, heterodyne receiver architecture has been adapted to the wireless receiver system for many years, although this architecture is complex, expensive, and requires more current consumption.

In the same manner as the homodyne receiver, the direct down-conversion receiver converts received RF signal directly to baseband analog signal without the need of an IF stage as shown in Figure 2. The down-converted baseband-analog signal is then filtered by LPF to eliminate unwanted signal (such as blockers) and then digitized to complex digital signal by dual-ADC. Any I/Q imbalance is corrected by an adaptive DSP algorithm (blind algorithm) in the baseband to restore the received signal quality.

There are additional benefits of direct down-conversion architecture, including the reduced cost of the transceiver system and a simpler design of analog front-end block which avoids any unnecessary IF filtering. Because the Nyquist bandwidth of a complex I/Q signal is twice that of real signal, an additional benefit is that system designers are able to use complex architecture requiring only half of the ADC sampling clock compared to real architecture. This concept is very important in a digital pre-distortion (DPD) system as increased requests of wider signal bandwidth grows. Assume a composite signal bandwidth of 40 MHz, the DPD processing rate on transmission and feedback path are theoretically 200 MHz for each path considering up to fifth-order nonlinearity correction of the power amplifier (PA). For complex processing on the feedback path, ADC on feedback requires 400 MHz of sampling clock in a real heterodyne system, while direct down-conversion system requires only 200 MHz for ADC clock frequency (see note below).

> **NOTE:** Direct down-conversion (Homodyne) system is always referred to as complex architecture.

The negative side-effects should also be considered. These side-effects include the possibility of a mirrored image and DC offset within an inband-carrier signal. The sideband image is generated by phase and amplitude mismatch between the I and Q channels. The impact on the signal quality is severe, and therefore should be corrected to obtain optimum receiver performance. I/Q correction processing completely eliminates these negative impacts.

3.1.3 Functional Description of FPGA in TSW6011

The FPGA performs baseband signal processing such as digital power measurement, I/Q correction, digital gain control, x2 interpolation, DC offset compensation, and quadrature mixing. To convert the data format from serial to 12-bits of parallel data in FPGA, 12-bits of ADS5282 serial output with 61.44 MHz of sampled data rate is delivered to Serial-to-Deserial (SERDES) interface. For the I/Q correction processing, 12-bits of input bits are simply extended to 16-bits of the 2-complement format, and then delivered to I/Q correction module in FPGA. Figure 7 shows the FPGA block diagram.

After I/Q correction processing, the gain of I and Q signals can increase up to 18 dB based on a 0.5-dB step size. Because the ADS5282 has a 12-bit resolution and the DAC5672 has a 14-bit resolution, a gain compensation of 11.5 dB is recommended for the TSW6011EVM. Therefore, the 11.5-dB gain compensation is required for optimum performance including 0.5 dB of headroom.

> **NOTE:** 1 bit represents 6 dB of gain.

The improved signal dynamic range produces an improved signal quality at the baseband for characteristics such as bit error rate (BER), SNR, and EVM. Interpolation by a factor of 2, DC-offset compensation, and quadrature-mixing blocks are followed by digital gain-control processing to the DAC interface.
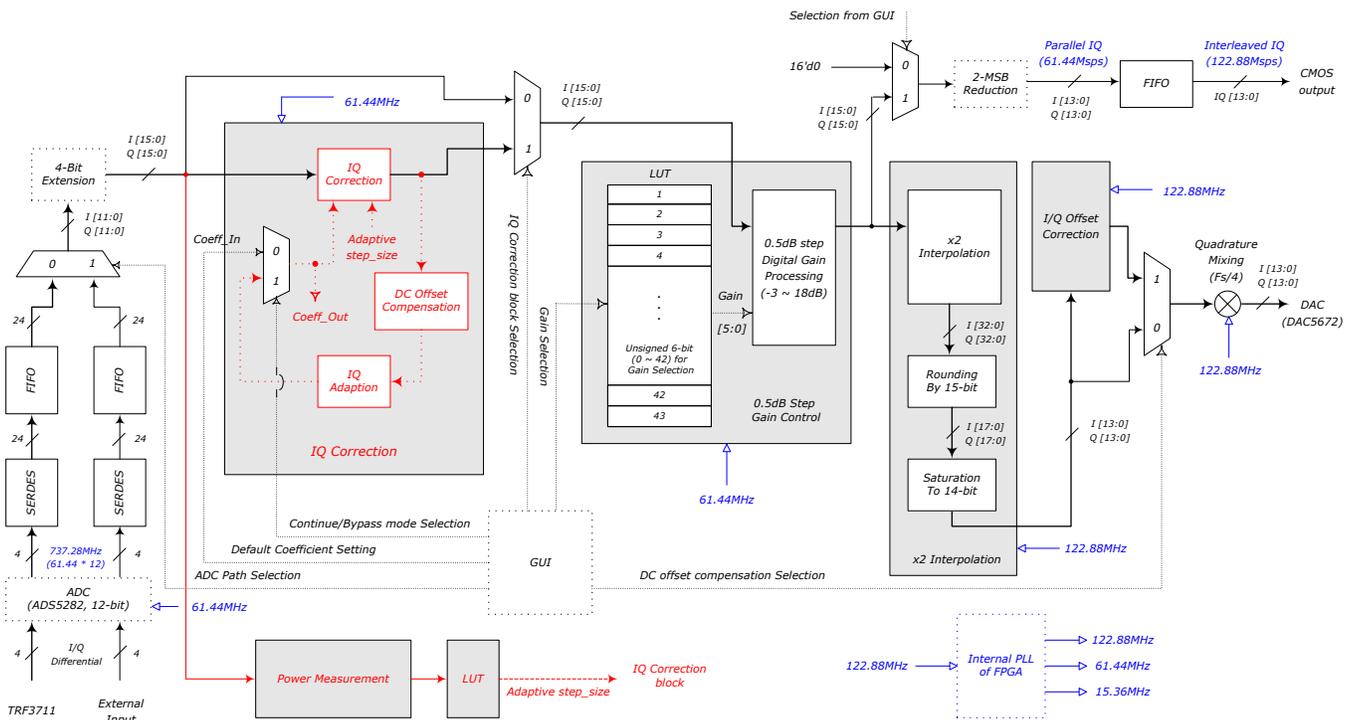
Figure 7. Block Diagram of FPGA in TSW6011

3.1.3.1 Power Measurement Block

The power measurement block calculates the digital power of the incoming signal to FPGA based on a 61.44-MHz clock cycle. Power values of each I and Q are accumulated four times for each 8.5 ms {= 2^{19} (524,288 samples) × 16.276 ns (61.44 MHz)} with different time intervals starting at t0, t1, t2, and t3 respectively, and averaged to 32-bits of bit width. Therefore, the power-averaged value is updated every 34 ms (= 8.5 ms × 4) in FPGA. Figure 8 shows a block diagram of the power measurement block of FPGA.
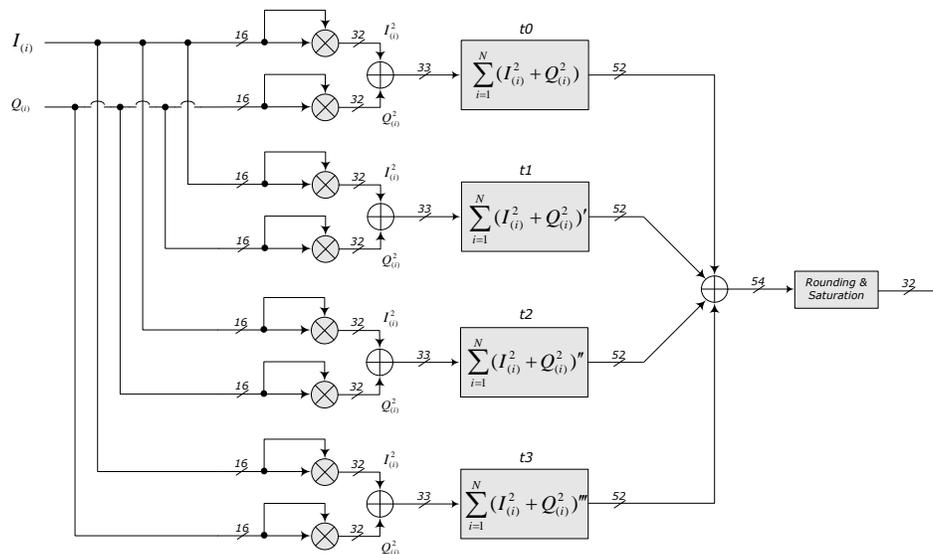
Figure 8. Block Diagram of Power Measurement in FPGA

The calculated power-averaged value is primarily used to find the optimum step size of I/Q correction processing. Depending on the input power level to FPGA, the optimum step size is automatically applied to the I/Q correction block. Without this automatic gear-shifting feature, the adaptive I/Q-correction performance is not very stable because the incoming receiver- (RX) signal power is not constant from mobile station.

3.1.3.2   I/Q Correction Block

In practice, the quadrature signals in the analog demodulator do not have exactly the same amplitudes or an exact phase difference of 90 degrees between I and Q paths. These characteristics are called amplitude-phase imbalance, and cause crosstalk between I and Q channels. Note that the asymmetry between analog filters in the I and Q rails after the demodulator also contributes to the imbalance. For narrow band-input signals, the amplitude-phase imbalance is considered as frequency independent. For wide band inputs, the amplitude/phase imbalance exhibits frequency-dependent behavior, which may be a result of both analog filter and demodulator. The I/Q correction block in TSW6011 is based on a frequency-independent algorithm that adapts blindly with the received signal. Figure 9 shows a block diagram of I/Q correction in FPGA.
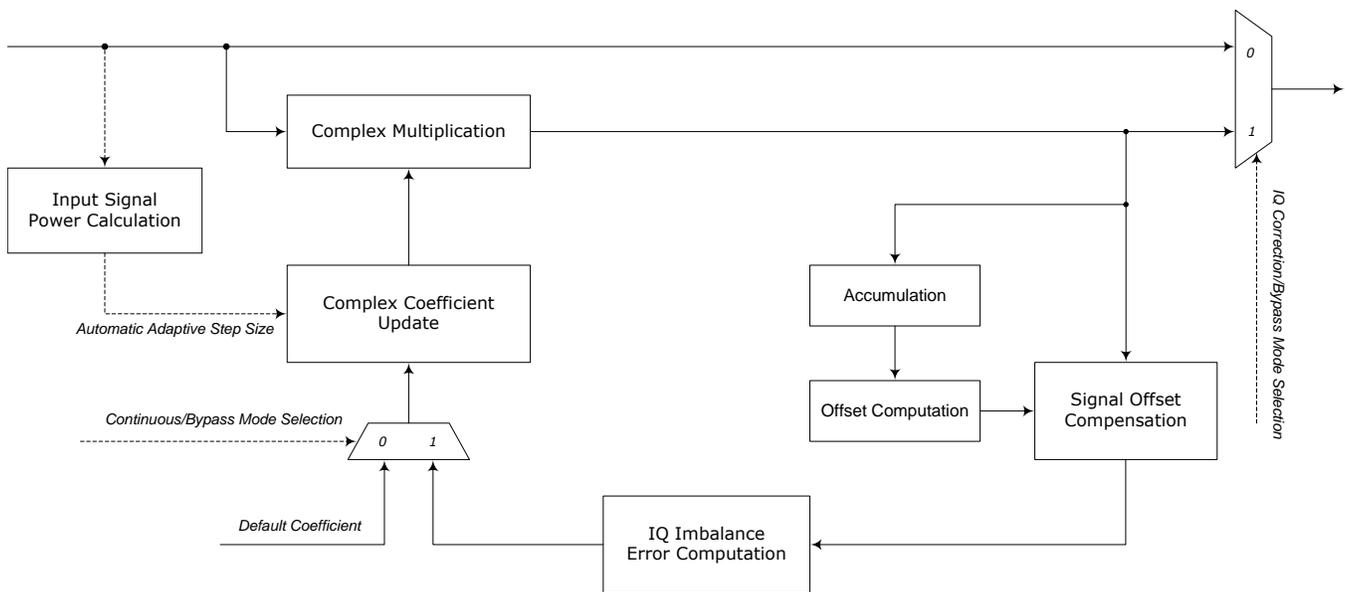
Figure 9. Block Diagram of I/Q Correction in FPGA

Three operating modes are supported in TSW6011EVM:

- Bypass
- Fixed
- Continuous

In bypass mode, the received input signal is multiplexed directly into the input stage of the digital gain control block in the FPGA. In fixed mode, the adaptation algorithm is turned off and the signal is multiplied by the externally-programmed fixed coefficients. This architecture means that the I/Q correction block does not behave adaptively with regards to external environment variables, such as temperature or input power variation. In continuous mode, the adaption loop continuously iterates; four coefficients for complex multiplication are updated at every iteration. The default operating mode is continuous in TSW6011EVM. To show the automatic-adaptive step-size capability of the blind algorithm implemented in the FPGA, apply the fixed and bypass modes.

The blind estimation algorithm for frequency-independent I/Q imbalance uses the properness of second-order statistics of a complex signal. The I/Q correction algorithm in TSW6011 is based on this second-order statistics of the received signal, which means complex signals are mutually independent and uncorrelated with each other. As long as a signal is proper (see note in Section 3), the average energy of I and Q are equal.

As I/Q imbalance in a direct down-conversion system forces the received complex signal to be non-proper and non-circular, I/Q correction algorithm chooses the blind estimation method to correct I/Q imbalance using this concept of orthogonality (properness or circularity). This blind-adaptive digital-signal-processing algorithm is implemented with a single-tap equalizer for the wideband input signals in the FPGA of the TSW6011EVM.

The analog filter inherently includes frequency-dependent I/Q imbalance in a wideband transceiver system. In practice, frequency response from the analog domain, including filter stages, results in frequency-dependent I/Q imbalance.

The blind algorithm based on adaptive single-tap of equalizer in TSW6011 compensates for the I/Q imbalance of received-wideband RF-input signal without the need of a training signal. The analog filter stage has phase/amplitude responses over different frequencies, and these responses contribute to the certain amount of recursiveness in a system. A recursive system means that the output of filter depends on previous values of the output as well as on the current input value. If enough taps exist, the performance of equalizer processing is more robust and stable in the recursive system. Depending on the linearity of the analog filter, even a small number of taps is enough to equalize the I/Q imbalance of the received wideband signal.

Another aspect of I/Q correction performance is the damping ratio of filter specification. Peaking of the amplitude at the edge of filter bandwidth depends on the damping ratio of LPF. And therefore the received signal is impacted less from the filter nonlinearity as the bandwidth of the filter becomes larger than the desired signal bandwidth.

From this point of view, the blocker location in the TSW6011EVM impacts equalizer performance, referring to I/Q correction processing. When the blocker has some frequency offset from the desired signal, the bandwidth of baseband LPF in TRF3711 (I/Q demodulator) is wider than that of the desired signal, implying the received signal stays in a linear zone of filter without severe distortion.

The bandwidth of a LPF in TRF3711 selection and impact on I/Q correction performance is dependent on the blocker location on a wireless receiver system. If the blocker is located at the edge of desired carrier, the bandwidth of a LPF is the same as the carrier bandwidth. This location is the worst case of I/Q correction performance with a single-tap equalizer. The performance of the I/Q correction processing improves as the blocker moves away from the edge of the desired carrier. A signal-tap equalizer achieves good-enough performance depending on blocker location. For example, bypassing the LPF perfectly restores EVM to –51.40 dB as shown in Figure 3, which is approximately –52.67 dB of the original baseband signal as shown in Figure 14 (see the following note).

NOTE: The phase noise of the RF mixer stage in Agilent Signal Generator, E4438C, degrades the error vector magnitude (EVM) of the original baseband signal to –52.67 dB as shown in Figure 14.

3.1.3.3 *DC Offset Compensation*

DC offset is generally caused by LO feedthrough. The feedthrough is typically caused by a hardware issue, a voltage drift of ADC (depending on any temperature variation in the transceiver system), or an I/Q-offset mismatch between the I and Q signals. DC offset is corrected by block-data DC removal, which computes the average bias of the accumulated input signal and subtracts the averaged value from each original input signal. If the received signal has any bias, the bias is reflected to the DC offset, and the properness of the signal is lost. Therefore, DC offset should be compensated before the I/Q imbalance estimation occurs.

DC offset values from each of the I and Q channels are calculated at 122.88 MHz of clock cycle and applied to the input signal at every 1.067 ms (that is: 2^{17} [131,072 samples] × 8.138 ns [122.88 MHz]). This calculation shows a robust iteration time over the slow temperature drift in the system.

DC offset accumulator, $offset_{acc}$, is given by Equation 2.

$$offset_{acc} = \sum_{i=1}^{N} y(i)$$

(2)

The update is given by Equation 3

$$\Delta offset = 2^{-shift} \times offset_{acc}$$

(3)

The offset estimator updated is expressed in Equation 4.

$$offset_{9n+1)} = offset_{(n)} + \Delta offset$$

(4)

The scalar, as shown in Equation 5, implements averaging plus adaptation step size.

$$2^{-shift} = \lambda \times \frac{1}{N}$$

(5)

The offset compensator operates as shown in Equation 6.

$$y_{(i)} = x(i) - offset_{(n)}$$

(6)
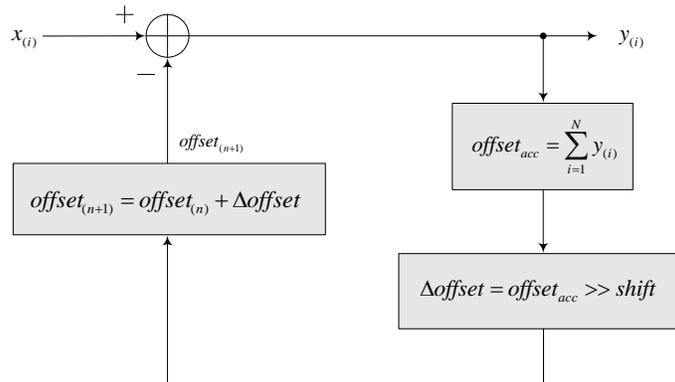
Figure 10. Block Diagram of Offset Compensation in FPGA

3.1.3.4   Digital Gain Block

The gain block implemented in the FPGA is controlled by 0.5-dB step and the range is –3 dB to 18 dB. The block has 43-step of look-up table (LUT) for gain control, and is selected from the Graphical User Interface (GUI) software. Considering the interface with data converters, the bit-width of input from ADS5282 is 12-bits, and is 14-bits for DAC5672. Therefore, there is a 2-bit headroom to the DAC interface, and a shortage of 12 dB with regard to the maximum dynamic range. A lower dynamic range causes SNR and EVM to degrade. In evaluating the I/Q-correction block in the TSW6011EVM, 11.5 dB works as a compensating gain of dynamic range given 0.5 dB of back-off from the incoming signal.

After correcting I/Q mismatch, the digital gain is applied to the received signal for optimum dynamic range of the complex baseband signal. If the digital gain is not applied to the received signal, it degrades the performance of EVM (Error Vector Magnitude) because the received signal still has 2-bit of headroom, causing a lower dynamic range of received signal. Figure 11 illustrates the digital-gain control block of the FPGA.
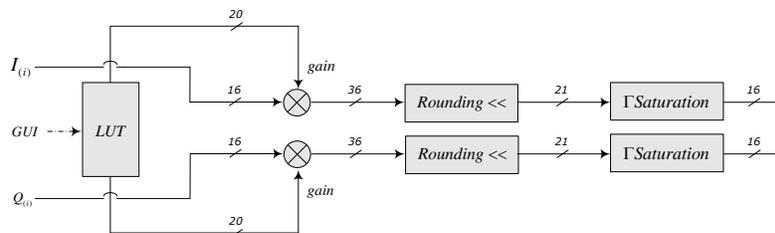
Figure 11. Block Diagram of Digital Gain Control in FPGA

3.1.3.5   2x Interpolation

After I/Q imbalance is corrected with a processing rate of 61.44 Msps, each of the I and Q data are interpolated to 122.88 MHz by a factor of 2 and sent to the DAC interface to measure the signal quality.

3.1.3.6   DQM Mixer

After interpolating the I/Q signal, the signal is then up-converted to 30.72 MHz for the easy measurement by the spectrum analyzer. If the signal is not up-converted, the demodulated signal is located at 0 Hz, making measurement difficult.

4   Component Selection

The TSW6011EVM is a single RX-channel board that demonstrates both the performance of a TRF3711 device and the I/Q correction algorithm implemented in the onboard the FPGA. TSW6011EVM contains a TRF371125 wide-bandwidth, integrated, direct down-conversion demodulator, an ADS5282 octal-ADC for data conversion, a FPGA for adaptive-digital signal processing for I/Q correction, a CDCE62005 clock generator and jitter cleaner to generate the system clocks, and a DAC5672 DAC for ease of performance measurement by a spectrum analyzer.

The TSW6011EVM provides options to send an RF input signal directly to the onboard TRF371125, or through one or two low-noise amplifiers by moving two resistors. Additionally, there is an option to drive two of the ADCs from an external source. This source is either a single-ended (default configuration, through a transformer) or a differential signal. For example, the CMOS output of TRF3711EVM interfaces with the CMOS input of TSW6011 in the chamber for the temperature testing of TRF371125. Bypassing the onboard oscillator with an external source is also an option.

4.1   TRF3711

The TRF3711 includes programmable baseband filters, adjustable DC-offset correction, and buffer amplifiers to directly drive ADCs. The device is suited for operation with WCDMA, WiMAX, and LTE modulation, as well as with other high-bandwidth signal-modulation schemes. The on-chip programmable-gain amplifiers allow adjustment of the output signal level without the need for external variable-gain (attenuator) devices. The TRF3711 integrates programmable-baseband low-pass filters that attenuate nearby interference, eliminating the need for an external baseband filter. The filter of th TRF3711 is an eighth-order Butterworth with 0.7 at approximately 15-MHz (8-bit resolution) programmable bandwidth which covers 1.4 MHz to 30 MHz of complex signal BW.

The features of the TRF371125 inclue:

- Frequency range up to 4 GHz
- Integrated baseband-programmable-gain amplifier
- On-chip programmable-baseband filter
- High out-of-band IP3: 24 dBm at 2400 MHz
- High out-of-band IP2: 60 dBm at 2400 MHz
- Single supply: 4.5- to 5.5-V operation
- Silicon Germanium technology

4.2   ADS5282

The ADS528x is a family of high-performance, low-power, octal-channel ADCs. The ADS528x is available in either a 9 mm × 9 mm QFN-package or an HTQFP-80 package, with serialized low-voltage differential-signaling (LVDS) outputs and a wide variety of programmable features. The ADS528x is highly customizable for a diversity of applications and offers an unprecedented level of system integration.

The features of the ADS5282 include:

- 12-bit resolution with 65-Msps sampling speed
- Low power dissipation: 48 mW per channel at 30 Msps, 55 mW per channel at 40 Msps, 64 mW per channel at 50 Msps, 77 mW per channel at 65 Msps
- 70 dBFS of SFDR at 10 MHz of IF
- Analog input full-scale range: 2-Vpp
- Low-Frequency noise-suppression mode
- 6-dB overload recovery in one clock
- 3.3 V of analog supply and 1.8 V of digital supply
- Programmable digital gain: –3 to 18 dB
- Serialized LVDS Double Data Rate (DDR) output

This device is applicable for medical imaging, wireless base-station infrastructure, and test and measurement instrumentation.

4.3 CDCE62005

The CDCE62005 has five to ten output-clock generators with jitter cleaner and integrated dual VCOs. The features of this device include:

- Frequency synthesizer with PLL and VCO, and a partially-integrated loop filter.
- Fully configurable outputs including frequency, output format, and output skew
- Integrated EEPROM determines device configuration at power-up
- Universal output blocks support up to 5-differential, 10-single-ended, or combinations of differential or single-ended.
- 0.35 ps of RMS (10 KHz to 20 MHz) output jitter performance
- Low output phase noise: –130 dBc/Hz at 1-MHz offset, Fc = 491.52 MHz

Applications of this device include data-converter and data-aggregation clocking, wireless infrastructure, switches and routers, medical electronics, military, aerospace, clock generation, and jitter cleaning.

5 Test Procedures and Equipment Setup

5.1 Test Signal Specifications and Direct Measurement of Error Vector Magnitude

The EVM of a given test signal, excluding degradation, from the hardware setup is important to understand. Figure 12 shows the direct measurement from the E4438C to the MXA signal analyzer. The WiMAX test signal is downloaded onto E4438C with a scaling factor of 70% before starting the measurement. With this test, identify approximately how much the evaluation module (including the onboard VCXO for ADC and DAC) contributes to the EVM degradation
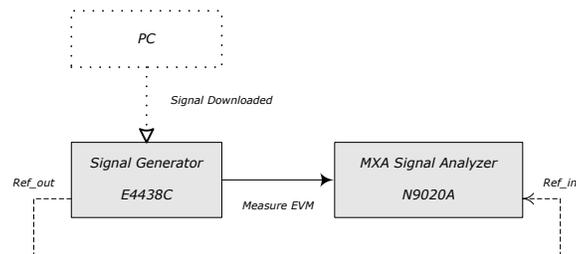
Figure 12. Setup for Direct Measurement of EVM

Figure 13 shows the time domain analysis of the WiMAX test signal. The start of every frame is a preamble, followed by the frame control header (FCH) burst. The preamble is used for synchronization, contains BPSK-modulated carriers, and is one OFDMA-symbol long. The preamble is power-boosted to a level that is a few decibels higher than the level of the subsequent data busts. According to the IEEE802.16e standard, preamble subcarriers can be boosted by maximum 9 dB, but only every third subcarrier is generally used. The mean power of the preamble is 9 dB – 4.77 dB = 4.23 dB above the mean power of the data signal. Considering the existence of pilot tones in data burst, the boosting factor of the preamble is approximately 4 dB above the data burst, but the peak-to-average ratio (PAR) is relatively smaller than that of data burst. IEEE802.16m specifies the magnitude boosting levels of preamble for different Fast Fourier Transform (FFT) sizes and number of antennas.
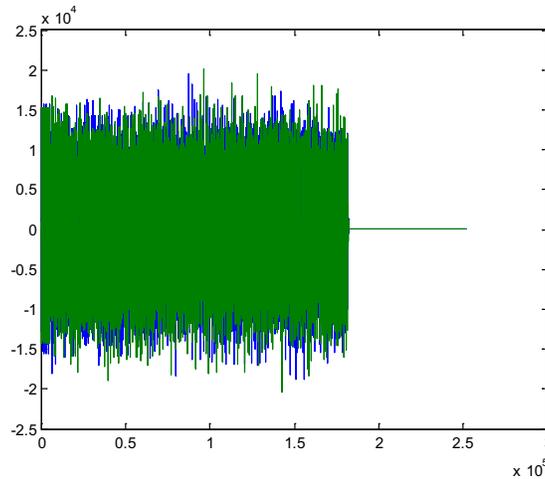
Figure 13. Time Domain Analysis of WiMAX Signal

Direct measurement produces –52.67 dB (or 0.23%) of baseband EVM, as shown in Figure 14. This result includes the degradation of EVM from the phase noise of the LO for up-conversion in the E4438C and for down-conversion of the demodulation function in the MXA signal analyzer.
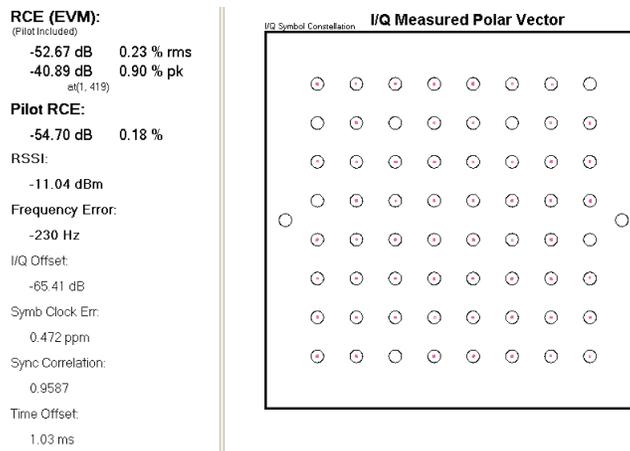
Figure 14. EVM of WiMAX Signal from Direct Measurement

5.2 Equipment Setup

The test environment, illustrated in Figure 15, is configured according to these parameters:

- Test signal: 11.2 Msps with 64 QAM of WiMAX TDD 1-carrier 10-MHz BW
- Architecture: Direct Down-Conversion
- External LO (HP 8673H): 2500 MHz and 0 dBm
- Measuring Equipment: MXA N9020A
- Target board: TSW6011

For EVM measurements, the signal is down-converted to the baseband (zero-IF) using the TRF3711 and the TSW6011. The system uses digital logic to up-convert the baseband signal back to IF (30.72 MHz) for ease of measurement
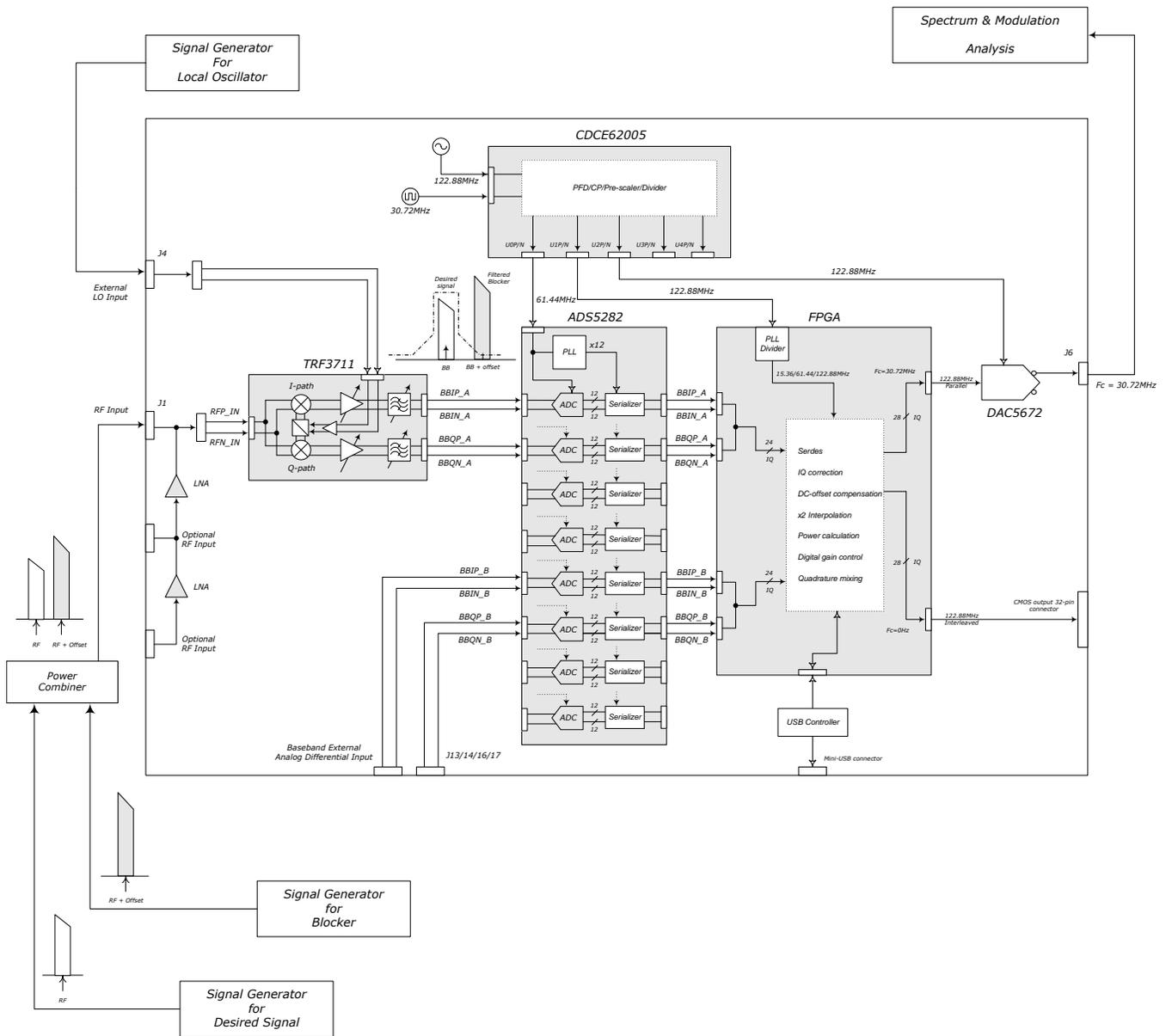
Figure 15. Block Diagram of Test Setup for TSW6011

Figure 16 describes how to setup the temperature chamber test, if necessary. The baseband-differential I and Q signals out of the TRF3711EVM are fed into differential I and Q ports on the TSW6011, and then sent to the ADS5282 for ADC process. From theTRF3711EVM, the bandwidth of the baseband low-pass filter is adjusted to eliminate the blocker on the receiver path.
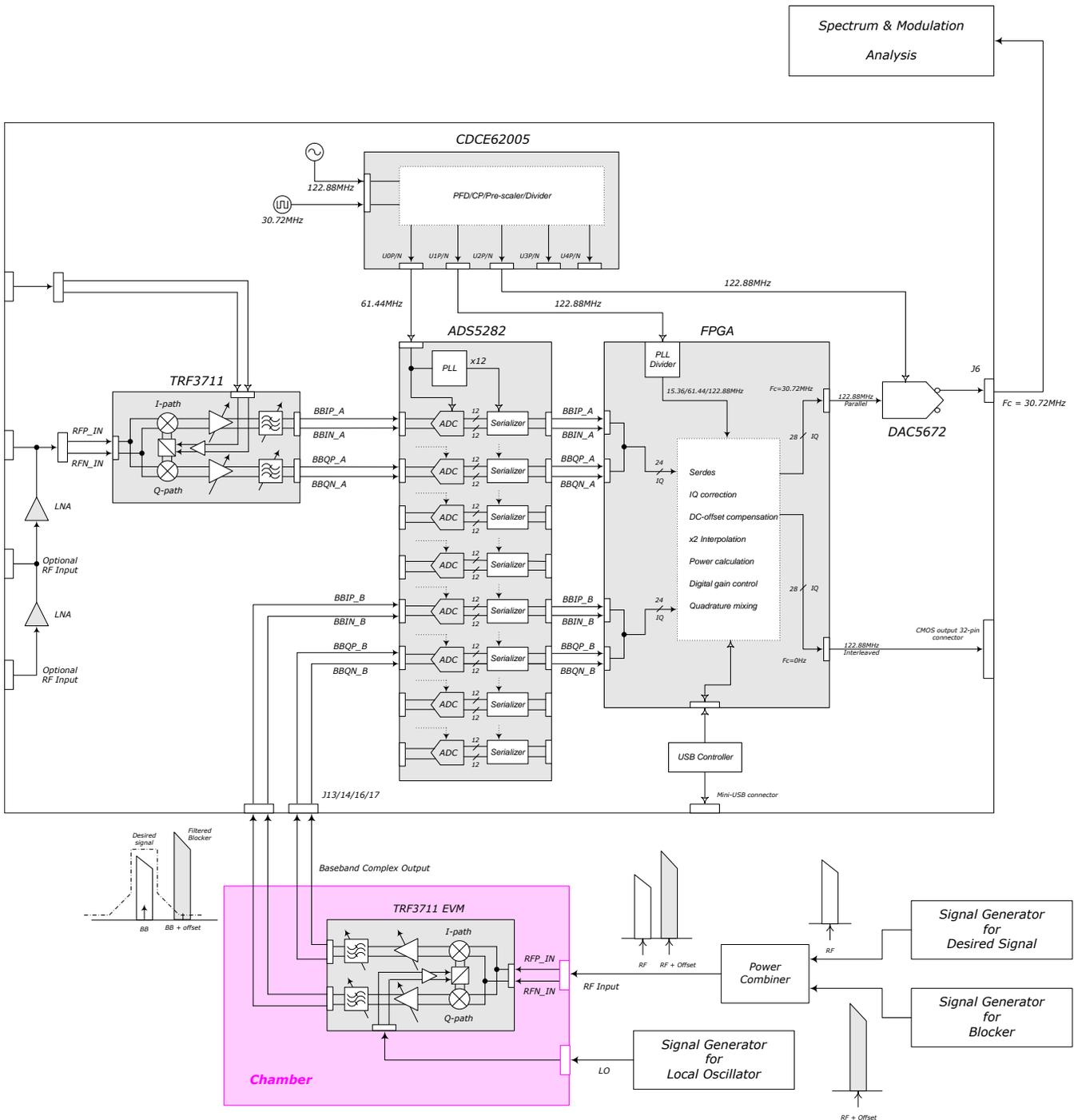
Figure 16. Block Diagram of Temperature Test Setup for TRF3711 and TSW6011

6 Verified Performance

6.1 EVM Improvement Bypassing the TRF3711 LPF

Figure 17 shows –35.66 dB of EVM with bypassing LPF before the I/Q correction processing. The I/Q correction block in the TSW6011 improves the EVM to –51.4 dB as shown in Figure 18.
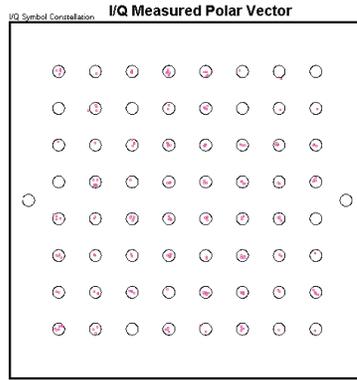
Figure 17. EVM Without LPF (Before I/Q Correction)   Figure 18. EVM Without LPF (After I/Q Correction)
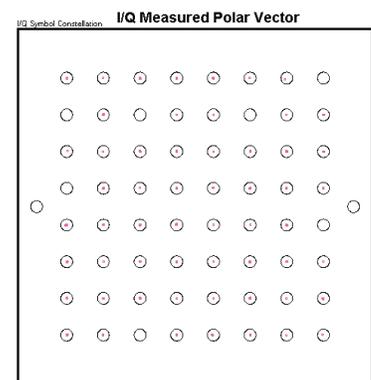
6.2 EVM Improvement Using Various Blocker Locations Along With Appropriate LPF BW

Figure 19 illustrates the RF input signal and the adjacent blocker to the TSW6011EVM.
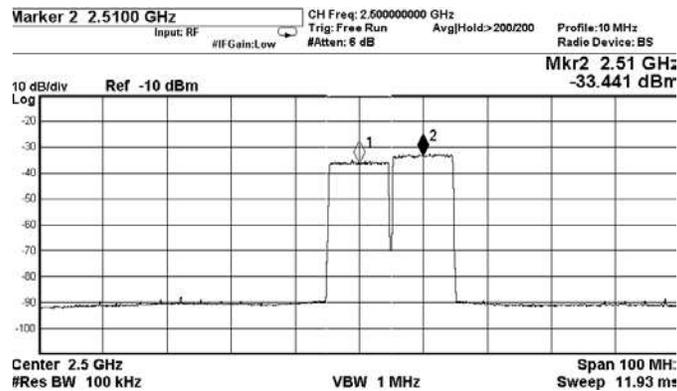
Figure 19. RF Input Signal With Adjacent Blocker (10-MHz Offset)

Figure 20 and Figure 21, respectively, show –35.24 dB of EVM with 10 MHz of LPF BW. The I/Q correction block in TSW6011 improves EVM to –47.49 dB.
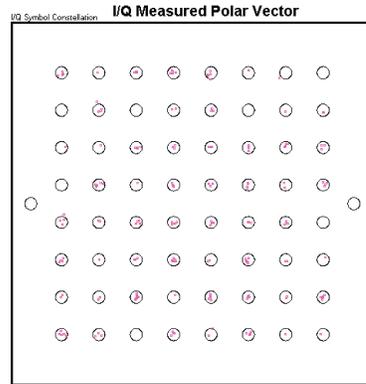
Figure 20. EVM With 10 MHz LPF BW (Before I/Q Correction)
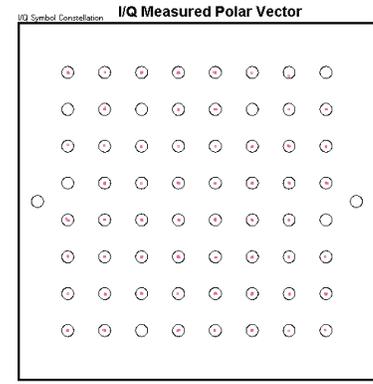
Figure 21. EVM With 10 MHz LPF BW (After I/Q Correction)

Figure 22 illustrates the RF input and blocker signal with 13 MHz of offset between the center-to-center to the input stage of TSW6011
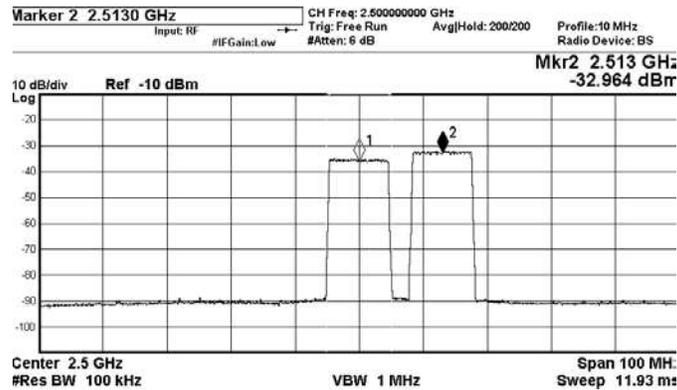
Figure 22. RF Input Signal With Blocker at 13-MHz Frequency Offset

Figure 23 and Figure 24, respectively, show –35.47 dB of EVM with 16 MHz of LPF BW. The I/Q correction block in the TSW6011 improves EVM to –48.06 dB.
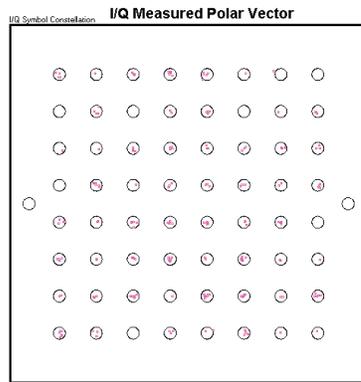
Figure 23. EVM With 16 MHz of LPF BW (Before I/Q Correction)
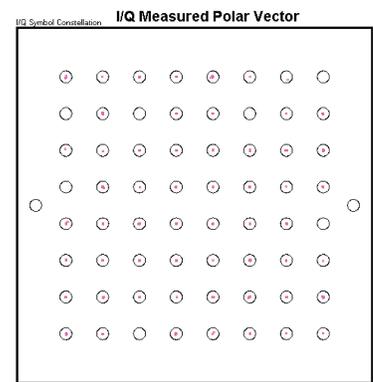
Figure 24. EVM With 16 MHz of LPF BW (After I/Q Correction)

Figure 25 illustrates the RF input and blocker signal with 15 MHz of offset between the center-to-center to the input stage of TSW6011.
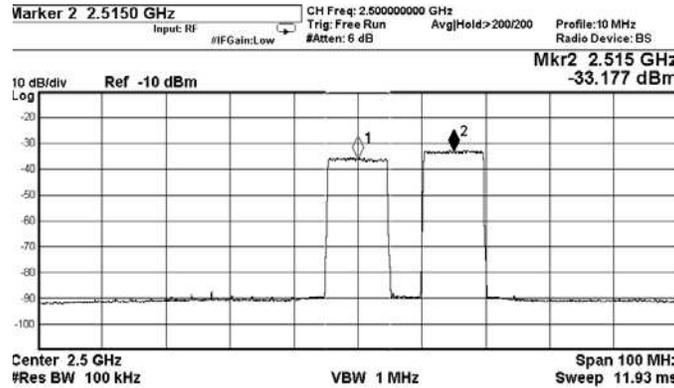
Figure 25. RF Input Signal With Blocker at 15-MHz Frequency Offset

Figure 26 and Figure 27, respectively, show –35.93 dB of EVM with 20 MHz of LPF BW. The I/Q correction block in the TSW6011 improves EVM to –49.51 dB.
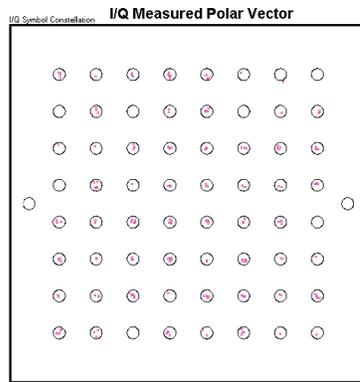
Figure 26. EVM With 20MHz of LPF BW (Before I/Q Correction)
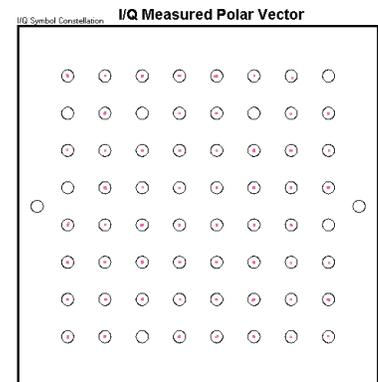
Figure 27. EVM With 20 MHz of LPF BW (After I/Q Correction)

Figure 28 illustrates the RF input and blocker signal with 20 MHz of offset between the center-to-center to the input stage of TSW6011.
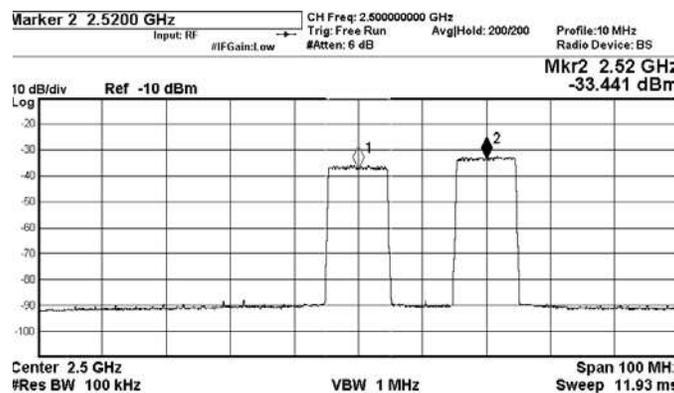
Figure 28. RF Input Signal With Blocker at 20-MHz Frequency Offset

Figure 29 and Figure 30, respectively, show –35.99 dB of EVM with 20 MHz of LPF BW. The I/Q correction block in TSW6011 improves EVM to –50.23 dB.
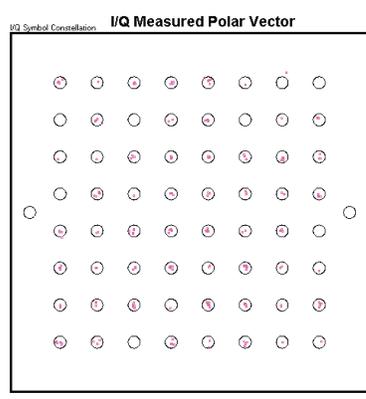
Figure 29. EVM With 30 MHz of LPF BW (Before I/Q Correction)
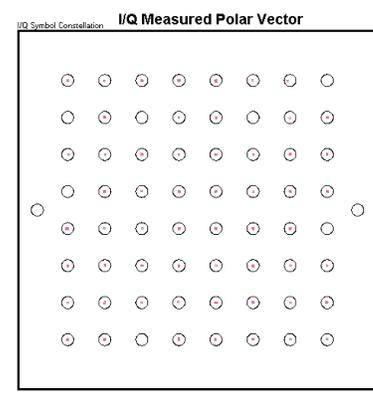
Figure 30. EVM With 30 MHz of LPF BW (After I/Q Correction)

7   Summary

Table 1 shows the EVM performance with different low-pass filter bandwidth over a different blocker location in TSW6011EVM. The nonlinearity of the TRF3711 low-pass filter affects the performance of I/Q correction. The worst-case scenario for the receiver operation shows –47.49 dB of EVM using a WiMAX TDD test signal after I/Q correction, improving by 12.25 dB.

12.25 to 15.74 dB of the EVM improved by I/Q correction, based on the low-pass filter bandwidth of TRF3711. Approximately 3.5 dB of EVM is degraded by 10 MHz of low-pass filter bandwidth compared to using the bypass mode of the TRF3711 low-pass filter. The low-pass filter bandwidth of TRF3711 is scalable up to 30 MHz and greatly depends on the blocker location. As the distance between blocker locations and the edge of the carrier increases, the low-pass filter bandwidth also increases improving the corresponding performance of I/Q correction processing, as shown in Table 1.

The measured results shown in Table 1 are the same as the temperature-chamber test shown in Figure 14 over different temperatures at –45°C, +45°C, and +85°C.

Table 1. Measured EVM Versus Various LPF BW of TRF3711

LPF BW from TRF3711	Measured EVM		Achieved Improvement in EVM
	Before I/Q Correction	After I/Q Correction	
10 MHz	–35.24 dB	–47.49 dB	12.25 dB
16 MHz	–35.47 dB	–48.06 dB	12.59 dB
20 MHz	–35.93 dB	–49.51 dB	13.58 dB
30 MHz	–35.99 dB	–50.23 dB	14.24 dB
Bypass	–35.66 dB	–51.40 dB	15.74 dB

8   About the Author

Kyung-wan Nam is a senior applications engineer in the High Speed Data Converter group at Texas Instruments. Prior to joining the TI Wireless Infrastructure Solutions Team in 2009, he supported key customers for wireless system solutions, such as Crest Factor Reduction (CFR) and Digital Pre-Distortion (DPD), at Optichron (Broadcom since 2011) from 2007 to 2009. From 2002 to 2007, he was a senior engineer in the commercial CDMA/WCDMA/M-WiMAX BTS/RRH development team, increasing system efficiency, at Samsung Electronics. Kyung-wan earned his master's degree in electrical and computer engineering from the University of Florida in 2001.

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