TSW3003 Demonstration Kit

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1 Demonstration Kit Configuration Options

The TSW3003 Demonstration (Demo) Kit can be configured in different ways to evaluate different components in different frequency bands. This section outlines the various component configurations. Based on the configuration, testing and board setup must be altered to accommodate the given components and features.

1.1 DAC Component

The TSW3003 Demo Kit is built for the DAC5687, although this Demo Kit can also support the DAC5686 because the two devices are pin compatible. The procedures outlined in this document are primarily suited for the DAC5687, but can be modified easily for the DAC5686 if desired.

1.2 VComm Configuration

The analog quadrature modulator requires a common-mode dc voltage of approximately 3.3 V. In order to use the dc-offset adjustment capabilities of the DAC5687 for carrier suppression, it is imperative to maintain a dc path from the DAC output to the modulator input. The common-mode voltage for the modulator is maintained with a passive resistor network that is designed to provide the proper operation point for the DAC5687 and the TRF3703 modulator. By design, in order to preserve the proper dc levels, the DAC coarse gain should be kept at the maximum (15), though deviation by a few steps is generally acceptable with no degradation in performance.

1.3 VCXO

The CDCM7005 requires a VCXO source to derive its output clock signals. The VCXO is at reference designator U1. The frequency of the VCXO can be changed to operate the Demo Kit with different clocking schemes for different modulation standards or for specific customer requirements. Denote which VCXO frequency is on the board so that the CDCM7005 part can be set up properly. The following conventions are typically used:

- WCDMA: Derivatives of 61.44 MHz (i.e., 122.88 MHz, 245.76 MHz, 491.52 MHz)
- GSM: Derivatives of 52 MHz (i.e., 104 MHz, 208 MHz)
- CDMA2K: Derivatives of 78.6432 (i.e., 157.2864 MHz, 314.5728 MHz)

1.4 LO Generation

The integrated VCO of the TRF3761 outputs the RF signal used for the LO drive on the analog quadrature modulator. The RF output frequency is contingent on the LO frequency value. The default TRF3761-H typically has a tuning range from 2028 to 2175 MHz. Other frequency bands will require the existing TRF3761 to be changed to another pin-compatible part in a different frequency band. Using the TRF3761 internal divider or another TRF3761 part to generate frequencies outside this range requires the output terminations to be changed. Contact TI for support in this situation.

The RF frequency band of the VCO must be noted in order to know how to program the TRF3761 and at what frequency to measure the output RF signal from the modulator. The typical bands of operation are shown in Table 1.

Table 1. Frequency Bands

	UMTS	PCS	GSM900	DCS1800
FREQUENCY	2110-2170 MHz	1930-1990 MHz	935-960 MHz	1805-1880 MHz

2 Block Diagrams

2.1 System Block Diagram

The basic radio system block diagram in Figure 1 demonstrates where the TSW3003 Demo Kit fits in the overall transceiver. The dash-line box illustrates the components found on the TSW3003 Demo Kit board.

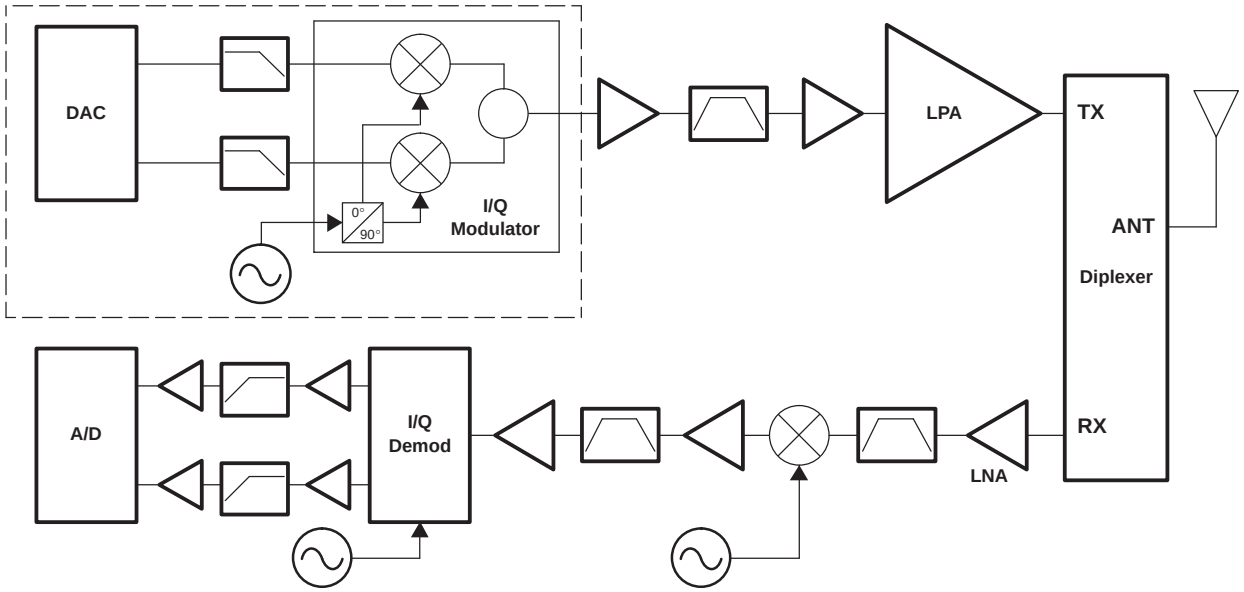


Figure 1. System Block Diagram

2.2 Demo Kit Block Diagram

The basic Demo Kit block diagram is shown in Figure 2. The shaded boxes illustrate the key Texas Instruments components found on the TSW3003 Demo Kit board.

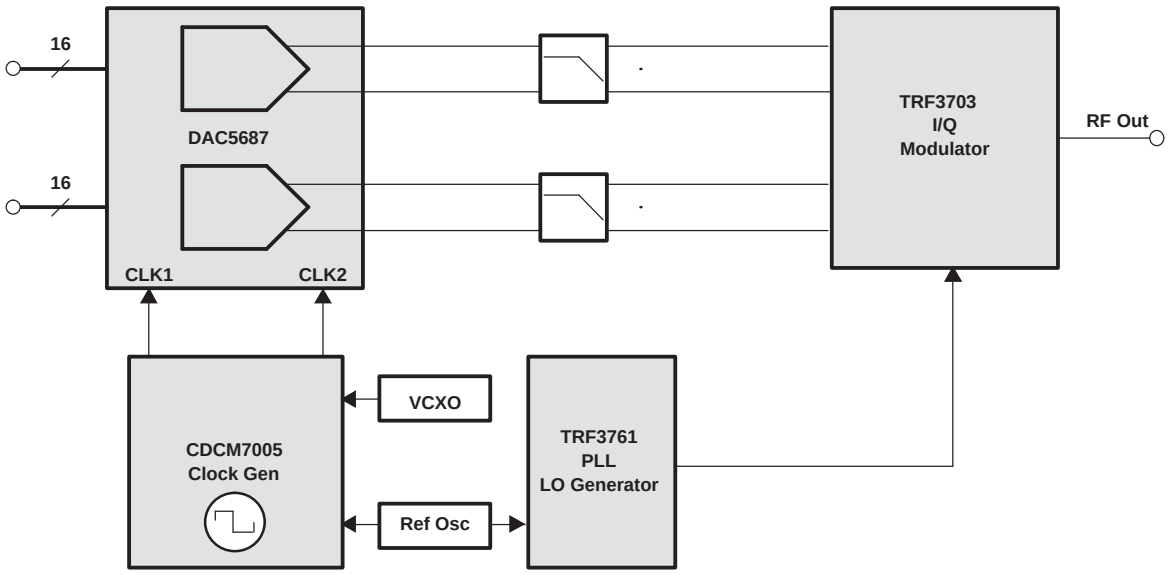


Figure 2. Demo Kit Block Diagram

3 Key Texas Instruments Components

3.1 CDCM7005

The CDCM7005 clock distribution chip is used to generate and synchronize the clock outputs to the system. The device has five outputs which can be either LVPECL or LVCMOS and can be divided down by 1, 2, 3, 4, 6, 8, and 16. The divide by 16 can be replaced with a divide by 4 or 8 with a 90 degree phase shift.

3.2 DAC5687

The DAC5687 is a 16-bit interpolating dual digital-to-analog converter (DAC). The device incorporates a digital modulator, independent differential offset control, and I/Q amplitude control. The device is typically used in baseband mode or in low IF mode with an analog quadrature modulator.

3.3 TRF3703

The TRF3703 is a direct upconversion IQ modulator. This device accepts a differential input voltage quadrature signal at baseband or low IF frequencies and outputs a modulated RF signal based on the LO drive frequency.

3.4 TRF3761

The TRF3761 is a family of high performance, highly integrated frequency synthesizers, optimized for wireless infrastructure applications. The TRF3761 includes an integrated VCO and integer-N PLL. Different members of the TRF3761 family can be chosen for application specific VCO frequency ranges.

4 Software Installation

This section summarizes the installation procedures for the software required to operate the Demo Kit. Once all of the software is loaded, it is recommended to reboot the computer. This software has been verified to be functional on Win2K and WinXP.

- Execute setup.exe
- Reboot computer as required by the Windows™ operating system.
- Power up the TSW3003EVM, and plug in the USB cable.
- Allow the Windows™ operating system to automatically find and install the TSW3003 USB drivers.
- Start the TSW3003 USB Vx.x software.

5 Software Operation

The following describes the use of the software required to set the TSW3003 Demo Kit in the baseline configuration for the CDCM7005, TRF3761, and DAC5687. The software should be configured in the order presented below. The first step requires starting the TSW3003 software. This opens a window as shown in Figure 3. The tabs on the left side of the window allow selection of different GUI controllers for the DAC5687, TRF3761, and CDCM7005. The lower left portion of the screen contains links to this user's guide as well as the data sheets for the DAC5687, TRF3761, and the CDCM7005.

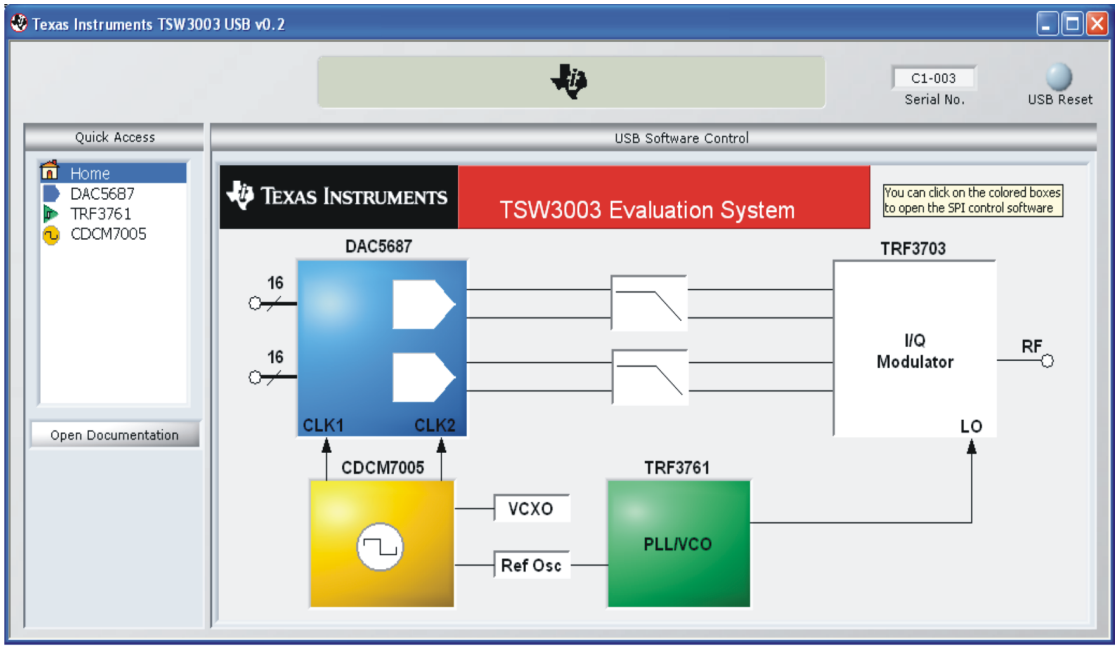


Figure 3. TSW3003 Startup Screen

5.1 CDCM7005 Software

By using the provided CDCM7005 serial peripheral interface (SPI) software, the user can load settings to the CDCM7005 internal registers. This must be performed every time the TSW3003 Demo Kit is powered up, because the CDCM7005 has default settings that are loaded at power up and the settings may be slightly different than the ones required to operate the Demo Kit. Executing the program brings up the interface seen in Figure 4. The default settings are correct for a VCXO of 491.52 MHz and a 10 MHz reference as on the TSW3003. The CDCM7005 GUI allows register settings to be saved and can be loaded back in afterwards. This can be accomplished with the Save and Load Settings buttons near the right side of the GUI.

It is recommended that any unused output clocks be tri-stated. In this case the TSW3003 only uses OUT_MUX_1 to drive the DAC5687. OUT_MUX_0, OUT_MUX_2, OUT_MUX_3, OUT_MUX_4 should be tri-stated unless there is a need to use the other output clocks.

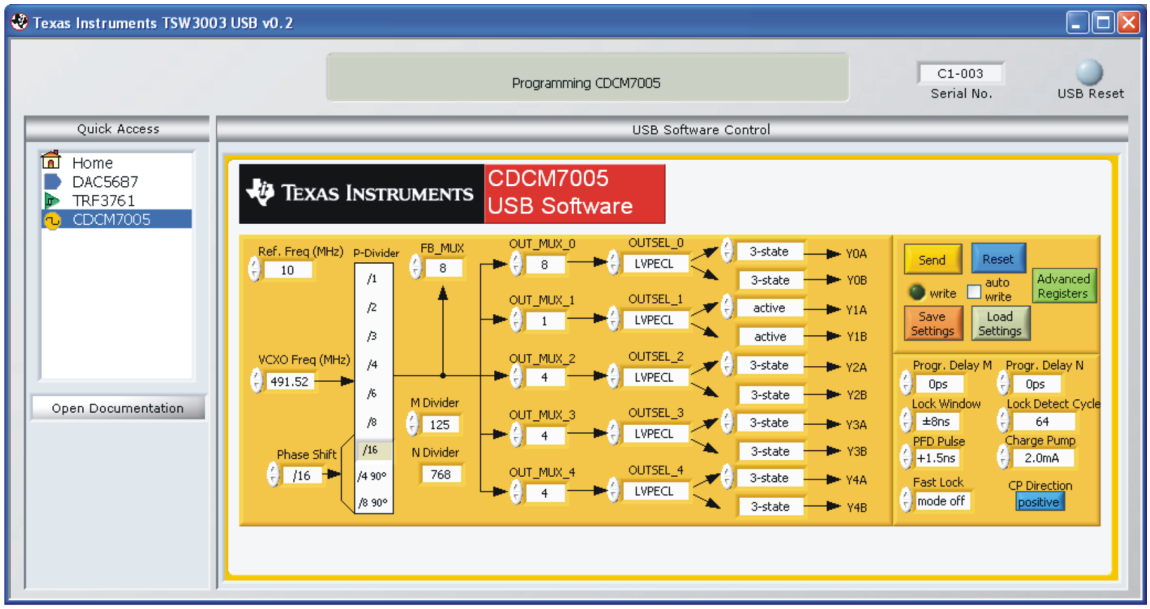


Figure 4. Default CDCM7005 SPI GUI

The divider parameters, M and N, are determined according to the following equation based on the internal reference frequency and internal VCXO frequency.

$F_{REF} = (F_{VCXO} \times M)/(N \times P)$

The p parameter is the VCXO input divider and set through the FB_MUX value. The M and N counter values need to be adjusted depending on the board configuration. The M and N counter registers are determined by the reference frequency and the VCXO frequency. The OUT_MUX sets the divide ratios for the individual output clocks. The OUTSEL determines whether the output clocks will be used as single-ended CMOS or differential LVPECL. With a 10-MHz reference oscillator the CDCM7005 settings are shown in Table 2 for a variety of common VCXO frequencies. A calculator is included in the CDCM7005 GUI software to calculate the M and N values based on Ref and VCXO frequencies.

Table 2. CDCM7005 Register Values

VCXO Freq. (MHz)	491.52	245.76	122.88	61.44
Divider M	125	125	125	125
Divider N	768	768	768	768
FB_MUX	8	4	2	1

5.2 TRF3761 Software

The TRF3761 software is used to program the internal PLL chip to lock the integrated VCO onto a desired frequency output. The main menu of the program is shown in Figure 5.

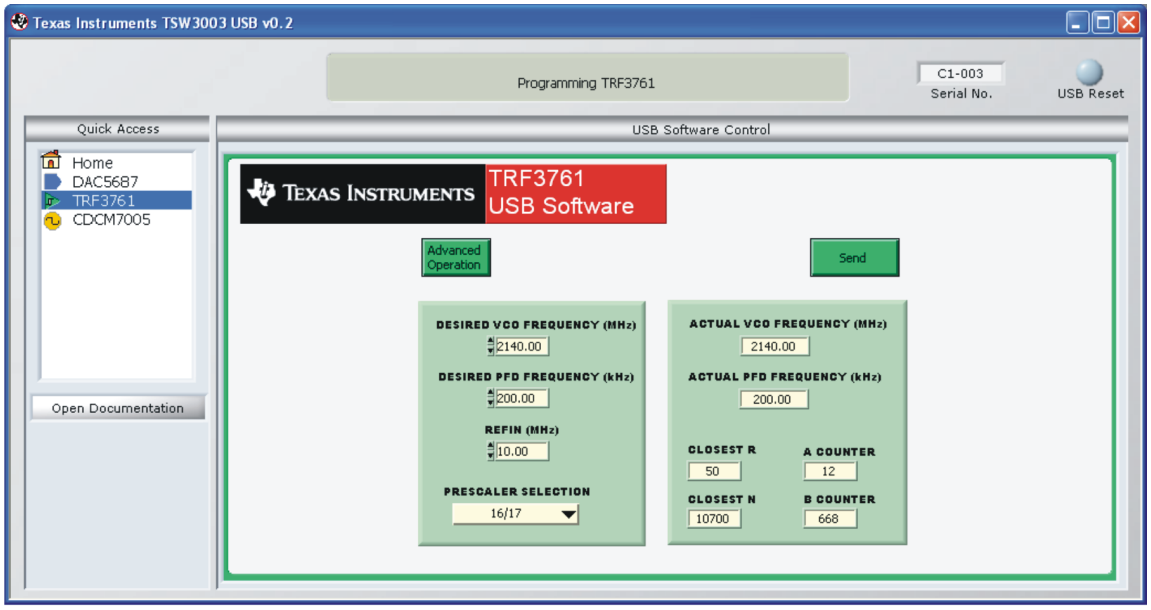


Figure 5. TRF3761 GUI - Main Menu

The options in the front panel allow the user to program the desired frequency of the VCO, the desired frequency of the PFD, the reference frequency, and the prescaler selection. The software then displays the actual VCO frequency, PFD frequency and the R, N, A, and B counter values to be programmed into the TRF3761. Hitting the Send button writes these values to the TRF3761. In default mode on a default board, only the desired VCO frequency (2028 MHz to 2175 MHz) needs to be changed. For other VCO ranges, a different member of the TRF3761 family needs to be selected and other parameters may need to be changed. The Advanced Operation button will bring up another user interface as shown in Figure 6.

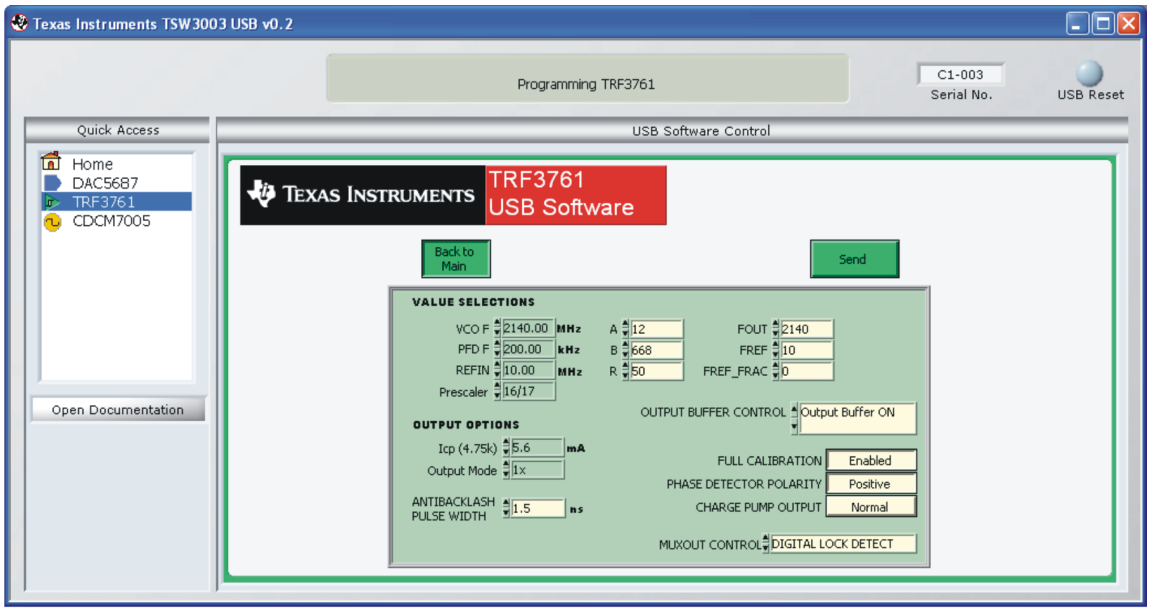


Figure 6. TRF3761 GUI - Advanced Menu

This menu allows control of more register settings. For details on these settings, see the TRF3761 data

sheet (SLWS181). The register of interest in this menu is the MUXOUT CONTROL which can be used to determine the function of LED D4. This mode defaults to Digital PLL Lock Detect and causes the LED D4 to light up when the PLL successfully locks. Normally, these menu settings do not need to be changed. If the divider ratios are changed, the TRF3761 output termination needs to be modified to accommodate the new output frequency. Otherwise, the performance may be degraded. Contact TI in this situation.

5.3 DAC5687 Software

By using the provided software, the user can write and read control register information to the DAC5687. Once the Demo Kit is powered on and connected properly, then the GUI shown in Figure 7 is displayed with the default settings read from the device. If there is a problem with the communication, such as the Demo Kit is not powered on or the USB cable is not connected, an error message will be displayed instructing the user to correct the problem. Once corrected, hit the Read All button to read the default settings of the device.

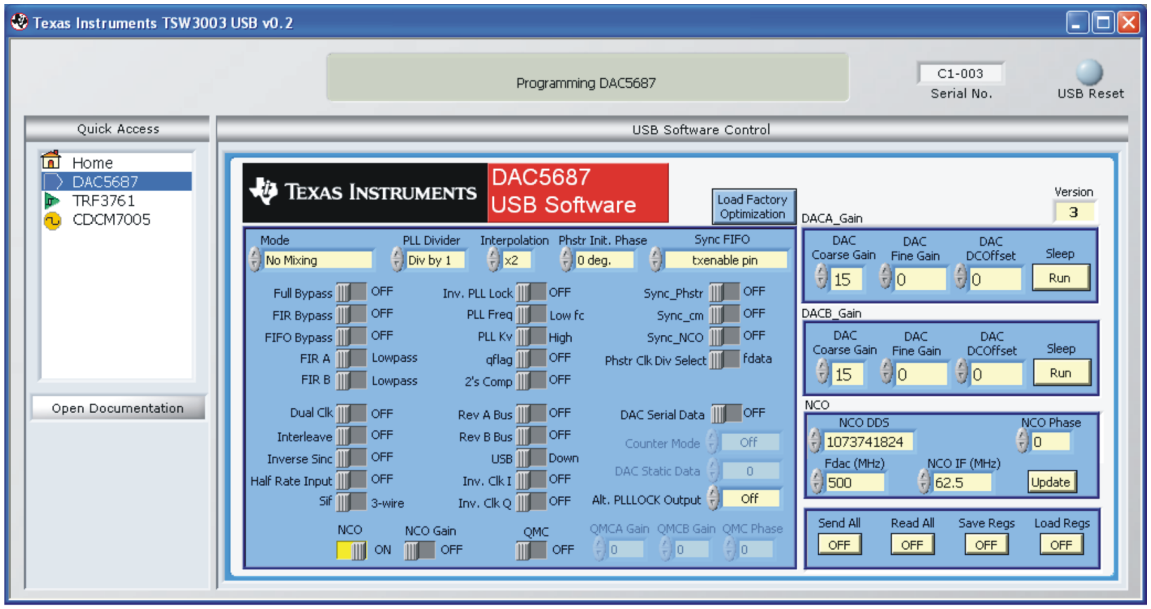


Figure 7. DAC5687 GUI

For normal operation, the user needs only to select values and switches as desired. The values are automatically sent to the device and read back to verify their configuration.

5.4 DAC5687 GUI Register Descriptions

5.4.1 Register Controls

- **Load Regs** – Loads register values from a saved file to the DAC5687 and updates the GUI.
- **Save Regs** – Saves current GUI registers settings to a text file for future use.
- **Read All** – Reads the current registers of the DAC5687. This is used to verify settings on the front panel.
- **Send All** – Sends the current front panel registers to the device. This is generally only used when the Demo Kit power has recycled or the device has been reset and the user wants to load the displayed settings to the device.
- **Load Factory Optimization** – Load default LO and sideband optimized values for the default board condition.

5.4.2 Configuration Controls

- **Full Bypass** – When set, all filtering, QMC, and NCO functions are bypassed.
- **FIR Bypass** – Bypass all interpolation filters. QMC INCO functional. Limited to FDAC = 250 MHz
- **FIFO Bypass** – When set to bypass, the internal four sample FIFO is disabled. When cleared, the FIFO is enabled.
- **FIR A** – A side first FIR filter in high-pass mode when set, low-pass mode when cleared.
- **FIR B** – B side first FIR filter in high-pass mode when set, low-pass mode when cleared.
- **Dual Clk** – Only used when the PLL is disabled. When set, two differential clocks are used to input the data to the chip; CLK1/CLK1C is used to latch the input data into the chip, and CLK2/CLK2C is used as the DAC sample clock.
- **Interleave** – When set, interleaved input data mode is enabled; both A and B data streams are input at the DA(15:0) input pins.
- **Inverse Sinc** – Enables inverse sinc filter.
- **Half Rate Input** – Enables half rate input mode. Input data for the DAC A data path is input to the chip at half speed using both the DA(15:0) and DB(15:0) input pins.
- **Sif** – Sets sif_4-pin bit. A 4-pin serial interface mode is enabled when on, 3-pin mode when off. The DAC5687 Demo Kit is configured for a 3-pin serial interface, so setting to a 4-bit serial interface makes reading registers impossible with the GUI.
- **Inv. PLL Lock** – Only used when PLL is disabled and dual clock mode is disabled. When cleared, input data is latched into the chip on rising edges of the PLLLOCK output pin. When set, input data is latched into the chip on falling edges of the PLLLOCK output pin.
- **PLL Freq** – Sets PLL VCO center frequency to low or high center frequency.
- **PLL Kv** – Sets PLL VCO gain to either high or low gain.
- **Qflag** – Sets qflag bit. When set, the QFLAG input pin operates as a B sample indicator when interleaved data is enabled. When cleared, the TXENABLE rising determines the A/B timing relationship.
- **2's Comp** – When set, input data is interpreted as 2's complement. When cleared, input data is interpreted as offset binary.
- **Rev A Bus** – When cleared, DA input data MSB to LSB order is DA(15) = MSB and DA(0) = LSB. When set, DA input data MSB to LSB order is reversed, DA(15) = LSB and DA(0) = MSB.
- **Rev B Bus** – When cleared, DB input data MSB to LSB order is DB(15) = MSB and DB(0) = LSB. When set, DB input data MSB to LSB order is reversed, DB(15) = LSB and DB(0) = MSB.
- **USB** – When set, the data to DACB is inverted to generate upper side band output.
- **Inv. Clk I(Q)** – Inverts the DAC core sample clock when set, normal when cleared.
- **Sync_Phstr** – When set, the internal clock divider logic is initialized with a PHSTR pin low to high transition.
- **Sync_cm** – When set, the coarse mixer is synchronized with a PHSTR low-to-high transition.
- **Sync_NCO** – When set, the NCO phase accumulator is cleared with a phstr low-to-high transition.
- **Phstr Clk Div Select** – Selects the clock used to latch the PHSTR input when restarting the internal clock dividers. When set, the full rate CLK2 signal latches PHSTR and when cleared, the divided down input clock signal latches PHSTR.
- **DAC Serial Data** – When set, both DAC A and DAC B input data is replaced with fixed data loaded into the 16-bit serial interface DAC Static Data.
  - **Counter Mode** – Controls the internal counter that can be used as the DAC data source: {off; all 16b; 7b LSBs; 5b MIDs; 5b MSBs}.
  - **DAC Static Data** – When DAC Serial Data is set, both DAC A and DAC B input data is replaced with fixed data loaded with this value. Range = 0 - 65535.
- **Alt. PLLLOCK Output** – Can be used to determine alternate outputs on the PLLLOCK pin when using the internal PLL mode. The EXTLO pin must be open when using this mode.
- **NCO** – When set, enables NCO.
  - **NCO Gain** – Sets NCO gain resulting in a 2x increase in NCO output amplitude. Except for $F_S/2$ and $F_S/4$ mixing NCO frequencies, this selection can result in saturation for full-scale inputs. Consider using QMC gain for lower gains.

- **QMC** – When set, enables the QMC.
  - **QMCA Gain** – Sets QMC gain A to a range = 0 to 2047. See the data sheet for more information.
  - **QMC B Gain** – Sets QMC gain B to a range = 0 to 2047. See the data sheet for more information.
  - **QMC Phase** – Sets QMC phase to a range = -512 to 511. See the data sheet for more information. Used to adjust for I/Q phase imbalance.
- **Mode** – Used to select the coarse mixer mode. See the DAC5687 data sheet for more information.
- **PLL Divider** – Sets VCO divider to div by 1, 2, 4, or 8.
- **Interpolation** – Sets FIR Interpolation factor: {X2, X4, X4L, X8}. X4 uses lower power than 4xL, but F_{dac} = 320 MHz max when NCO or QMC are used.
- **Phstr Init. Phase** – Adjusts the initial phase of the FS/2 and FS/4 CMIP block at PHSTR.
- **Sync FIFO** – Sync source selection mode for the FIFO. When a low to high transition is detected on the selected sync source, the FIFO input and output pointers are initialized. See the DAC5687 data sheet for source description.

5.4.3 DAC A(B) Gain

- **DAC Coarse Gain** – Sets coarse gain of DAC A(B) full-scale current. Range is 0 to 15. See the DAC5687 data sheet for full-scale gain equation.
- **DAC Fine Gain** – Sets fine gain of DAC A(B) full scale current. Range is -128 to127. See the DAC5687 data sheet for full-scale gain equation. Used to adjust for I/Q amplitude imbalance.
- **DAC DCOffset** – Sets DAC A(B) dc-offset register. Range is -4096 to 4095. Used to adjust for carrier suppression.
- **Sleep** – DAC A(B) sleeps when set, operational when cleared.

5.4.4 NCO

- **NCO DDS** – Sets NCO DDS registers. See the DAC5687 data sheet for formula.
- **NCO Phase** – Sets initial NCO phase registers. See the DAC5687 data sheet for more information.
- **F_{DAC} (MHz), NCO IF (MHz)** – Used to calculate the required NCO DDS value.

5.4.5 Additional Control/Monitor Registers

- **Version** – Displays the version of the silicon. If a version of 0 is read then the communication is not functioning and an error message will be displayed.

6 Board Setup

6.1 Jumper Settings

The TSW3003 Demo Kit has onboard jumpers that allow the user to selectively disengage devices as desired. The unit is shipped with jumpers in place that activate all of the devices on board. Table 3 explains the functionality of the jumpers on the board.

Table 3. Jumper List

Jumper	Label	Function	Condition	Default
JP1	VCXOB	Choose internal VCXO or external VCXO INB	Internal VCXO	Pin 1, 2
JP2	VCXO	Choose internal VCXO or external VCXO INA	Internal VCXO	Pin 1, 2
SJP3	SJP3	Choose 1.8 or 2.1 VDD	1.8 VDD	Pin 1, 2
JP6	REF CLK	Choose internal 10-MHz ref or external ref	10 MHz	Pin 2, 3
JP8	DEFAULT 3.3VA	Choose 3.3V or 1.8V for IOVDD	3.3 VDD	Pin 1, 2
J31-2	PLL_VDD	PLLVDD GND (OFF) or 3.3V (ON)	GND	Pin 1, 2
J31-5	SLEEP	SLEEP GND (ACTIVE) or 3.3V (SLEEP)	GND	Pin 4, 5
J31-8	EXTLO	Internal (GND) or external (3.3V) voltage reference	GND	Pin 7, 8
J31-11	TX_ENABLE	High enable data for DAC	3.3 V	Pin 11, 12
J31-14	TESTMODE	GND	GND	Pin 22, 23
J31-17	No Connect			
J31-20	$\overline{\text{CDC}}$_PD	Low active power down of CDCM7005	3.3 V	Pin 20, 21
J31-23	PD_OUTBUF	Power down output buffer of TRF3761	GND	Pin 22, 23
J31-26	CHIP_EN	Enable TRF3761 chip	3.3 V	Pin 26, 27
J31-29	$\overline{\text{RESET}}$	Low active reset of DAC5687	3.3 V	Pin 29, 30
J31-32	$\overline{\text{PLLLCK}}$_EN	Low active PLLLOCK output buffer	GND	Pin 31, 32
J31-35 (1)	No Connect			

(1) VCXO does not have Output Enable control.

6.2 Input/Output Connectors

The input and output connections are shown in Table 4.

Table 4. Input/Output Connections

Reference Designator	Connector Type	Description
J1	Power Connector	6 VDC from wall adapter
J4	34-pin header	External VCXO connection
J7	SMA	Optional input clock from CDCM7005
J8	SMA	Optional input clock from CDCM7005
J9	SMA	Optional input clock from CDCM7005
J27	SMA	PLLLLCK output from DAC5687, used to indicate lock or to drive external data source
J29	34-pin header	DA input to the DAC5687
J30	34-pin header	DB input to the DAC5687
J32	SMA	RF output from modulator
J34	USB	USB connector for GUI software
J35	SMA	External Ref clock input
J37	Banana Plug	+6-VDC connector for external DC supply
J38	Banana Plug	GND connection for external DC supply

6.3 USB Port

The TSW3003 Demo Kit contains a 4-pin USB port connector (J34) to interface to a standard computer USB port. Programming of the CDCM7005, DAC5687, and TRF3761 are accomplished through this port.

6.4 DC Power Requirements

The Demo Kit requires a single dc-voltage supply that is nominally 6 V. From that supply, the 5 V, 3.3 V, and 1.8 V required for the devices on the board are generated internally through linear voltage regulators. It is possible to use a higher input voltage; however, care should be taken not to over dissipate the onboard voltage regulators.

7 Demo Kit Test Configuration

7.1 Test Setup Block Diagram

The test set up for general testing of the TSW3003 Demo Kit is shown in Figure 8.

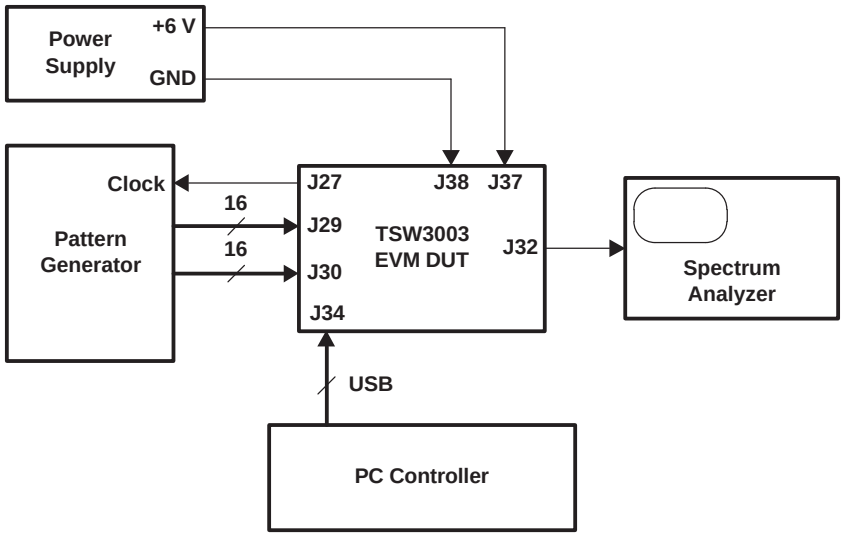


Figure 8. Test System Block Diagram

7.2 Test Equipment

The following is a list of the test equipment required for testing the TSW3003 Demo Kit. Equivalent models may be used for certain applications, but may produce different results due to limitations within the instrument.

- Dual Power Supply: Any with current readout capability or use the supplied 6VDC 4A wall supply
- Spectrum Analyzer: Rhode & Schwartz FSU, Agilent PSA, or equivalent

  This particular piece can measure >70-dBc ACPR with the noise cancellation option active. This amount of dynamic range is required to accurately measure the ACPR of the Demo Kit. Another spectrum analyzer can be substituted if it achieves as good or better dynamic range.
- Pattern Generator: Agilent 16720A
- Oscilloscope: Tektronix 650 or equivalent

  Used to probe clock output signals and for debugging.
- Digital Voltmeter: Agilent 34401A or equivalent

7.3 Calibration

In order to record proper output power the insertion loss of the output cable must calibrated. Measure the insertion loss of the cable from J32 to the spectrum analyzer; set the analyzer's reference level offset to that value.

7.4 Test Specifications

The test specifications are outlined in Table 5.

Table 5. Demo Kit Typical Specifications

	MIN	MAX	UNITS
CURRENT			
+6 V		1.5	A
CW TESTS			
Carrier suppression	30		dBc
Sideband rejection	25		dBc
Spurious Output			
2nd harmonic	45		dBc
Aliased LSB (pos)	40		dBc
Output clock	40		dBc
Aliased USB	15		dBc
Aliased USB (neg)	8		dBc
WCDMA ACPR			
Channel power		-14	dBm
ACPR -Low	76		dBc
ACPR -High	76		dBc

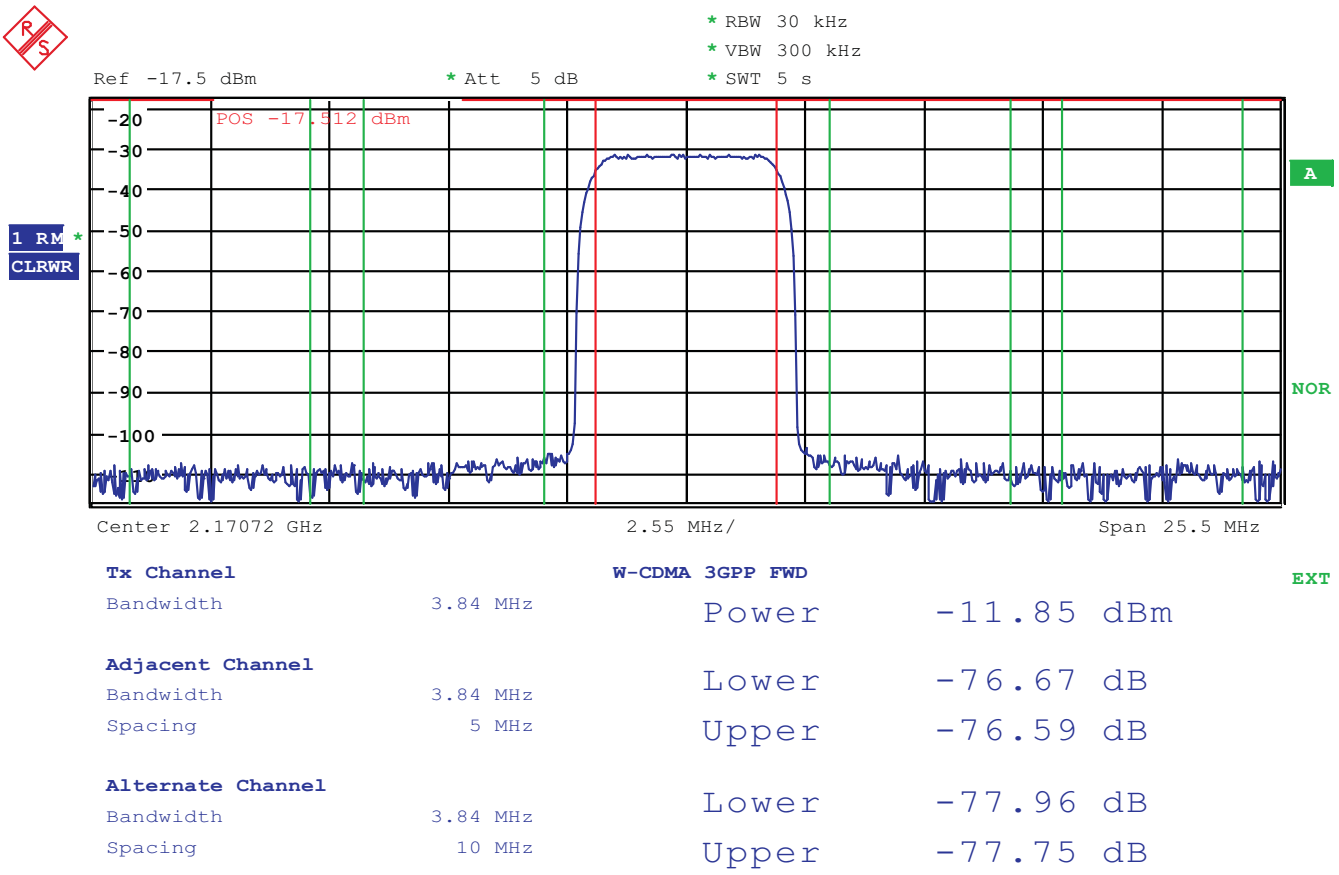


Figure 9. Single-Carrier Test Mode 1 WCDMA, Typical Performance With IF=30.72 MHz, LO=2.14 GHz

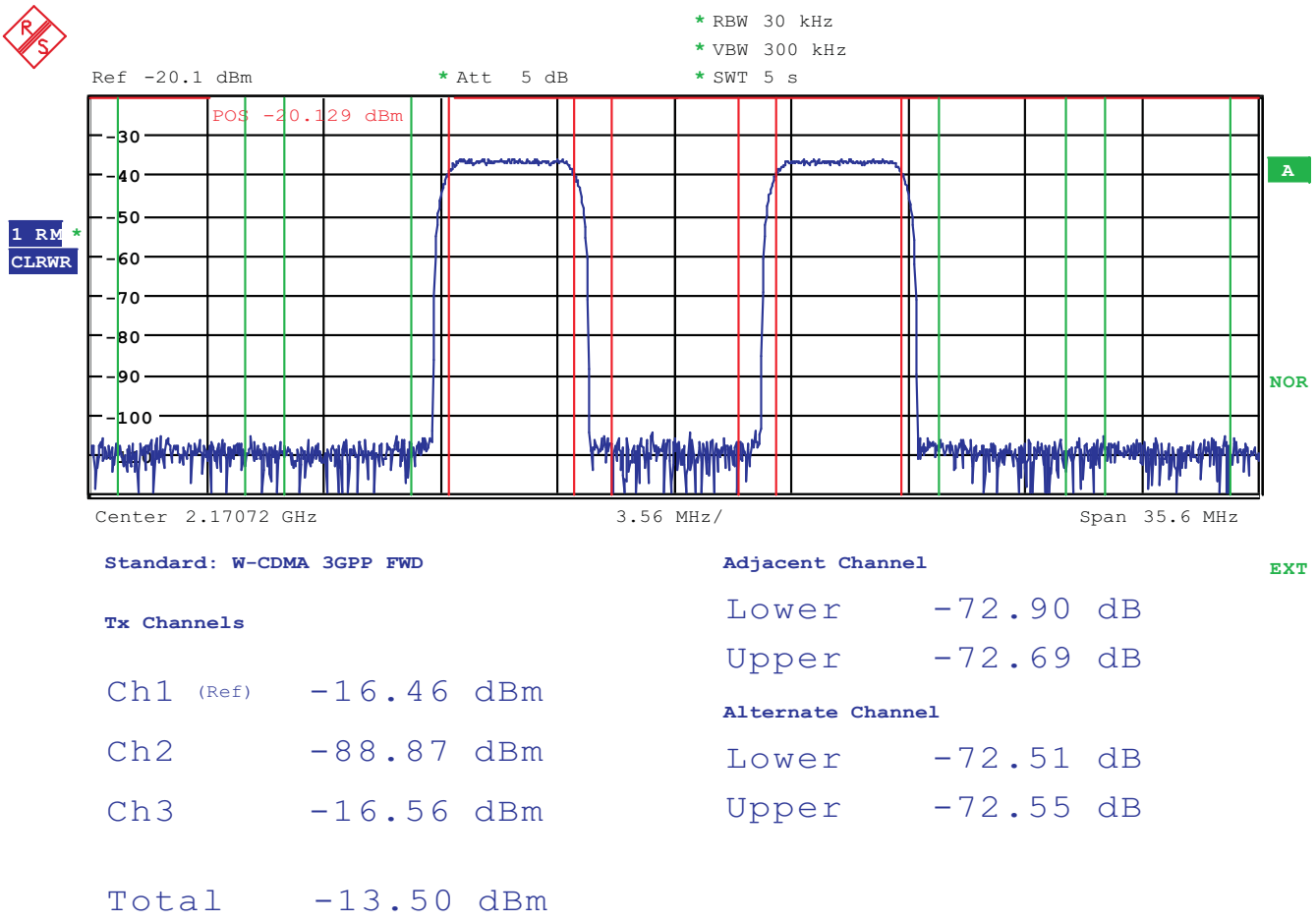


Figure 10. Missing Middle-Carrier Test Mode 1 WCDMA, Typical Performance With IF=30.72 MHz, LO=2.14 GHz

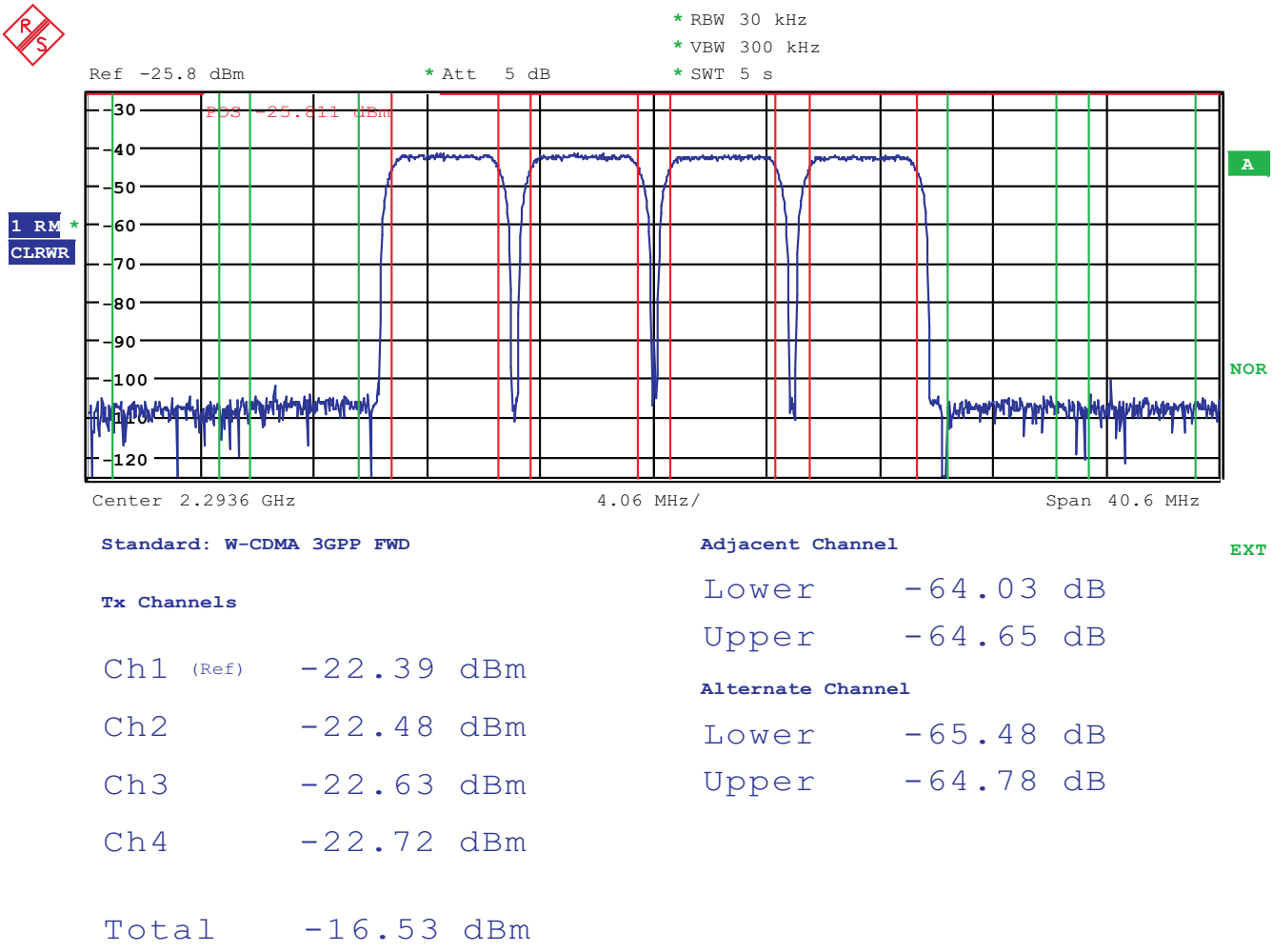


Figure 11. Four-Carrier Test Mode 1 WCDMA, Typical Performance With IF=153.6 MHz, LO=2.14 GHz

7.5 WCDMA Output Power Versus ACPR Performance

The ACPR has some dependency on the output power of the TSW3003. The RF output spectrum shows some IMD effects as the output power of the DAC is increased. The optimum ACPR performance occurs when there is approximately a -6dB attenuation pad between the DAC output and the TRF3703 input. As the power is increased the IMD3 effects start to affect the ACPR. As the power is decreased, the ACPR becomes linear as a function of the signal power and the noise floor.

The ACPR results have been tabulated in Figure 12 through Figure 15 for 1, 2, 3, and 4 WCDMA carriers with the TM1 signal.

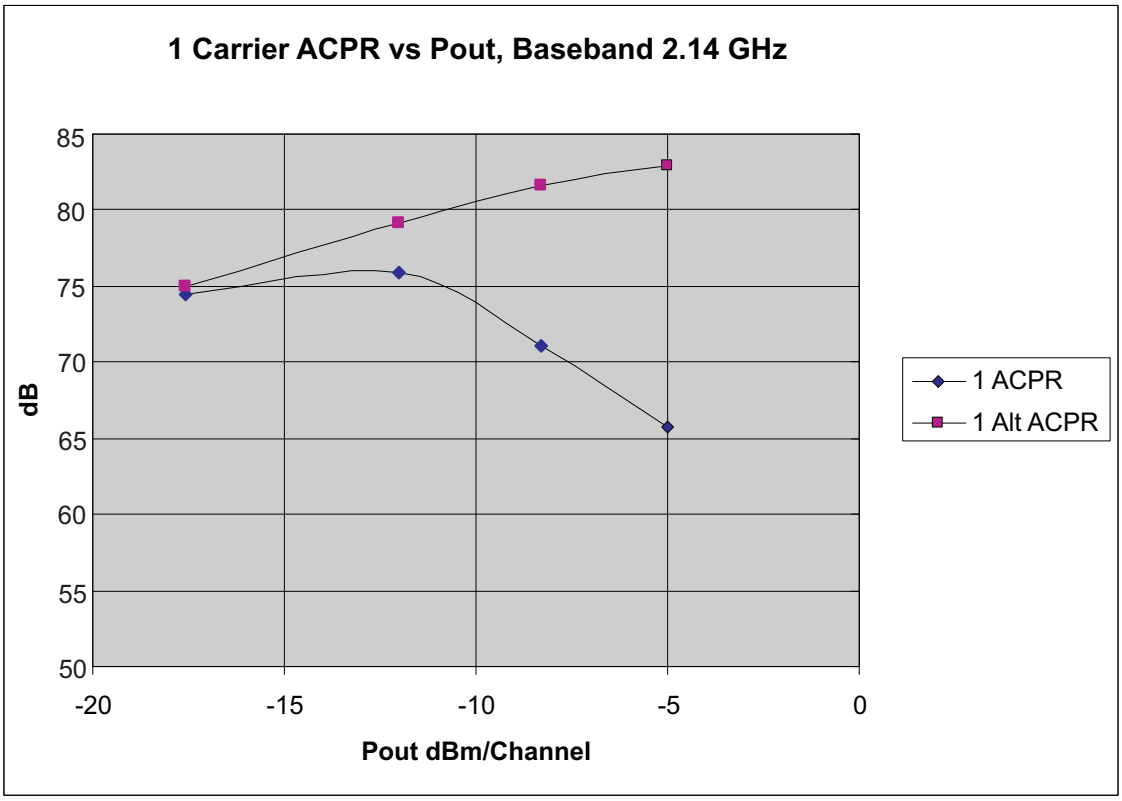


Figure 12. ACPR Versus Output Power for 1Carrier WCDMA

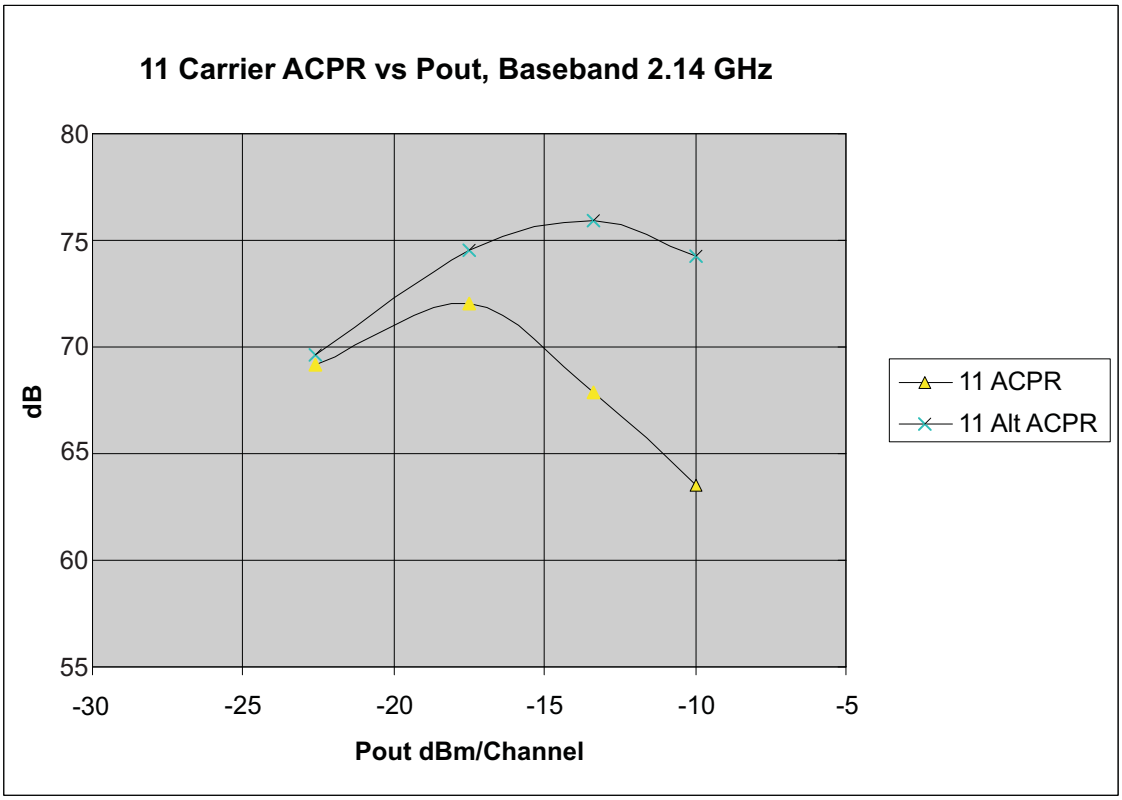


Figure 13. ACPR Versus Output Power for 2 Carriers WCDMA

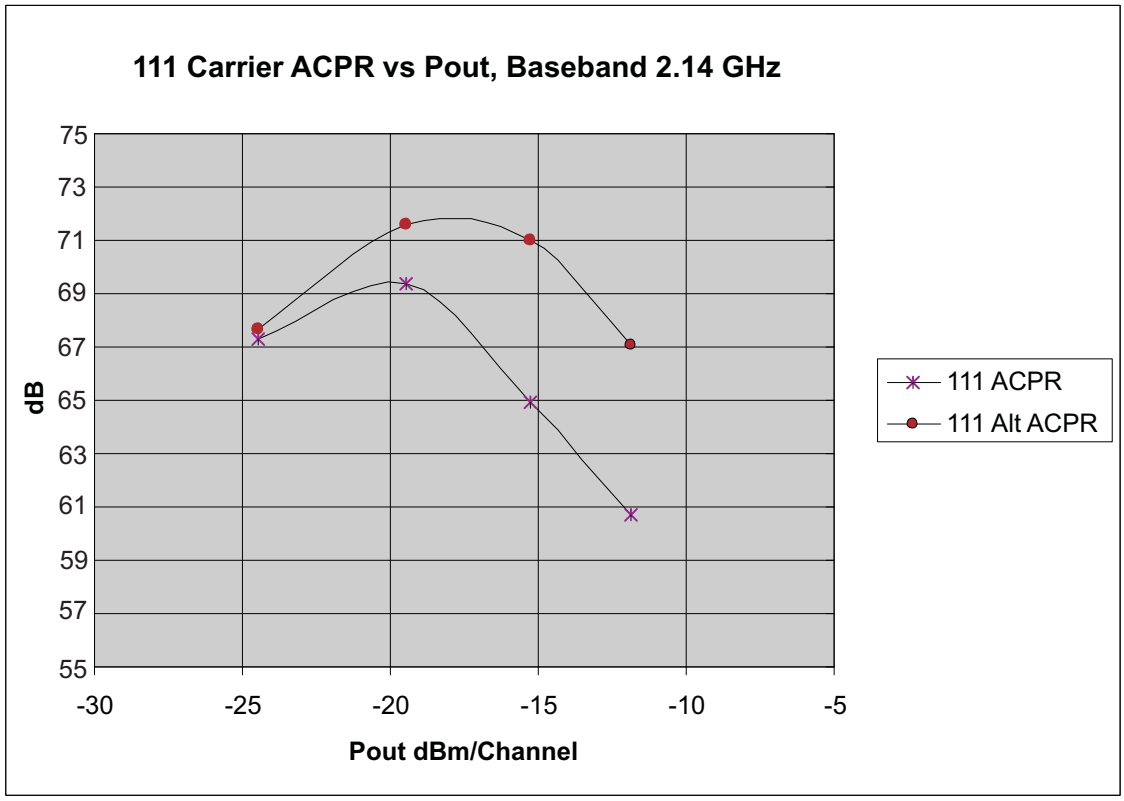


Figure 14. ACPR Versus Output Power for 3 Carriers WCDMA

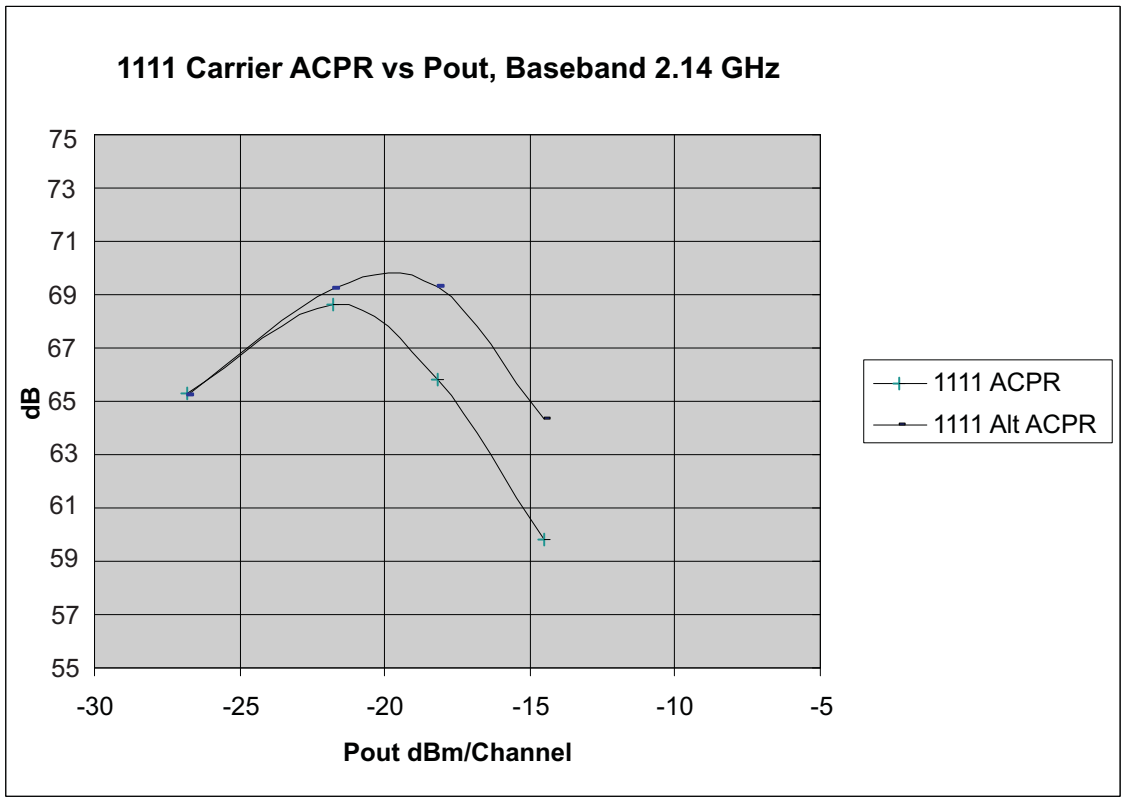


Figure 15. ACPR Versus Output Power for 4 Carriers WCDMA

Typical ACPR results are shown in Figure 16 through Figure 19 for the four cases.

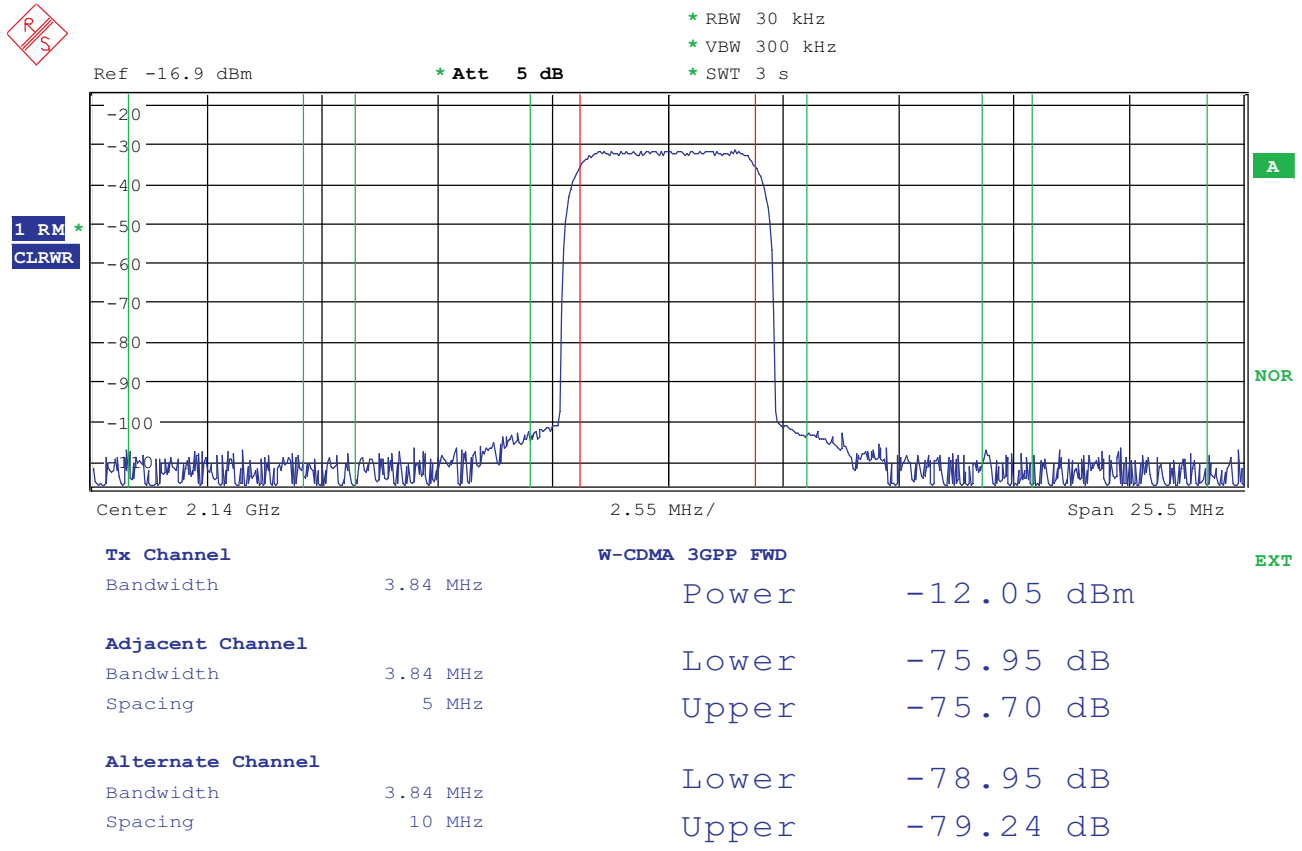


Figure 16. Optimum ACPR for 1 Carrier WCDMA, -7-dB Pad

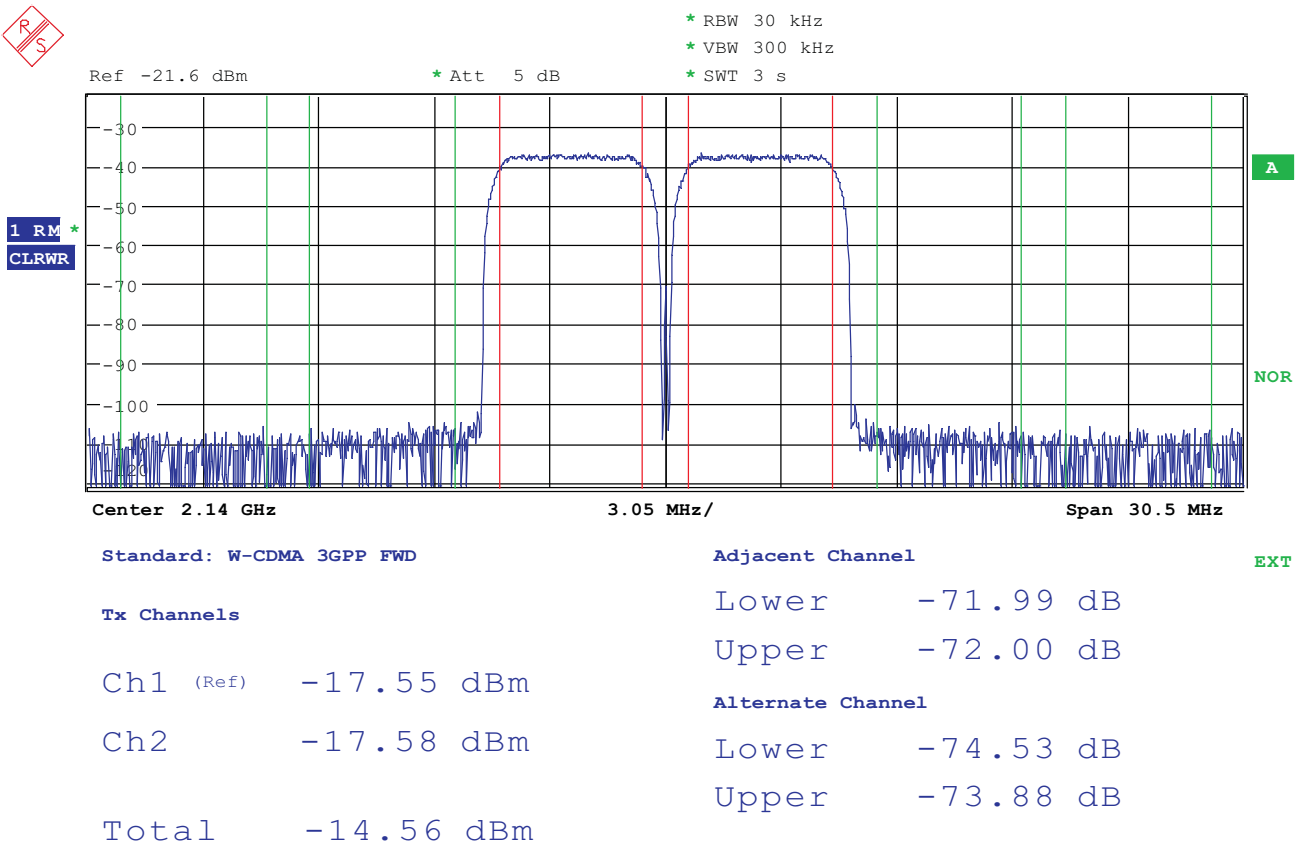


Figure 17. Optimum ACPR for 2 Carrier WCDMA, -7-dB Pad

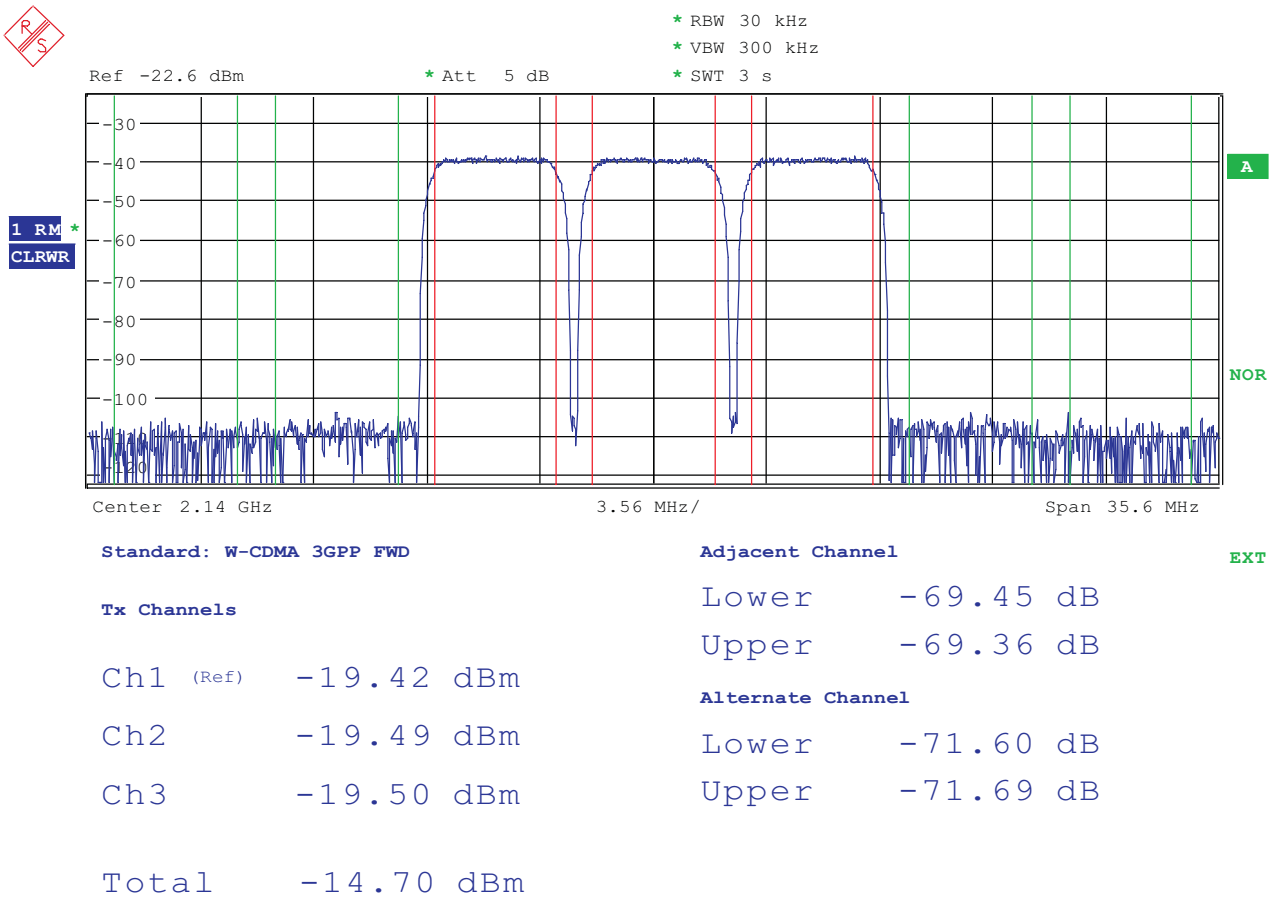


Figure 18. Optimum ACPR for 3 Carrier WCDMA, -7-dB Pad

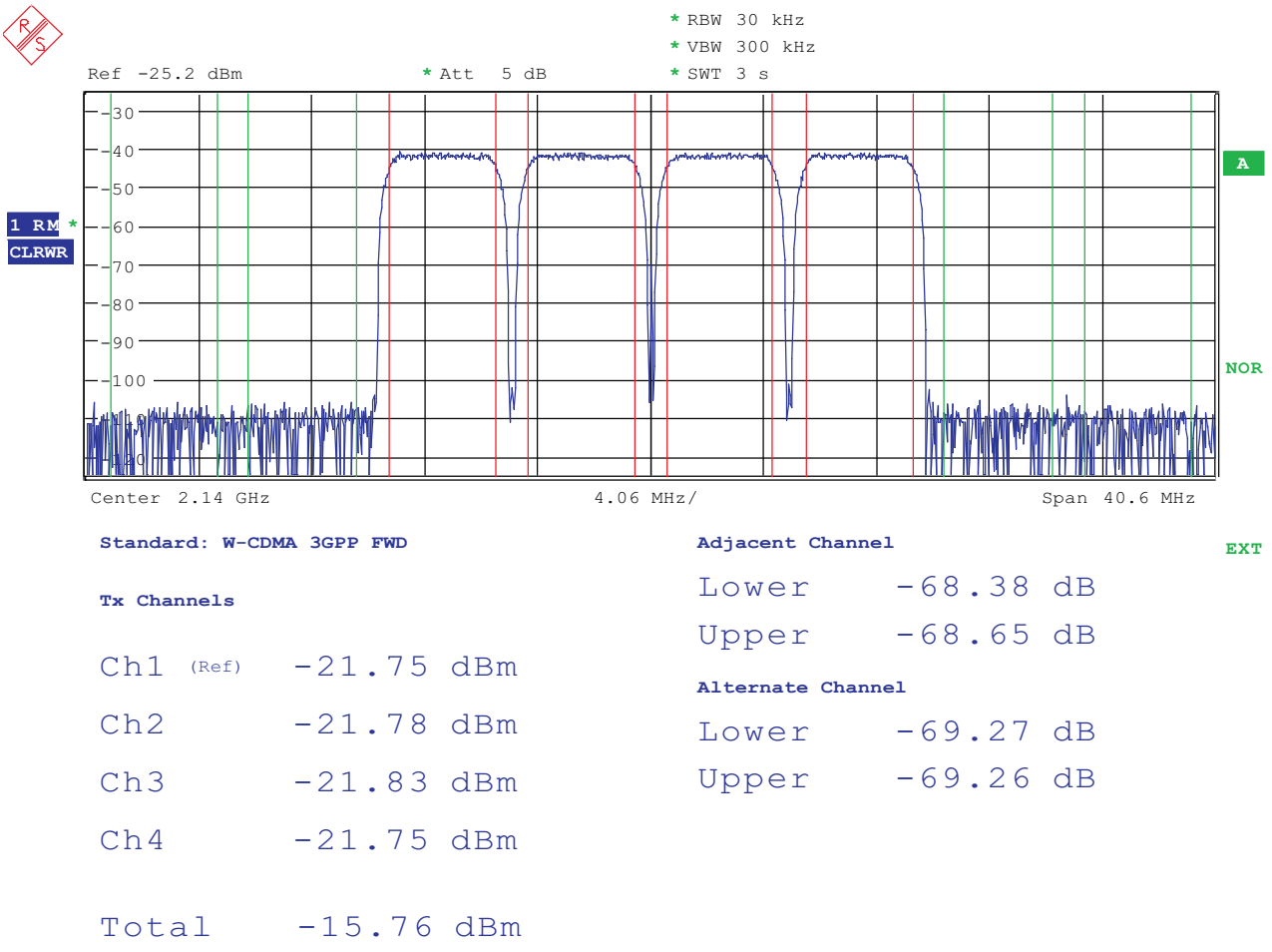


Figure 19. Optimum ACPR for 4 Carrier WCDMA, -7-dB Pad

8 Basic Test Procedure

This section outlines the basic test procedure to get the Demo Kit operational. Disconnect the cables at J29 and J30 that connect to the pattern generator. Connect the power supply cable and the RF output to the spectrum analyzer.

8.1 Initial Inspection

Inspect the board to determine which devices were used.

- Note the VCXO frequency (U1) that is on the board

8.2 Engage Power Supplies

Engage 6-V power supply

- Verify the current reading is between 0.8 A to 1.3 A when configured with the DAC5687, if applicable. When using the wall adapter, this may be difficult. In this case, just note that the D12 and D13 are on.

8.3 Program the CDCM7005

Use the Default Settings on the CDCM7005 GUI (See Section 5.1). This generates a 491.52-MHz clock.

- Hit the GUI Send button
- Verify that LEDs D12, D13, and D14 are illuminated

8.4 Program the TRF3761

Use the Default Settings in the TRF3761 GUI (See Section 5.2). This places a carrier at 2.14 GHz

- Hit the GUI send button.
- Verify the LED D15 is illuminated. This indicates that a locked LO is present.
- Monitor RF output from the spectrum analyzer
- Verify a single frequency tone at the default 2.14 GHz.

There may be side tones created by the default complex output of the DAC5687.

Table 6. Frequency Designations

VCO BAND	UMTS	GSM900	PCS	DCS1800
Midband (MHz)	2140	950	1960	1850
Low (MHz)	2110	935	1930	1805
High (MHz)	2170	960	1990	1880

8.5 DAC5687 Program

- The DAC PLL mode is disabled as per the default jumper settings on J31. See section 6.
- Verify DACA and DACB Coarse Gain is set to 15
- Ensure DAC Offsets and DAC fine gain for both A and B are set to 0
- Set the spectrum analyzer as follows:
  - Center Freq: 2.14 GHz
  - RBW: 30 kHz, VBW: 300 kHz
  - Span: 491.52 MHz
  - Attn: 5 dB
  - Ref Level: 10 dBm

8.6 Carrier Suppression

The carrier suppression can be tuned for better performance by adjusting the dc-offset controls on the DAC5687. The default DAC GUI is shown below with the NCO mixer turned on to output a 61.44-MHz tone. The output spectrum is illustrated in Figure 21.

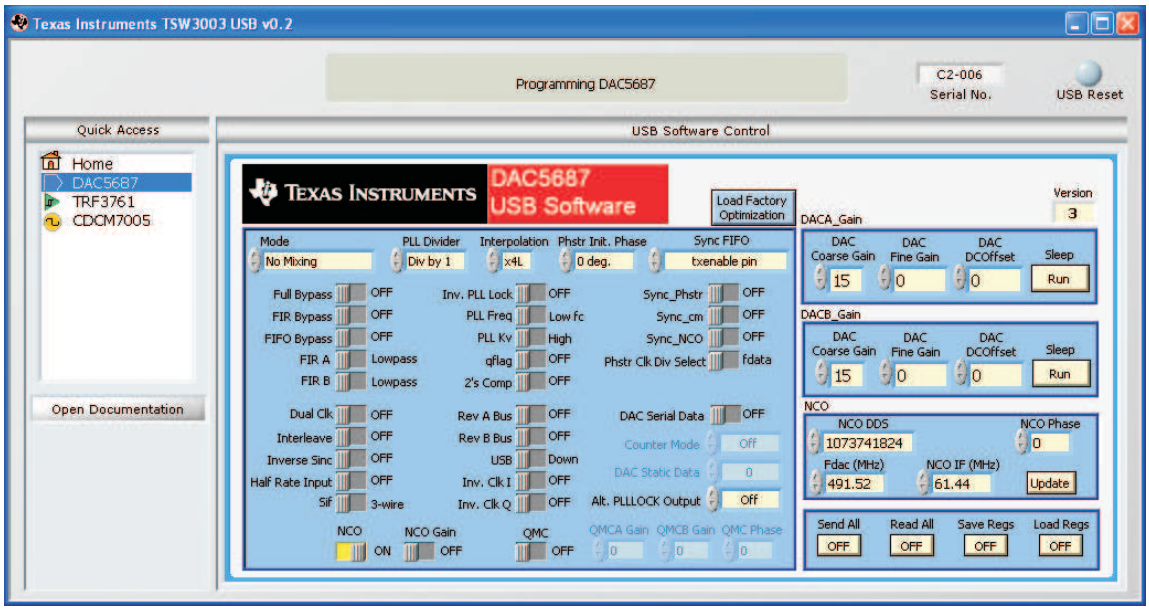


Figure 20. Default DAC GUI With $f_{DAC}/8$ Tone From NCO

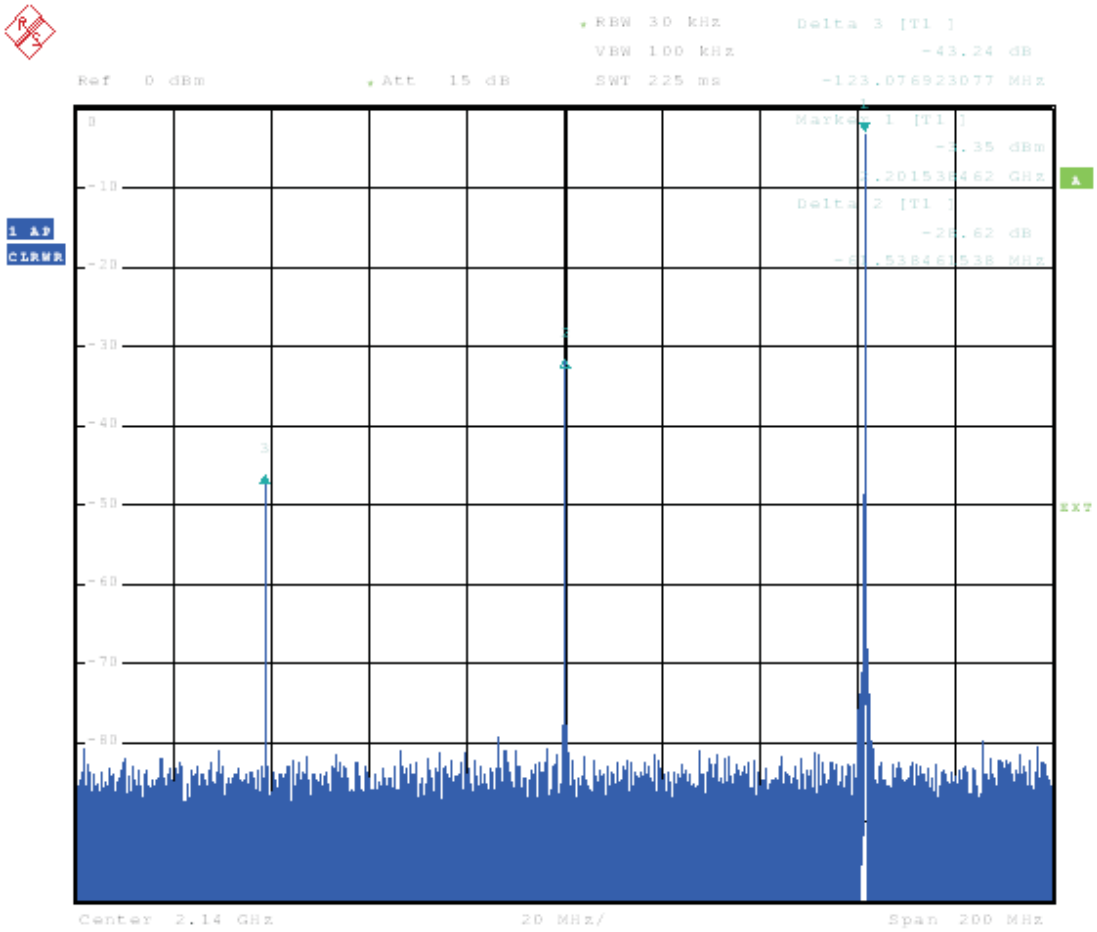


Figure 21. Single Sideband Spectrum Output Before DAC Offset and QMC Adjustments

An iterative process is used to achieve the best performance.

- Place a normal marker at the peak upper sideband, place a delta marker at the carrier signal, and note the initial delta value.
- Set initial DACA offset to 0 and DACB offset to 0.
- Change DACA offset by 1000 steps and monitor the output performance change.
- If performance gets better, then repeat the process with an additional 1000 steps. If the performance gets worse or doesn't change, then change the offset in the other direction by 1000 steps.
- Once the best performance remains basically unchanged, repeat the process on DACB offset with 1000 step changes.
- Once optimized, go back to the A side and repeat the tuning process with a step size of 100.
- Continue tuning. After each complete cycle, reduce the step size down (i.e., to 10, then to 1 if desired).
- A performance greater that 70 dBc should be achievable.

8.7 Sideband Rejection

Sideband rejection is determined by the two quadrature signals to the modulator being exactly 180 degrees out of phase and exactly the same amplitude. Amplitude and phase imbalance between the two paths yield an unwanted lower sideband. The amplitude variation between the two paths can be compensated for by adjusting the DAC fine gain controls or by adjusting the QMC gain controls if the device is operating with the QMC on. The phase can be compensated by using the QMC phase adjustment. Note this is only possible when the coarse mixer is not used in the $f_{DAC}/4$ mode. Coarse mixing in the $f_{DAC}/4$ mode causes the relative phase information between I and Q paths to be mixed. In the $f_{DAC}/2$ mode there are no cross terms (terms are 0) and the relative phase information is maintained between I and Q paths.

- Place marker delta on the lower sideband
- Turn on the QMC. Set the Gain of the QMC to 1024 for gain of 0 dB for I and Q paths. Other initial settings may be needed depending on the state of the NCO gain and signal amplitude.
- Change the phase of the QMC by small increments until the sideband is minimized.
- Change the QMC A or B gains in increments of 1 until the sideband is minimized.
- The overall performance should be greater than 60 dBc from the other sideband with amplitude and phase corrections.
- Re-optimized the dc-offset values as required to maintain carrier suppression performance as specified.

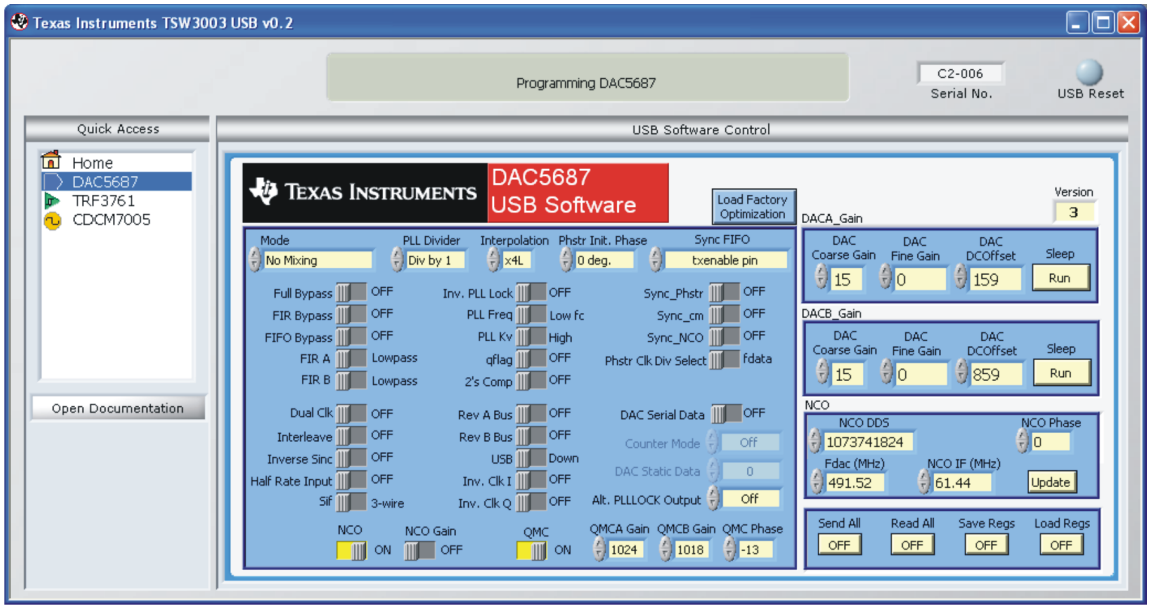


Figure 22. DAC GUI With Typical Settings To Minimize LO and Sideband

Sideband and LO are reduced significantly. Other spurs can be easily filtered out using an RF filter.

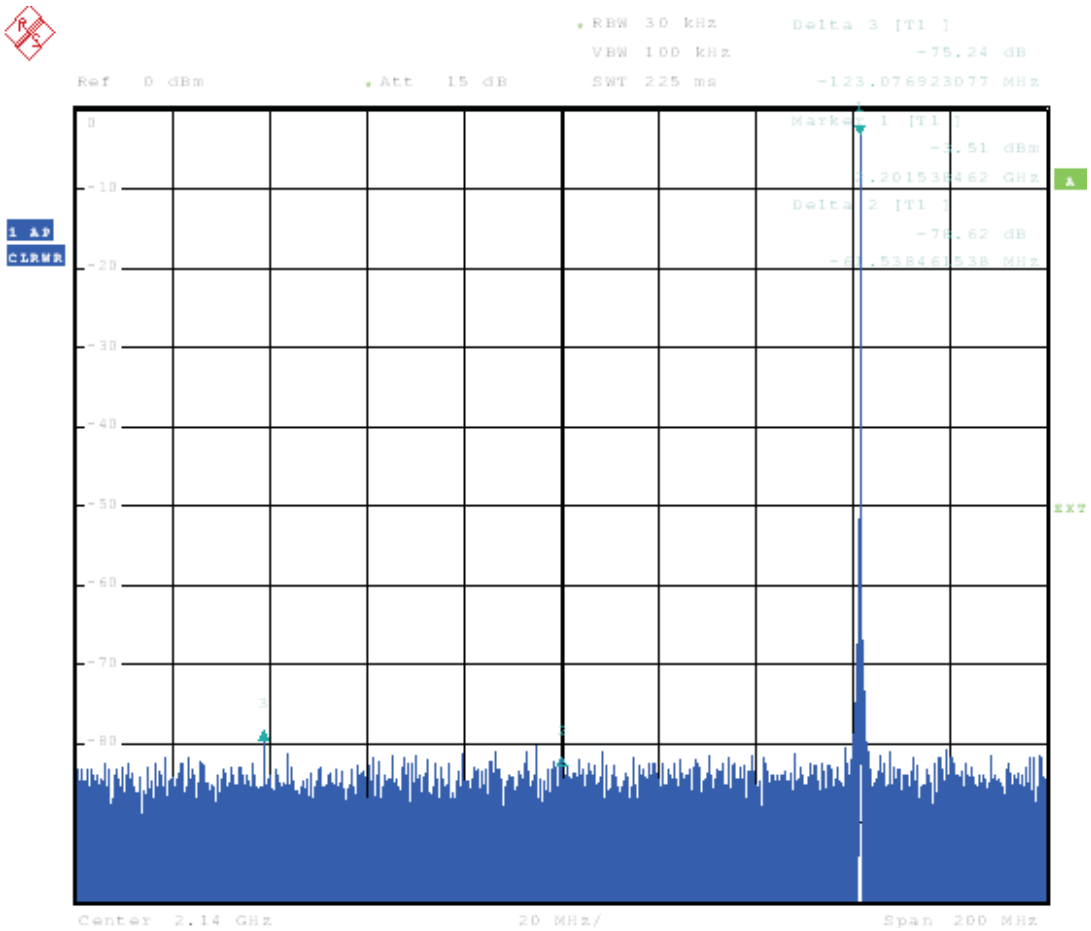


Figure 23. Sideband and LO Compensated Using QMC Settings

9 Optional Configurations

9.1 External LO

To configure the board for external LO implement the following modifications:

- Remove C154, C155; disconnect the TRF3761 from LO path
- Install C390, C391, R114 to connect the external LO to modulator, external LO J39
- Disable the TRF3761 output by setting J31-23, 24 PD_OUTBUF, J31-25, 26 CHIP_EN

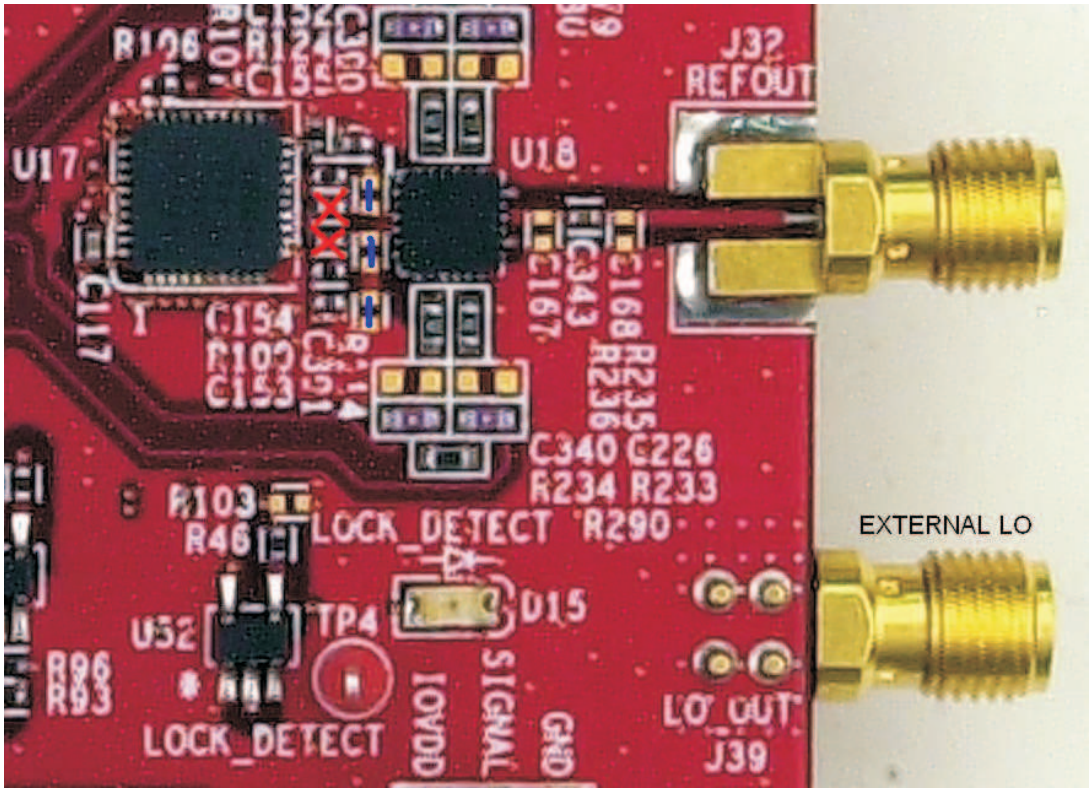


Figure 24. Board Modifications for External LO

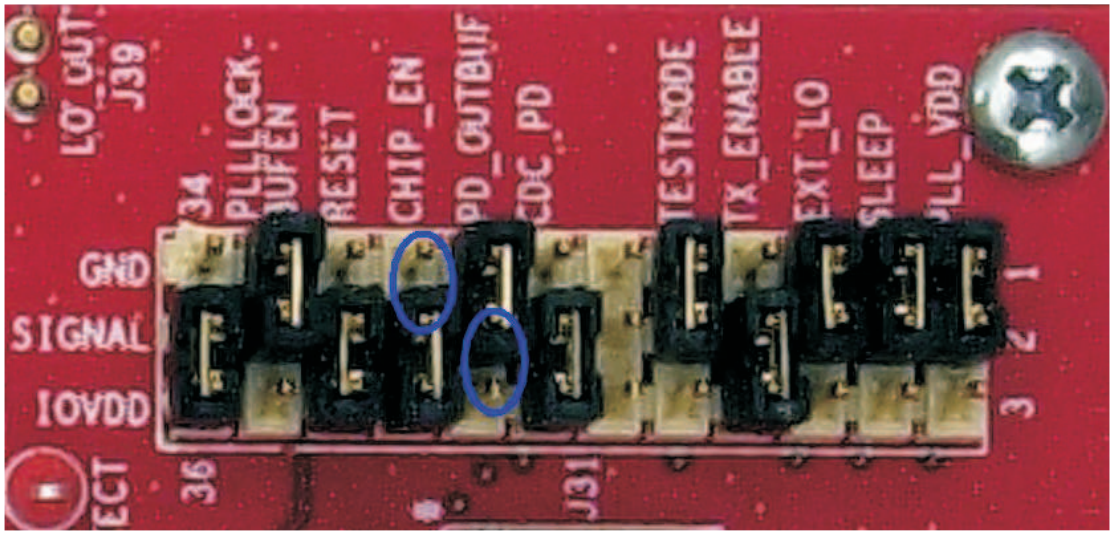


Figure 25. Jumper Settings to Disable TRF3761

9.2 External Reference

To configure the board for external reference, implement the following modifications:

- Change JP1-2,3 and JP2-2,3. Connect external VXCO to J4.

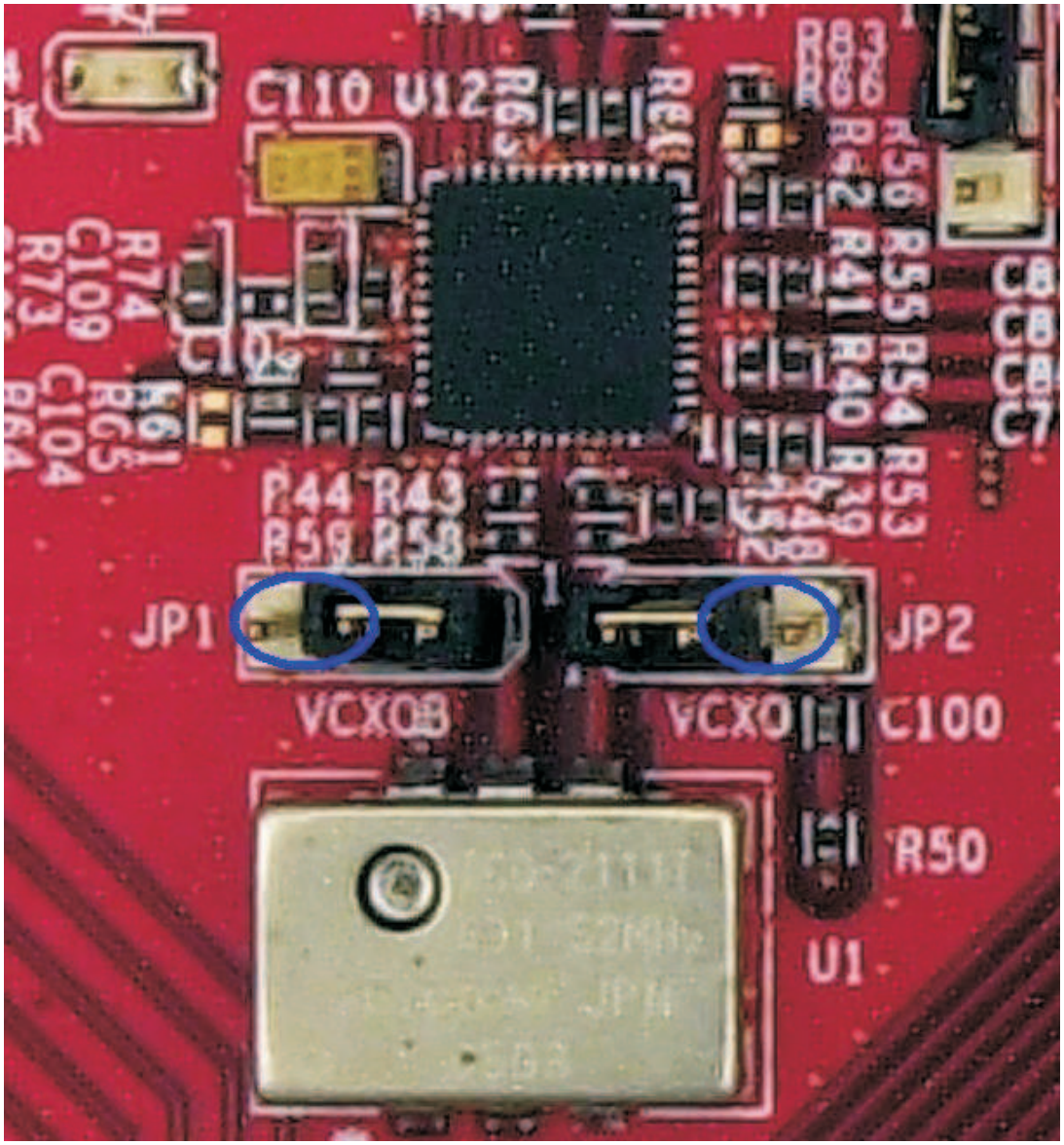


Figure 26. Jumper Changes for External VCXO

10 Filter Specifications

10.1 Baseband Filter

The TSW3003 Demo Kit layout provides the opportunity to place components to realize up to a 5th order LC filter. The Demo Kit is by default populated with a resistive network to provide some attenuation and a two-inductor network to compensate for the droop caused by the parasitic board capacitance. This provides about 0.5 dB of ripple up to ±200 MHz of bandwidth, followed by a slow, low-pass rolloff.

10.1.1 RF Filter/Output Match

The TSW3003 Demo Kit layout also provides the opportunity to place a small 3rd order LC filter on the output of the modulator for either filtering or impedance matching purposes. This filter has been disabled by removing the shunt elements.

11 Bill of Materials and Schematics

This section contains the bill of materials and schematics for the TSW3003 Demo Kit.

11.1 Bill of Materials

Table 7 lists the parts used in constructing the TSW3003 Demo Kit.

Table 7. Bill of Materials

Qty	Ref Des	Value	PCB Footprint	MFR Name	MFR Part Number	Note
8	C1 C18 C21 C26 C34 C39 C41 C46	47µF	tant_b	Kemet	T494B476M010AS	
62	C3 C20 C28 C36 C38 C43 C48-C54 C56-C66 C70-C72 C74 C75 C78 C85-C94 C97-C100 C103 C106 C111 C112 C115 C118 C120 C121 C123 C124 C144 C145 C162 C165 C344-C347	0.1µF	0402	Panasonic	ECJ-0EB1C104K	
2	C4 C109	1µF	0603	Panasonic	ECJ-1V41E105M	
6	C5 C77 C80-C82 C96	0.01µF	0402	Panasonic	ECJ-0EB1E103K	
12	C19 C24 C25 C27 C35 C37 C40 C42 C44 C45 C47 C348	10µF	1206	Panasonic	ECJ-3YB1C106K	
13	C55 C67-C69 C76 C79 C83 C84 C101 C116 C122 C148 C150	10µF	tant_a	Kermet	T494A106M016AS	
6	C95 C104 C117 C127 C163 C164	0.001µF	0402	Panasonic	ECJ-0EB1E102K	
1	C102	560pF	0402	Panasonic	ECJ-0EB1H561K	
1	C108	0.47µF	0603	Murata	GRM188R71C474KA88D	
1	C110	22µF	tant_a	Kemet	T494A226M010AS	
2	C119 C343	100pF	0402	Panasonic	ECJ.-0EB1E101K	
1	C126	680pF	0603	Murata	GRM1885C2A681JA01D	
1	C128	330pF	0603	Murata	GRM1885C2A331JA01D	
1	C136	0.033µF	0402	AVX	0402ZC333KAT2A	
1	C137	330pF	0402	Panasonic	ECJ-0EB1E331K	
1	C138	10,000pF	0603	Murata	GRM188R71H103KA01D	
7	C147 C149 C151 C154 C155 C377 C387	10pF	0402	Murata	GRM1555C1H100JZ01D	
2	C152 C153	22pF	0402	Panasonic	ECJ-0EC1H220J	
0	C156-C158 C171	2.2pF	0603	AVX	06035A2R2CAT2A_DNI	DNI
3	C160 C161 C169	4.7µF	tant_a	AVX	TAJA475K020R	
0	C167 C168	DNI	0402	Panasonic	ECJ-0EB1E103K_DNI	DNI
0	C224-C226 C340	4.7pF	0603	Panasonic	ECJ-1VC1H047C_DNI	DNI
2	C381 C386	3.3pF	0402	Murata	GRM1555C1H3R3CZ01D	
2	C383 C384	47pF	0603	Panasonic	ECJ-1VC1H470J	
1	C385	10nF	0603	Panasonic	ECJ-1VB1C103K	
0	C390 C391	22pF	0402	Panasonic	ECJ-0EC1H220J_DNI	DNI
5	D12-D16	LED green	LED_0805	Panasonic	LNJ306G5UUX	
16	FB1-FB16	68Ω at 100MHz	1206	Panasonic	EXC-ML32A680U	
1	J1	CONN JACK PWR	CON_RAPC722_JACK_THVT_3	Switchcraft	RAPC722	

Table 7. Bill of Materials (continued)

Qty	Ref Des	Value	PCB Footprint	MFR Name	MFR Part Number	Note
8	J4 J7-J9 J27 J32 J35 J39	SMA_END_RND	SMA_SMEL_218x247	Johnson Components	142-0761-821	
2	J29 J30	TSM-117-01-S-DV-LC	SAMTEC_TSM_117_01_S_DV_LC	SAMTEC	TSM-117-01-S-DV-LC	
1	J31	HTSW-120-07-L-T	HDR_THVT_3x12_100_M	SAMTEC	HMTSW-120-07-G-T	
1	J34	USB_B_S_F_B_TH	CON_THRT_USB_B_F	SAMTEC	USB-B-S-F-B-TH	
1	J37	BANANA_JACK_RED	JACK_THVT_BANANA_250dia	Alectron Connectors	ST-351A RED	
1	J38	BANANA_JACK_BLK	JACK_THVT_BANANA_250dia	Alectron Connectors	ST-351B BLK	
4	JP1 JP2 JP6 JP8	Jumper_1x3_100_430L	HDR_THVT_1x3_100_M	SAMTEC	HMTSW-103-07-G-S-.230	
10	L19 L21 L22 L25 R179 R230 R235-R237 R262	0	0603	Panasonic	ERJ-3GEY0R00V	
4	L20 L23 L24 L26	33nH	0603	Coilcraft	0603CS-33NX_L	
2	L27 L28	8.2nH	0402	Coilcraft or Johanson	0402CS-3N3XJL or L-07C3N3SV6S	
3	R13 R18 R21	100K	0603	Panasonic	ERJ-3EKF1003V	
3	R23 R24 R105	1K	0402	Panasonic	ERJ-2RKF1001X	
0	R25 R37 R97 R98	130	0402	Panasonic	ERJ-2RKF1300X_DNI	DNI
14	R26 R31 R45 R46 R67 R68 R71 R72 R75 R76 R90 R91 R101 R108	22.1	0402	Panasonic	ERJ-2RKF22R1X	
1	R27	15.8K	0603	Panasonic	ERJ-3EKF1582V	
1	R28	30.1K	0603	Panasonic	ERJ-6ENF3012V	
1	R29	10	0402	Panasonic	ERJ-2RKF10R0X	
11	R32 R33 R82 R86 R88 R89 R92 R93 R96 R99 R125	100	0402	Panasonic	ERJ-2RKF1000X	
3	R34-R36	750	0402	Panasonic	ERJ-2RKF7500X	
8	R39-R44 R47 R49	130	0402	Panasonic	ERJ-2RKF1300X	
3	R48 R52 R83	150	0402	Panasonic	ERJ-2RKF1500X	
3	R50 R63 R69	0	0402	Panasonic	ERJ-2GE0R00X	
8	R53-R56 R58 R59 R70 R78	82.5	0402	Panasonic	ERJ-2RKF82R5X	
8	R61 R65 R77 R79 R81 R84 R94 R95	10K	0402	Panasonic	ERJ-2RKF1002X	
0	R64	1K	0402	Panasonic	ERJ-2RKF1001X_DNI	DNI
0	R66	22.1	0402	Panasonic	ERJ-2GE0R00X_DNI	DNI
1	R73	162	0402	Panasonic	ERJ-2RKF1620X	
3	R74 R106 R107	4.75K	0402	Panasonic	ERJ-2RKF4751X	
2	R102 R109	300	0603	Panasonic	ERJ-3EKF3000V	
0	R103	100	0402	Panasonic	ERJ-2RKF1000X_DNI	DNI
1	R104	7.5k	0603	ROHM	MCR03EZPFX7501	
1	R110	649	0603	Yageo	RC0603FR-07649RL	
0	R114	49.9	0402	Panasonic	ERJ-2RKF49R9X_DNI	DNI
4	R118 R119 R133 R134	634	0603	Yageo	RC0603FR-07634RL	
4	R120 R171 R180 R184	60.4	0603	Yageo	RC0603FR-0760R4L	
4	R172 R177 R280 R281	115	0603	Yageo	RC0603FR-07115RL	
1	R261	93.1	0402	Panasonic	ERJ-2RKF93R1X	
0	R284	110	0603	Panasonic	ERJ-3EKF1100V_DNI	DNI
0	R285	221	0603	Panasonic	ERJ-3EKF2210V_DNI	DNI
1	R287	23.2K	0603	Panasonic	ERJ-3EKF2322V	
1	R288	6.34K	0603	Panasonic	ERJ-3EKF6341V	

Table 7. Bill of Materials (continued)

Qty	Ref Des	Value	PCB Footprint	MFR Name	MFR Part Number	Note
2	R289 R290	90.9	0603	Panasonic	ERJ-3EKF90R9V	
4	RN1-RN4	4816P-001-220	RNET_16_225x445_50	Bourns	4816P-001-220	
1	SJP3	Jumper_1x3_SMT	SJP3_JUMPER			
1	SW2	SW RESET	switch_reset	C&K	KT11P3JM	
2	TP1 TP4	Testloop_Red	TP_THVT_060_RND	Keystone Electronics Corp	5000	
1	U1	2115-491.52MHZ	VCXO_6	Toyocom	TCO-2111-491.52	
1	U6	TPS76733QPWP	HTSSOP_20_260x177_26_pwrpad	Texas Instruments	TPS76733QPWP	
1	U8	TPS76701QPWP	HTSSOP_20_260x177_26_pwrpad	Texas Instruments	TPS76701QPWP	
1	U9	TPS76701QPWP	HTSSOP_20_260x177_26_pwrpad	Texas Instruments	TPS76750QPWP	
1	U10	DAC5687	HTQFP100	Texas Instruments	DAC5687	
1	U12	CDCM7005	QFN48	Texas Instruments	CDCM7005RGZT	
1	U16	OSC-VECTRON	OSC_4_SM_460x386	VECTRON	VTD3-J0BC-10M000	
1	U17	TRF3761	PQFP_40_242x242_0p5mm	Texas Instruments	TRF3761	
1	U18	TRF3703-33	QFN24	Texas Instruments	TRF3703	
1	U47	SN74AHC541PW	tssop_20_260x177_26	Texas Instruments	SN74AHC541PW	
1	U48	SN74HC241PW	tssop_20_260x177_26	Texas Instruments	SN74HC241PW	
3	U49 U51 U52	SN74LVC1G125DBVR	SOT_5_120x69_57	Texas Instruments	SN74LVC1G125DBVR	
1	U50	FT245RL	ssop_28_413x220_26	FTDI Chip	FT245RL	
0	U53	OSC-VECTRON	XTAL_4_SM_203x132	Vectron International	VTC4_DNI	DNI
4	SCREW1-SCREW4		SCREW PANHEAD 4-40 x 3/8	Building Fasteners	PMS 440 0038 PH	
4	STANDOFF1-STANDOFF4	STANDOFF ALUM HEX 4-40 × 0.500		Keystone	2203	

11.2 Schematics

The schematic for the TSW3003 Demo Kit appears on the following page.

NOTE: DNI = DO NOT INSTALL

JP8 - JUMPER PINS 1 & 2

R23 1K
C56 .1uF
C49 .1uF
+1.8VD
+3.3VA
R24 1K
SW2 RESET
SW RESET
SH2 EXT_LO
IOUTA1 SH3
IOUTA2 SH3
IOUTB2 SH3
IOUTB1 SH3

U10
DAC5687

AGND AVDD AVDD AGND IOUTA1 IOUTA2 AGND AVDD AGND AVDD EXTLO AVDD BIASJ AGND EXTIO AVDD AGND AGND AGND IOUTB2 IOUTB1 AGND AVDD AVDD AGND
25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1

DVDD DGND SDENB SCLK SDIO SDO DVDD TXENABLE DA15(MSB) DA14 DA13 DVDD DGND DA12 DA11 DA10 DA9 DA8 DVDD DGND IOVDD IOGND DA7 DA6 DA5
26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50

DA4 DA3 DA2 DA1 DA0(LSB) DVDD DGND CLKGND CLK1 CLK1C CLKVDD CLK2 CLK2C CLKGND PLLGND LPF PLLVDD DVDD DGND PLLLOCK DB0(LSB) DB1 DB2 DB3 DB4
51 52 53 54 55 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70 71 72 73 74 75

DVDD DGND QFLAG TESTMODE SLEEP RESETB PHSTR DGND DB15(MSB) DB14 DB13 DVDD DGND DB12 DB11 DB10 DB9 DB8 DVDD DGND IODVDD IOGND DB7 DB6 DB5
100 99 98 97 96 95 94 93 92 91 90 89 88 87 86 85 84 83 82 81 80 79 78 77 76

SH5 SDENB
SH5 SCLK
SH5 SDIO
SH2 TX_ENABLE
DA15 DA14 DA13 DA12 DA11 DA10 DA9 DA8 DA7 DA6 DA5 DA4 DA3 DA2 DA1 DA0
SH2 DA[0..15]
DB15 DB14 DB13 DB12 DB11 DB10 DB9 DB8 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0
DB[0..15] SH2

R37 130 DNI
R25 130 DNI
R97 130 DNI
R98 130 DNI
R237 0
QFLAG SH2
SLEEP SH2
/RESET SH2,4
PHSTR SH2

IOVDD
C68 10uF 10V
C69 10uF 10V
C71 .1uF
C70 .1uF
JP8 DEFAULT +3.3VA
+3.3VA
+1.8VD

R29 10
C75 .1uF
R26 22.1
R261 93.1
C136 .033uF
C137 330pF
C74 .1uF
C76 10uF 10V
PLL_VDD SH2
R284 110 DNI
R285 221 DNI
SH2 /PLLCK_EN
U49
OE A GND VCC Y
1 2 3 5 4
SN74LVC1G125DBVR
C115 .1uF
C116 10uF 10V
R31 22.1
AMS DNF
J27 PLL_LOCK

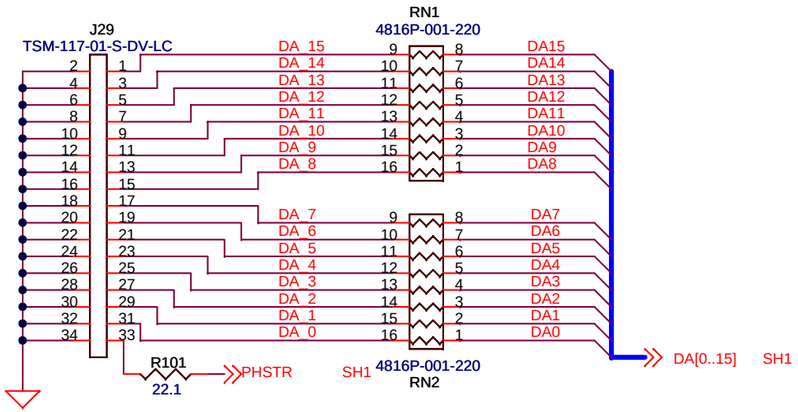
+3.3VA
C50 .1uF
C51 .1uF
C52 .1uF
C53 .1uF
C54 .1uF
C57 .1uF
C58 .1uF
C59 .1uF
C60 .1uF
C55 10uF 10V

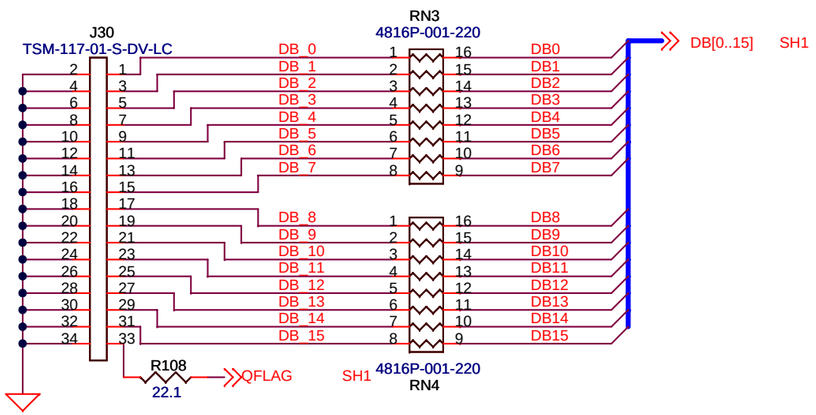
+3.3VCLK
C78 .1uF
C79 10uF 10V
R32 100
R33 100
C77 .01uF
C80 .01uF
C81 .01uF
C82 .01uF
CLK2CB SH4
CLK2B SH4
CLK1CB SH4
CLK1B SH4

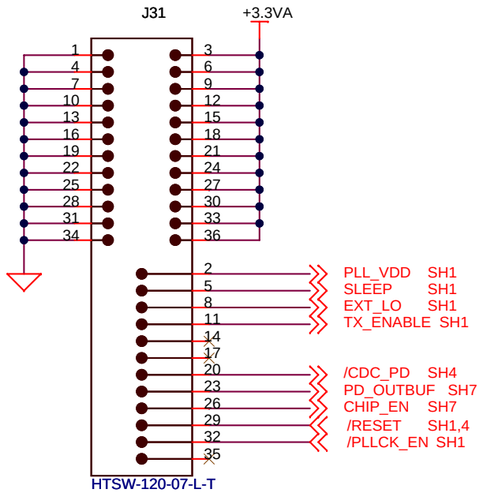
+1.8VD
C61 .1uF
C62 .1uF
C63 .1uF
C64 .1uF
C65 .1uF
C66 .1uF
C72 .1uF
C67 10uF 10V

TEXAS INSTRUMENTS

Title	TSW3003_EVM	
Size B	Document Number DAC	Rev D
Date: Wednesday, March 07, 2007	Sheet 1 of 7	
Engineer: J. SETON		
Drawn By: P. LARSON		
FILE:		





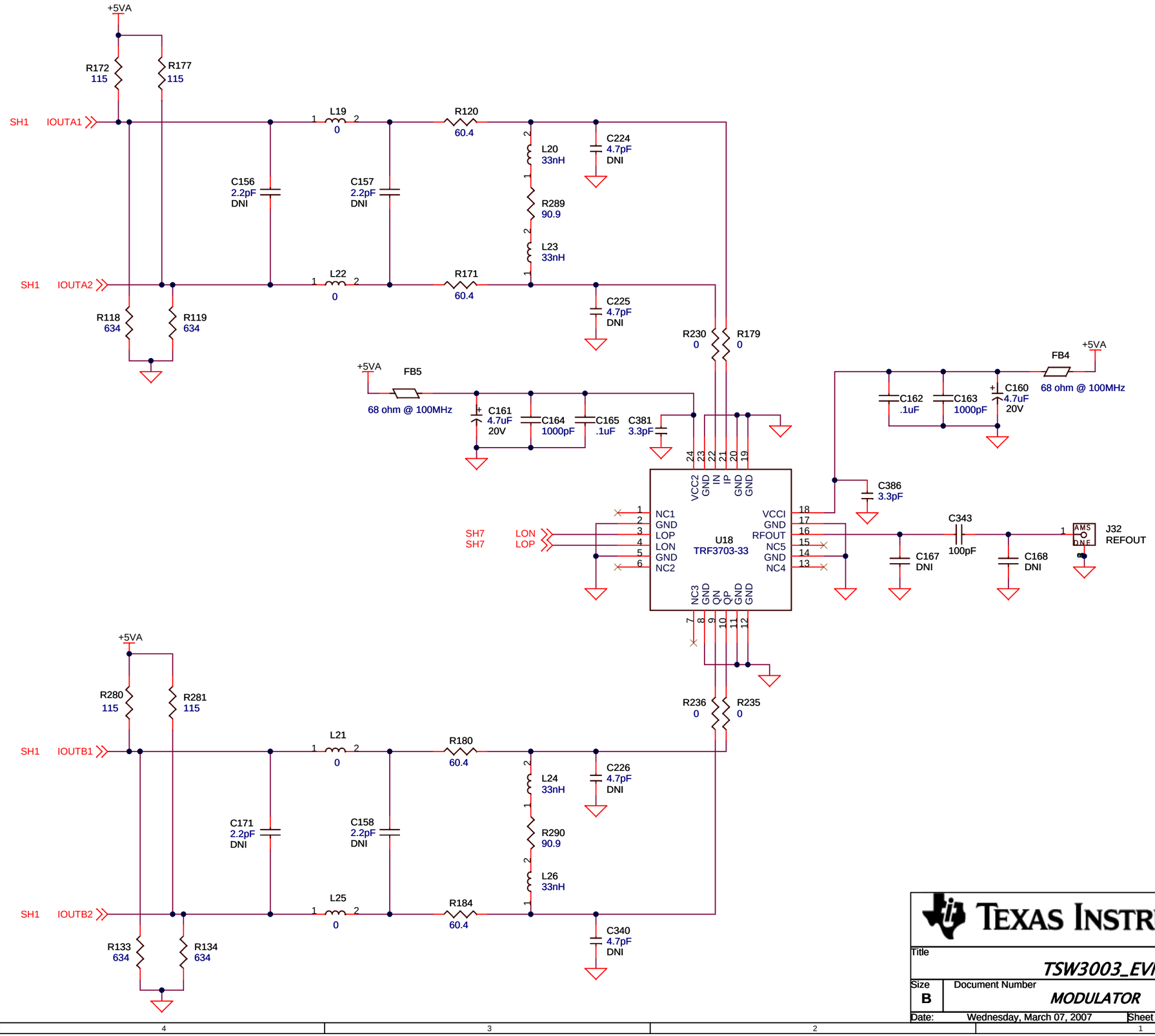


J31 - JUMPER PINS 1 & 2
JUMPER PINS 4 & 5
JUMPER PINS 7 & 8
JUMPER PINS 11 & 12
JUMPER PINS 20 & 21
JUMPER PINS 22 & 23
JUMPER PINS 26 & 27
JUMPER PINS 31 & 32

TEXAS INSTRUMENTS

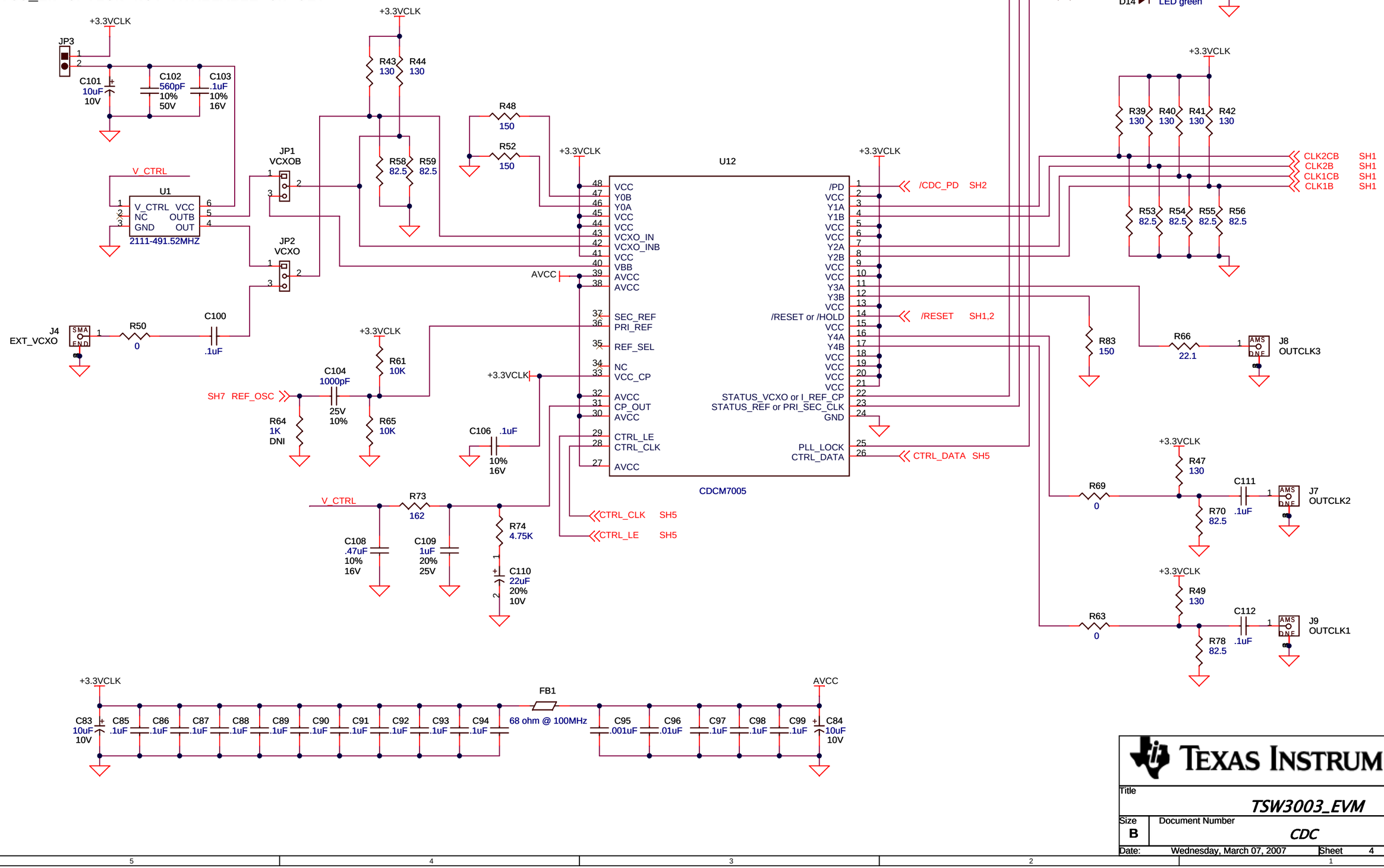
Title: *TSW3003_EVM*		
Size: B	Document Number: *INTERFACE CONTROL*	Rev: D
Date: Wednesday, March 07, 2007	Sheet 2 of 7	

NOTE: DNI = DO NOT INSTALL



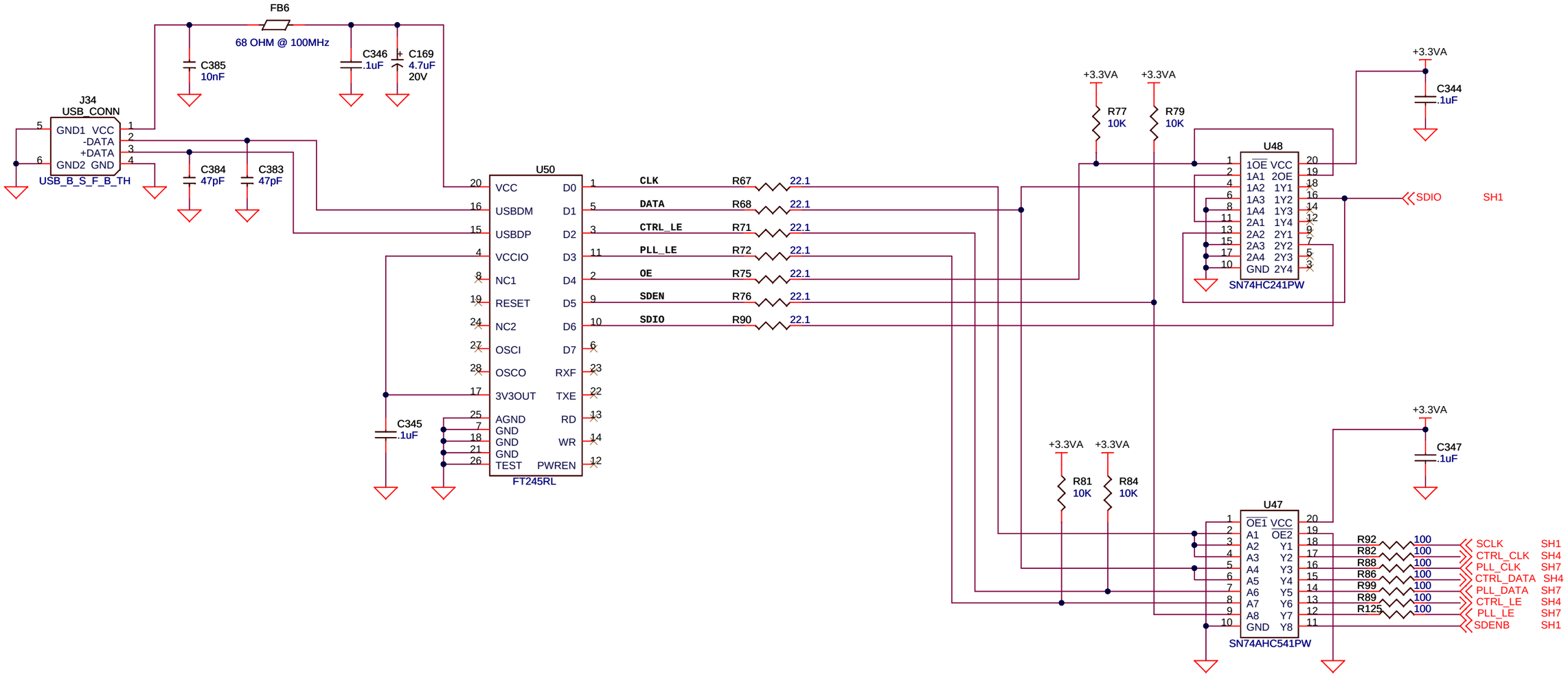
Title	TSW3003_EVM	
Size: B	Document Number: MODULATOR	Rev: D
Date: Wednesday, March 07, 2007	Sheet 3 of 7	

NOTES:
DNI = DO NOT INSTALL
JP1 - JUMPER PINS 1 & 2
JP2 - JUMPER PINS 1 & 2
VCO_EN OPTION NOT AVAILABLE ON U1.



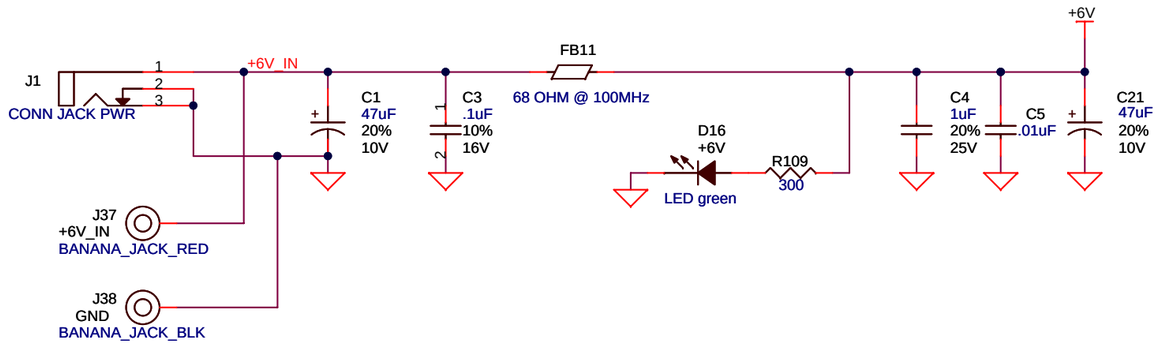
TEXAS INSTRUMENTS

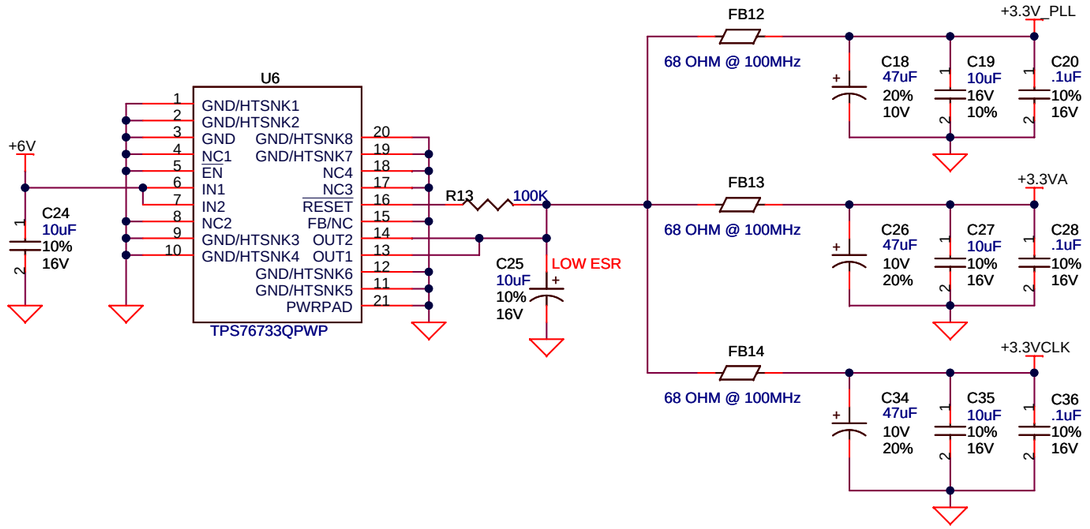
Title: *TSW3003_EVM*		
Size: B	Document Number: *CDC*	Rev: D
Date: Wednesday, March 07, 2007	Sheet 4 of 7	

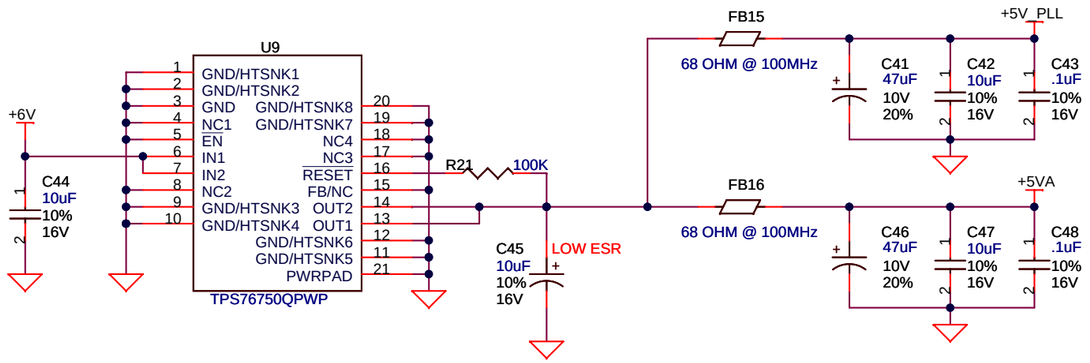


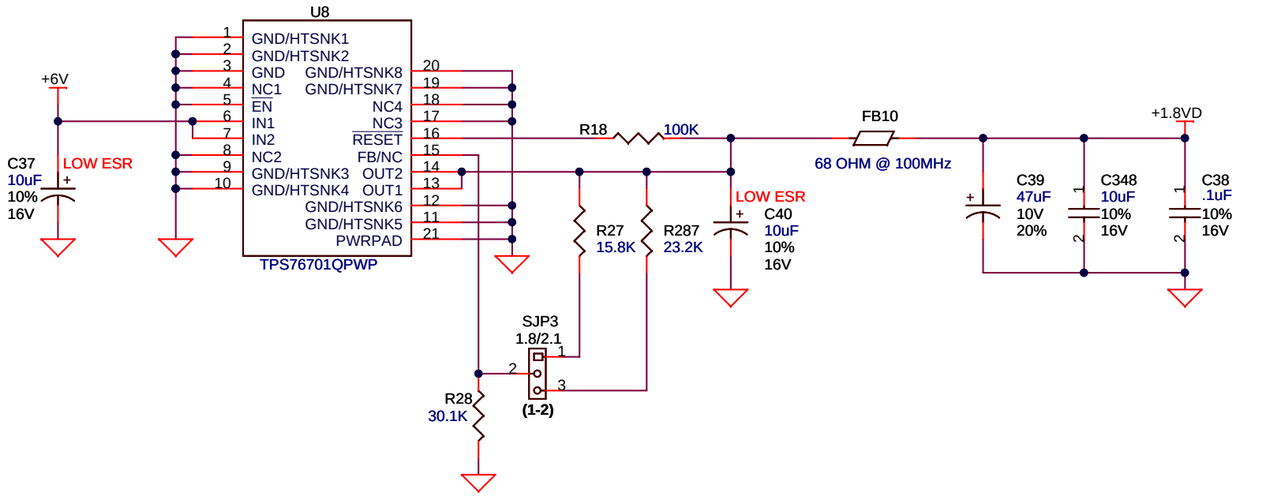
TEXAS INSTRUMENTS

Title	TSW3003_EVM	
Size: B	Document Number: USB INTERFACE	Rev: D
Date: Wednesday, March 07, 2007	Sheet 5 of 7	





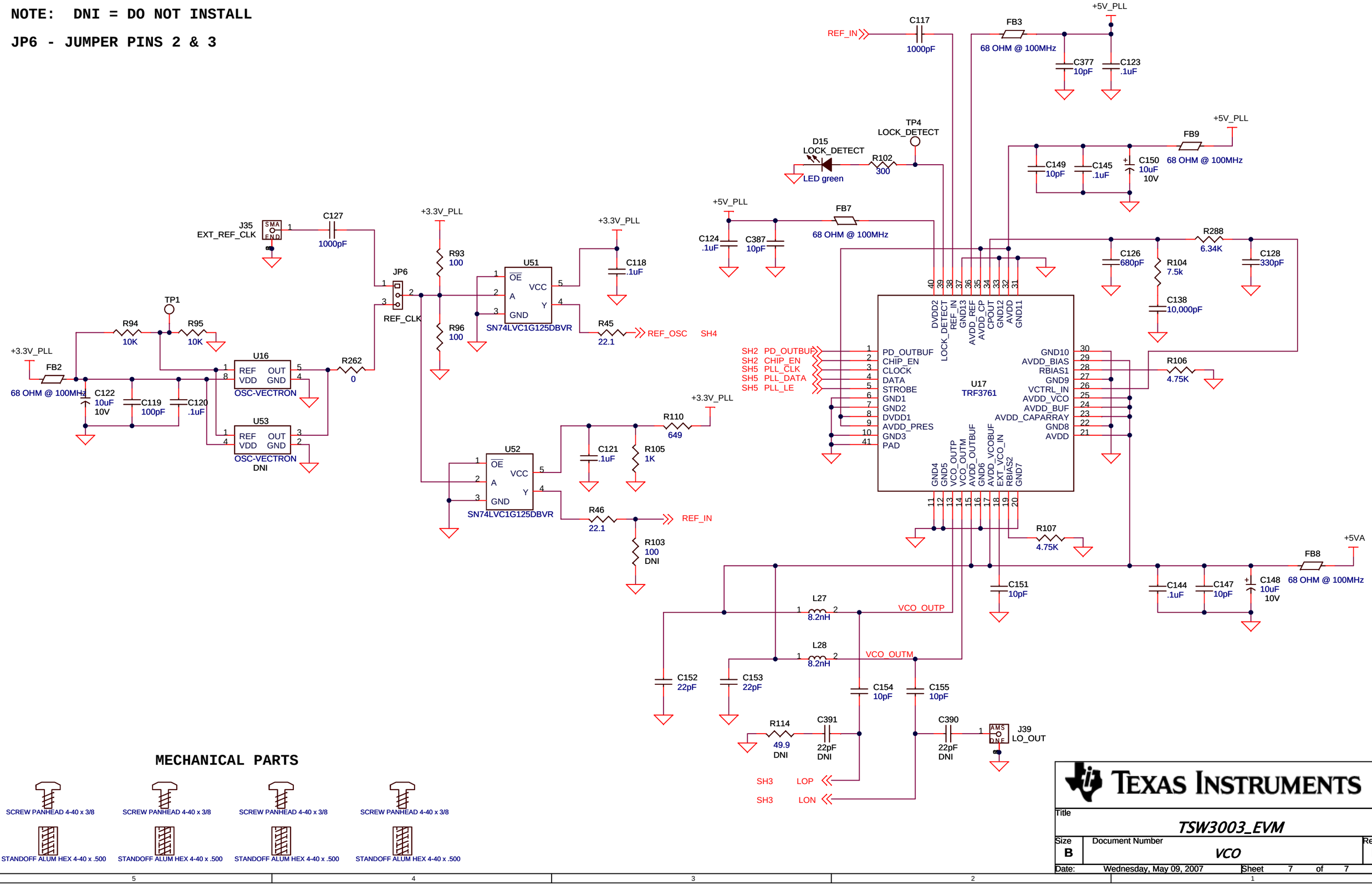




Title	TSW3003_EVM	
Size: B	Document Number: POWER DISTRIBUTION	Rev: D
Date: Wednesday, March 07, 2007	Sheet 6 of 7	

NOTE: DNI = DO NOT INSTALL

JP6 - JUMPER PINS 2 & 3



MECHANICAL PARTS

SCREW PANHEAD 4-40 x 3/8 — SCREW PANHEAD 4-40 x 3/8 — SCREW PANHEAD 4-40 x 3/8 — SCREW PANHEAD 4-40 x 3/8

STANDOFF ALUM HEX 4-40 x .500 — STANDOFF ALUM HEX 4-40 x .500 — STANDOFF ALUM HEX 4-40 x .500 — STANDOFF ALUM HEX 4-40 x .500

TEXAS INSTRUMENTS

Title	TSW3003_EVM	
Size: B	Document Number: VCO	Rev: D
Date: Wednesday, May 09, 2007	Sheet 7 of 7	

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of 5.75 V to 6.25 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 45°C. The EVM is designed to operate properly with certain components up to 85°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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