Texas Instruments

TSW3000 Demo Kit

User's Guide

November 2005

SLWU013B

TSW3000 Demo Kit

User's Guide

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Texas Instruments

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TSW3000 Demo Kit

1 Demo Kit Configuration Options

The TSW3000 Demo Kit can be configured in different ways to evaluate different components in different frequency bands. This section outlines the various component configurations. Based on the configuration, testing and board setup must be altered to accommodate the given components and features.

1.1 DAC Component

The TSW3000 Demo Kit is built for the DAC5687, although this Demo Kit can also support the DAC5686 since the two devices are pin compatible. The procedures outlined in this document are primarily suited for the DAC5687, but can be modified easily for the DAC5686 if desired.

1.2 VComm Configuration

The analog quadrature modulator requires a common-mode dc voltage of approximately 3.7 V. In order to utilize the dc-offset adjustment capabilities of the DAC568x for carrier suppression, it is imperative to maintain a dc path from the DAC output to the modulator input. The common-mode voltage for the modulator is maitained with a passive resistor network that is designed to provide the proper operation point for the DAC568x and the TRF370x modulator. By design, in order to preserve the proper dc levels, the DAC gain should be kept at maximum (15), though deviation by a few steps is generally acceptable with no degradation in performance.

1.3 VCXO

The CDCM7005 requires a VCXO source to derive its output clock signals. The VCXO is at reference designator U10 on the back side of the board. The frequency of the VCXO can be changed to operate the Demo Kit with different clocking schemes for different modulation standards or for specific customer requirements. Denote which VCXO frequency is on the board so that the CDCM7005 part can be set up properly. The following conventions are typically used:

- WCDMA: Derivatives of 61.44 MHz (i.e., 122.88 MHz, 245.76 MHz, 491.52 MHz)
- GSM: Derivatives of 52 MHz (i.e., 104 MHz, 208 MHz)
- CDMA2K: Derivativies of 78.6432 (i.e., 157.2864 MHz, 314.5728 MHz)

1.4 VCO

The VCO outputs the RF signal used for the LO drive on the analog quadrature modulator. The RF output frequency is contingent on the LO frequency value.

The RF frequency band of the VCO must be noted in order to know how to program the TRF3750 and where to measure the output RF signal from the modulator. The typical bands of operation are shown in Table 1.

Table 1. Frequency Bands

	UMTS	PCS	GSM900	DCS1800
FREQUENCY	2110-2170 MHz	1930-1990 MHz	935-960 MHz	1805-1880 MHz

2 Block Diagrams

2.1 System Block Diagram

The basic radio system block diagram in Figure 1 demonstrates where the TSW3000 Demo Kit fits in the overall transceiver. The dash-line box illustrates the components found on the TSW3000 Demo Kit board.

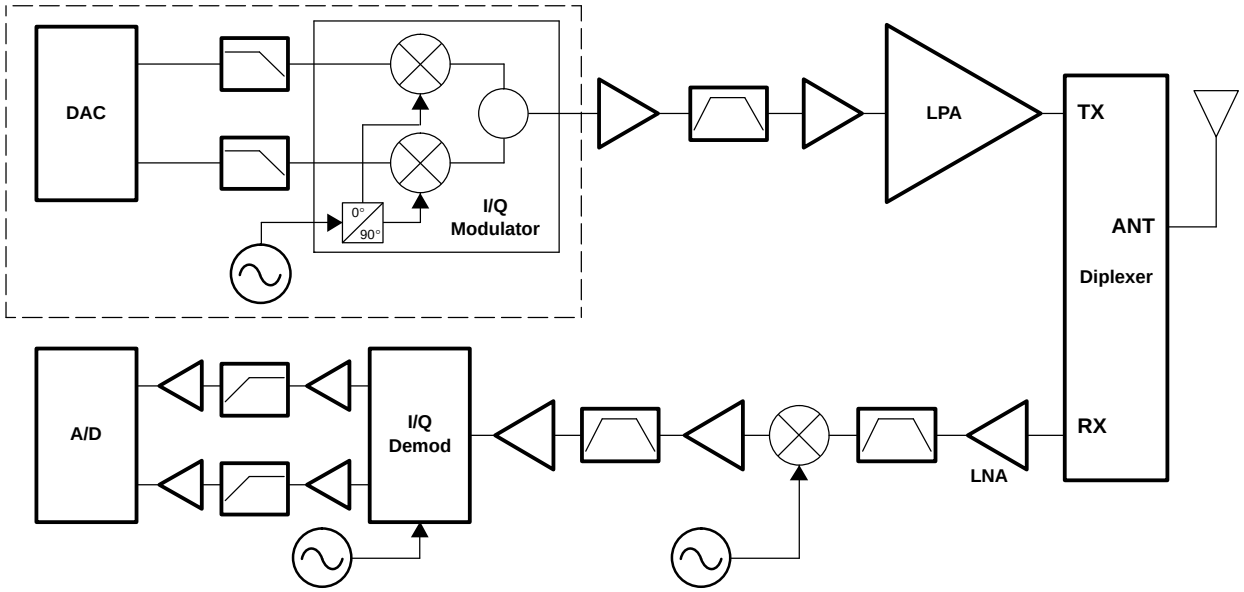

Figure 1. System Block Diagram

2.2 Demo Kit Block Diagram

The basic Demo Kit block diagram is shown in Figure 2. The shaded boxes illustrate the key Texas Instruments components found on the TSW3000 Demo Kit board.

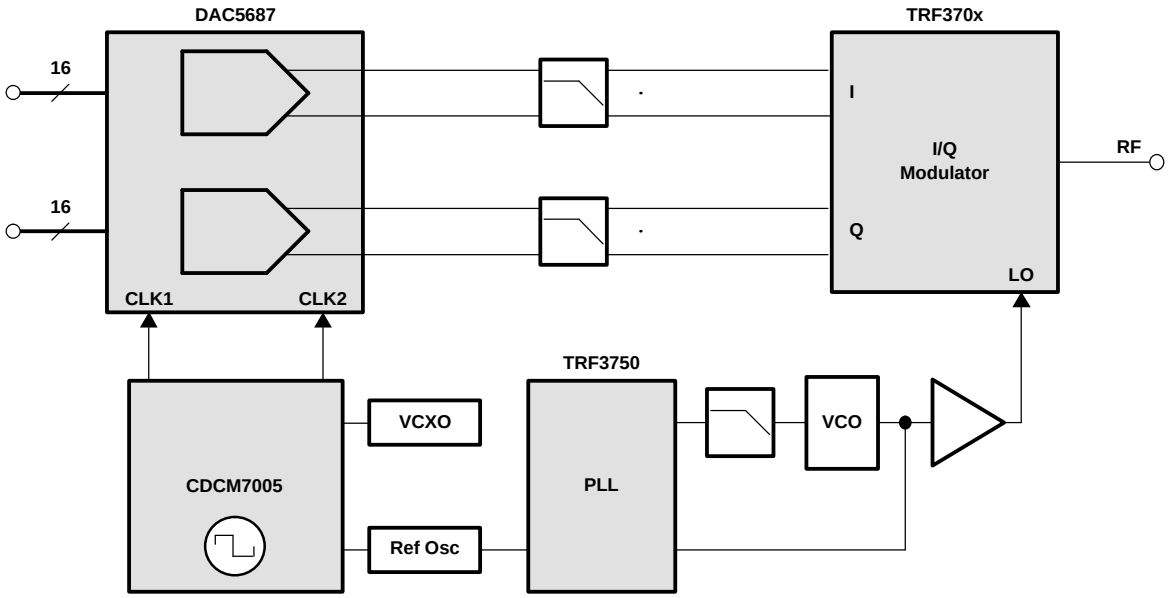

Figure 2. Demo Kit Block Diagram

3 Key Texas Instruments Components

3.1 CDCM7005

The CDCM7005 clock distribution chip is used to generate and synchronize the clock outputs to the system. The device has five outputs which can be either LVPECL or LVCMOS and can be divided down by 1, 2, 3, 4, 6, 8, and 16. The divide by 16 can be replaced with a divide by 4 or 8 with a 90 degree phase shift.

3.2 DAC5687

The DAC5687 is a 16-bit interpolating dual digital-to-analog converter (DAC). The device incorporates a digital modulator, independent differential offset control, and I/Q amplitude control. The device is typically used in baseband mode or in low IF mode in conjunction with an analog quadrature modulator.

3.3 TRF370x

The TRF370x is a direct upconvert I/Q modulator. The device accepts differential input voltage at baseband or low IF frequencies and outputs an RF signal based on the LO drive frequency.

3.4 TRF3750

The TRF3750 is a PLL chip used in the synthesizer section to generate the LO frequency required for the I/Q modulator.

4 Software Installation

This section summarizes the installation procedures for the software required to operate the Demo Kit. Once all of the software is loaded, it is recommended to reboot the computer.

- Extract TSW3000-Installv2p0.zip
- Execute setup.exe

5 Software Operation

The following describes the use of the software required to set the TSW3000 Demo Kit in the baseline configuration for the CDCM7005, TRF3750, and DAC5687. The software should be configured in the order presented below. The first step requires starting the TSW3000 software. This opens a window as shown in Figure 3. The tabs on the left side of the window allow selection of different GUI controllers for the DAC5687, TRF3750, and CDCM7005. The lower left portion of the screen contains links to this user's guide as well as the data sheets for the DAC5687, TRF3750, and the CDCM7005.

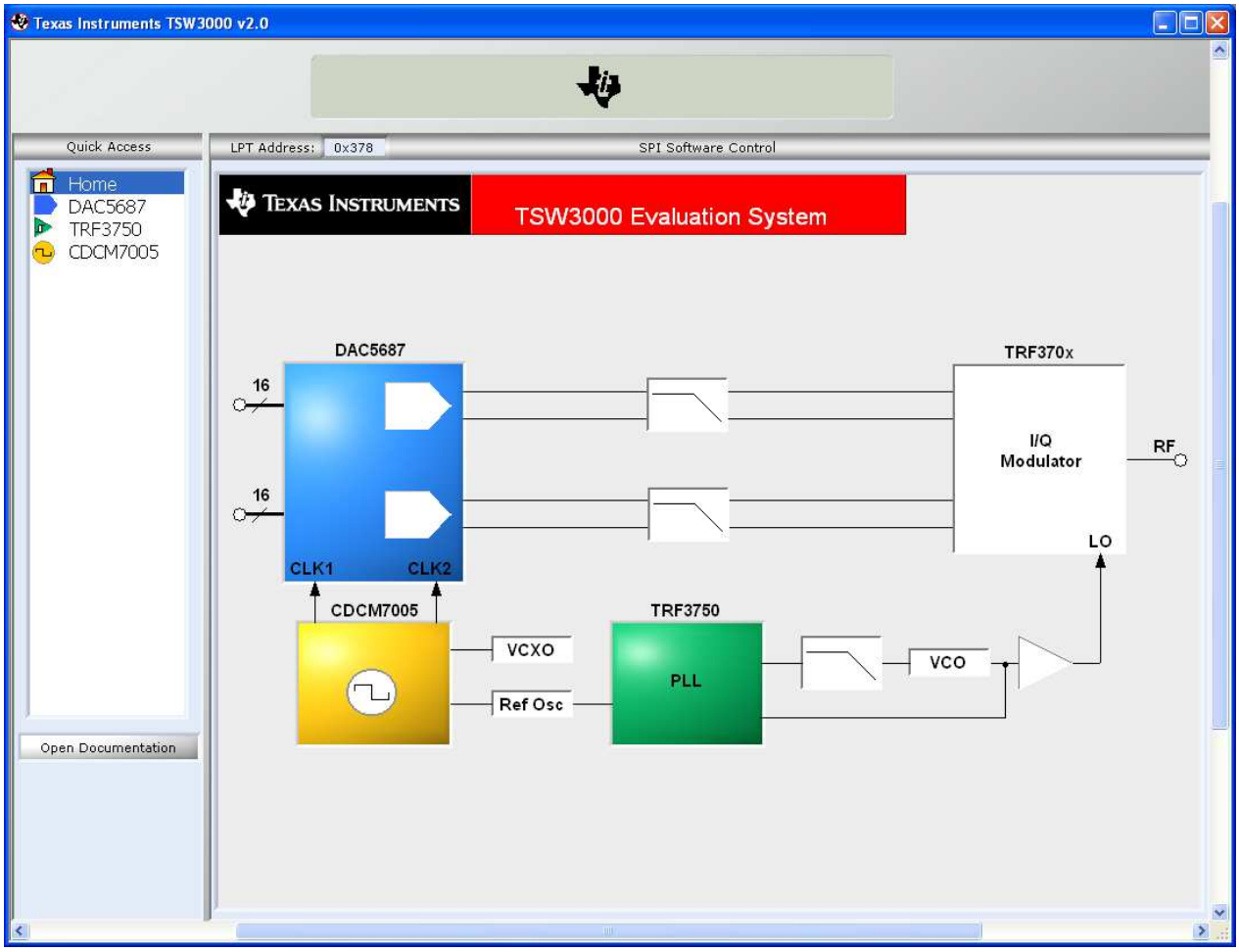

Figure 3. TSW3000 Startup Screen

5.1 CDCM7005 Software

By using the provided CDCM7005 serial peripheral interface (SPI) software, the user can load settings to the CDCM7005 internal registers. This must be performed every time the TSW3000 Demo Kit is powered up, since the CDCM7005 has default settings that are loaded at power up and the settings may be slightly different than the ones required to operate the Demo Kit. Executing the program brings up the interface seen in Figure 4. The default settings are correct for a VCXO of 491.52 MHz and a 10 MHz reference as on the TSW3000. The CDCM7005 GUI allows register settings to be saved and can be loaded back in afterwards. This can be accomplished with the Save and Load Settings buttons near the right side of the GUI.

It is recommended that any unused output clocks be tri-stated. In this case the TSW3000 only uses OUT_MUX_1 to drive the DAC5687. OUT_MUX_0, OUT_MUX_2, OUT_MUX_3, OUT_MUX_4 should be tri-stated unless there is a need to use the other output clocks.

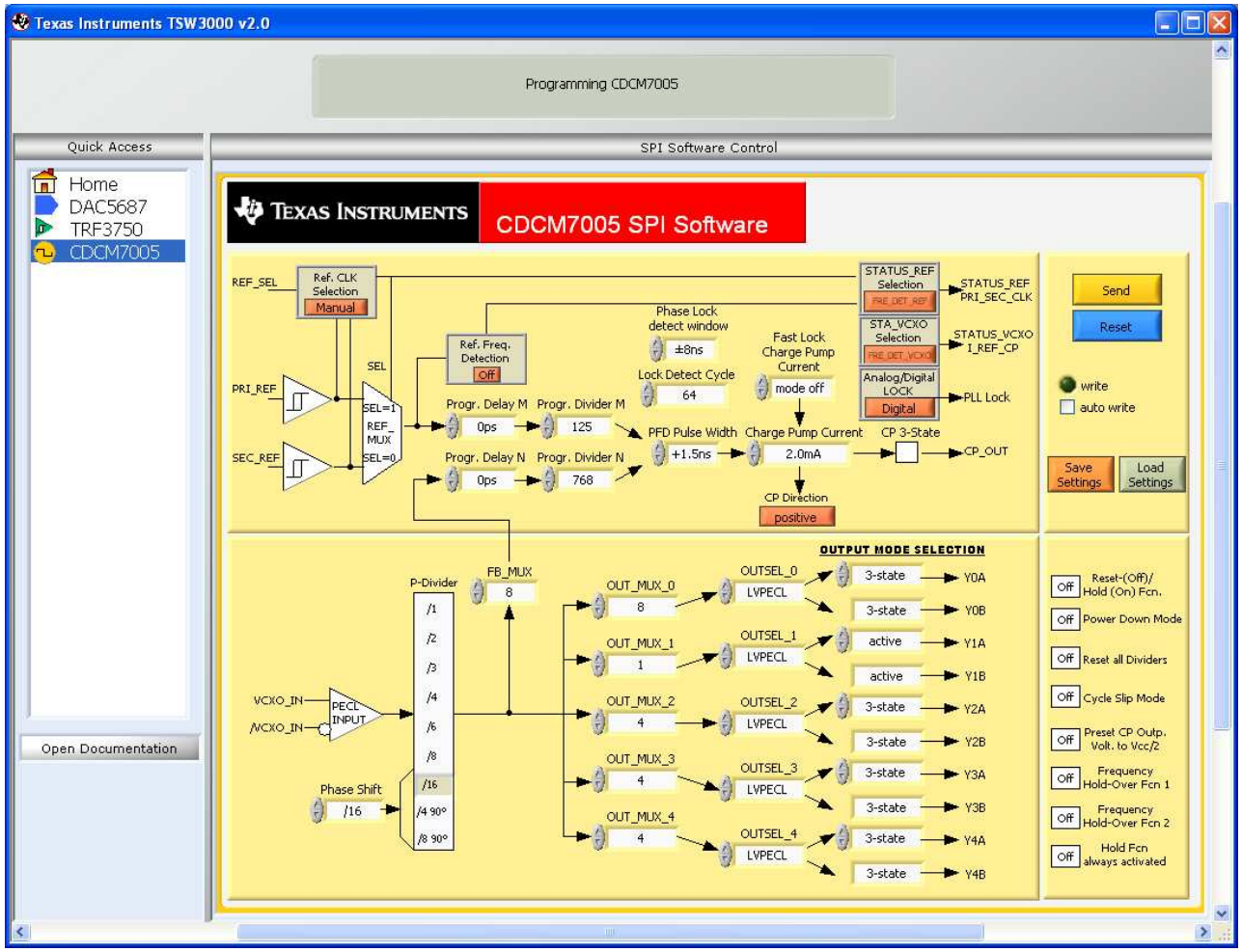

Figure 4. Default CDCM7005 SPI GUI

The divider parameters, M and N, are determined according to the following equation based on the internal reference frequency and internal VCXO frequency.

$F_{REF} = (F_{VCXO} \times M)/(N \times P)$

The p parameter is the VCXO input divider and set through the FB_MUX value. The M and N counter values need to be adjusted depending on the board configuration. The M and N counter registers are determined by the reference frequency and the VCXO frequency. The OUT_MUX sets the divide ratios for the individual output clocks. The OUTSEL determines whether the output clocks will be used as single-ended CMOS or differential LVPECL. With a 10-MHz reference oscillator the CDCM7005 settings are shown in Table 2 for a variety of common VCXO frequencies. For other frequencies, see to the CDCM7005 data sheet for more details.

Table 2. CDCM7005 Register Values

VCXO Freq. (MHz)	491.52	245.76	122.88	61.44
Divider M	125	125	125	125
Divider N	768	768	768	768
FB_MUX	8	4	2	1

5.2 TRF3750 Software

The TRF3750 software is used to program the PLL chip to lock the VCO oto a desired frequency output. The main menu of the program is shown in Figure 5.

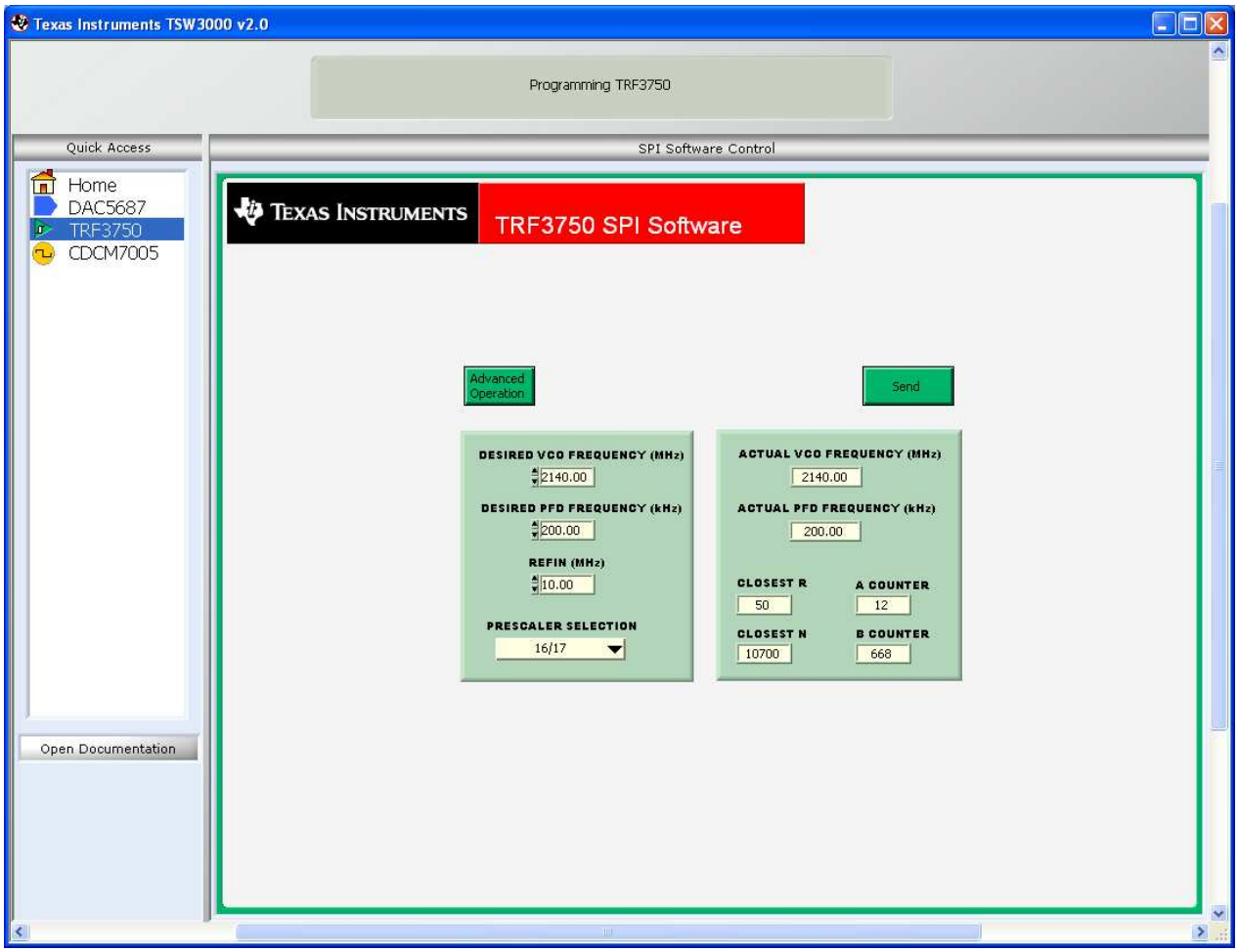

Figure 5. TRF3750 GUI - Main Menu

The options in the front panel allow the user to program the desired frequency of the VCO, the desired frequency of the PFD, the reference frequency, and the prescaler selection. The software then displays the actual VCO frequency, PFD frequency and the R, N, A, and B counter values to be programmed into the TRF3750. Hitting the Send button writes these values to the TRF3750. In default mode on a default board, only the desired VCO frequency (2100 MHz to 2200 MHz) needs to be changed. For other VCO ranges, other parameters may need to be changed.

The Advanced Operation button will bring up another user interface as shown in Figure 6.

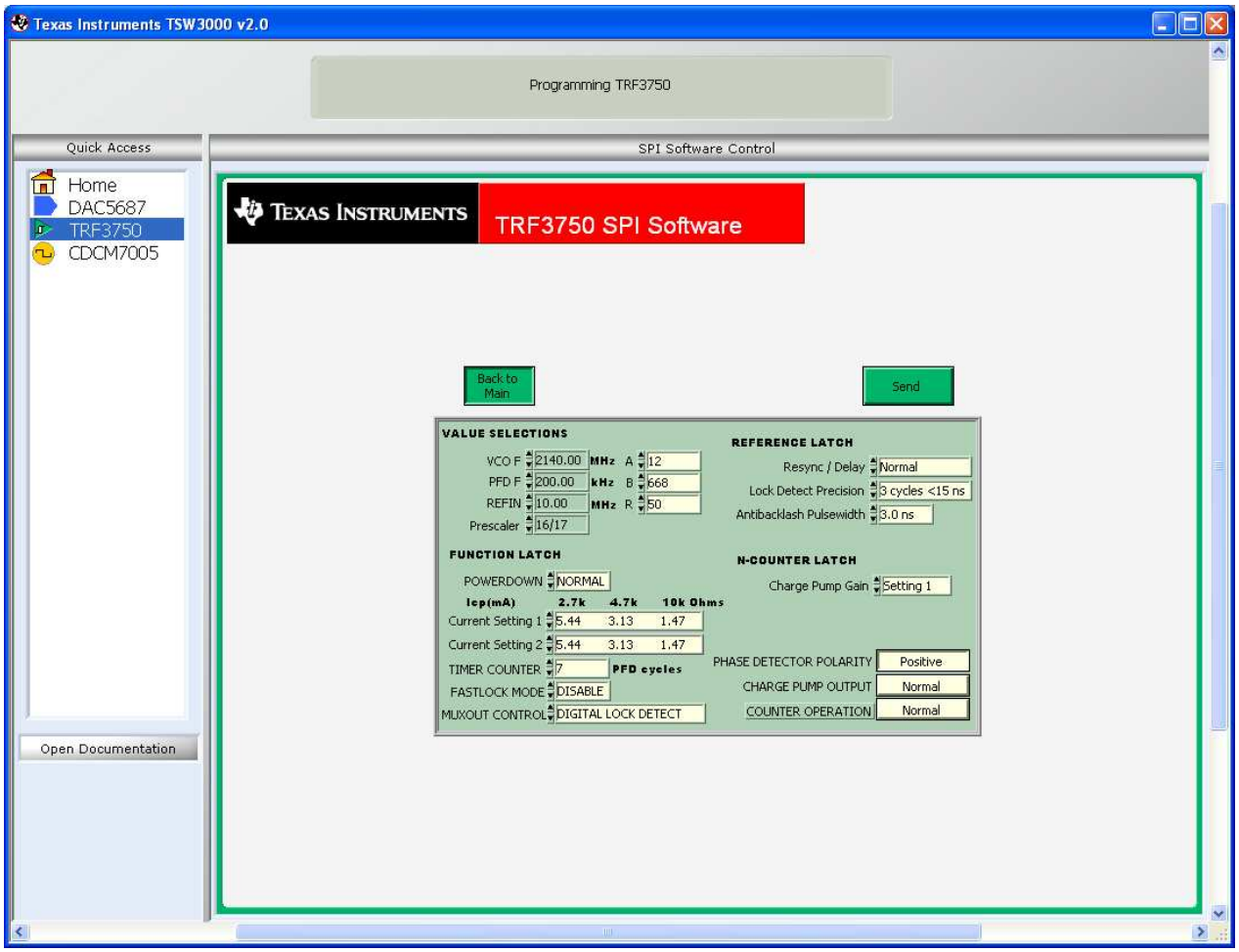

Figure 6. TRF3750 GUI - Advanced Menu

This menu allows control of more register settings. For details on these settings, see the TRF3750 data sheet (SLWS146). The register of interest in this menu is the MUXOUT CONTROL which can be used to determine the function of LED D4. This mode defaults to Digital PLL Lock Detect and causes the LED D4 to light up when the PLL successfully locks. Normally, these menu settings do not need to be changed.

5.3 DAC5687 Software

By using the provided software, the user can write and read control register information to the DAC5687. At first startup of this software, it is imperative to select the Pll Port Config button to bring up the parallel port configuration settings. From the menu, select the TSW3000 setting. This configures the port to be compatible with the TSW3000. Once the Demo Kit is powered on with the parallel port configured and connected properly, then the GUI shown in Figure 7 is displayed with the default settings read from the device. If there is a problem with the communication, such as the Demo Kit is not powered on or the parallel port cable is not connected, an error message will be displayed instructing the user to correct the problem. Once corrected, hit the Read All button to read the default settings of the device.

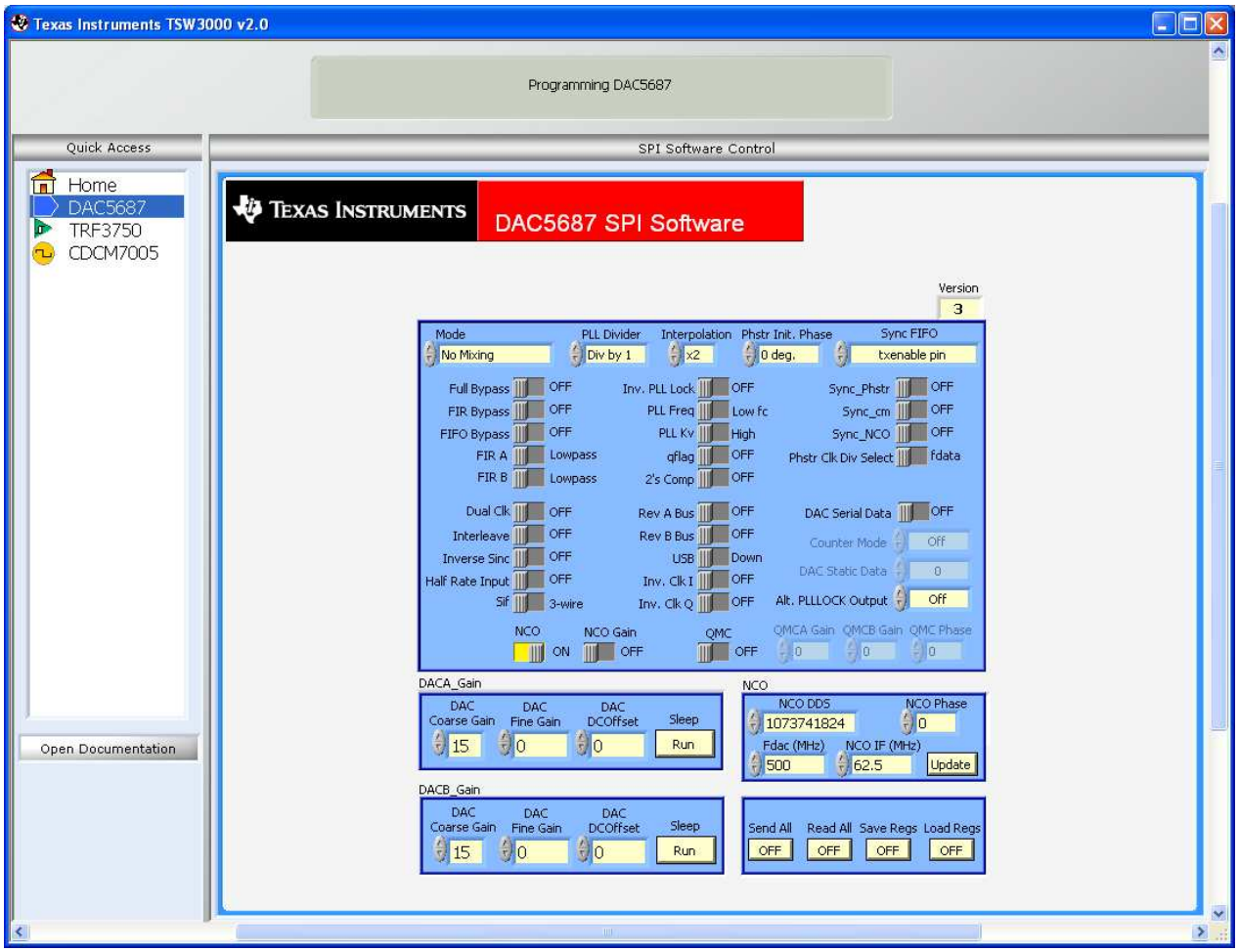

Figure 7. DAC5687 GUI

For normal operation, the user needs only to select values and switches as desired. The values are automatically sent to the device and read back to verify their configuration.

5.4 DAC5687 GUI Register Descriptions

5.4.1 Register Controls

- **Load Regs**– Loads register values from a saved file to the DAC5687 and updates the GUI.
- **Save Regs**– Saves current GUI registers settings to a text file for future use.
- **Read All**– Reads the current registers of the DAC5687. This is used to verify settings on the front panel.
- **Send All**– Sends the current front panel registers to the device. This is generally only used when the Demo Kit power has recycled or the device has been reset and the user wants to load the displayed settings to the device.

5.4.2 Configuration Controls

- **Full Bypass**– When set, all filtering, QMC, and NCO functions are bypassed.
- **FIR Bypass**– Bypass all interpolation filters. QMC INCO functional. Limited to FDAC = 250 MHz
- **FIFO Bypass**– When set to bypass, the internal four sample FIFO is disabled. When cleared, the FIFO is enabled.
- **FIR A**– A side first FIR filter in high-pass mode when set, low-pass mode when cleared.

- **FIR B**– B side first FIR filter in high-pass mode when set, low-pass mode when cleared.
- **Dual Clk**– Only used when the PLL is disabled. When set, two differential clocks are used to input the data to the chip; CLK1/CLK1C is used to latch the input data into the chip, and CLK2/CLK2C is used as the DAC sample clock.
- **Interleave**– When set, interleaved input data mode is enabled; both A and B data streams are input at the DA(15:0) input pins.
- **Inverse Sinc**– Enables inverse sinc filter.
- **Half Rate Input**– Enables half rate input mode. Input data for the DAC A data path is input to the chip at half speed using both the DA(15:0) and DB(15:0) input pins.
- **Sif**– Sets sif_4-pin bit. A 4-pin serial interface mode is enabled when on, 3-pin mode when off. The DAC5687 Demo Kit is configured for a 3-pin serial interface, so setting to a 4-bit serial interface makes reading registers impossible with the GUI.
- **Inv. PLL Lock**– Only used when PLL is disabled and dual clock mode is disabled. When cleared, input data is latched into the chip on rising edges of the PLLLOCK output pin. When set, input data is latched into the chip on falling edges of the PLLLOCK output pin.
- **PLL Freq**– Sets PLL VCO center frequency to low or high center frequency.
- **PLL Kv**– Sets PLL VCO gain to either high or low gain.
- **Qflag**– Sets qflag bit. When set, the QFLAG input pin operates as a B sample indicator when interleaved data is enabled. When cleared, the TXENABLE rising determines the A/B timing relationship.
- **2's Comp**– When set, input data is interpreted as 2's complement. When cleared, input data is interpreted as offset binary.
- **Rev A Bus**– When cleared, DA input data MSB to LSB order is DA(15) = MSB and DA(0) = LSB. When set, DA input data MSB to LSB order is reversed, DA(15) = LSB and DA(0) = MSB.
- **Rev B Bus**– When cleared, DB input data MSB to LSB order is DB(15) = MSB and DB(0) = LSB. When set, DB input data MSB to LSB order is reversed, DB(15) = LSB and DB(0) = MSB.
- **USB**– When set, the data to DACB is inverted to generate upper side band output.
- **Inv. Clk I(Q)**– Inverts the DAC core sample clock when set, normal when cleared.
- **Sync_Phstr**– When set, the internal clock divider logic is initialized with a PHSTR pin low to high transition.
- **Sync_cm**– When set, the coarse mixer is synchronized with a PHSTR low-to-high transition.
- **Sync_NCO**– When set, the NCO phase accumulator is cleared with a phstr low-to-high transition.
- **Phstr Clk Div Select**– Selects the clock used to latch the PHSTR input when restarting the internal clock dividers. When set, the full rate CLK2 signal latches PHSTR and when cleared, the divided down input clock signal latches PHSTR.
- **DAC Serial Data**– When set, both DAC A and DAC B input data is replaced with fixed data loaded into the 16-bit serial interface DAC Static Data.
  - **Counter Mode**– Controls the internal counter that can be used as the DAC data source: {off; all 16b; 7b LSBs; 5b MIDs; 5b MSBs}.
  - **DAC Static Data**– When DAC Serial Data is set, both DAC A and DAC B input data is replaced with fixed data loaded with this value. Range = 0 - 65535.
- **Alt. PLLLOCK Output**– Can be used to determine alternate outputs on the PLLLOCK pin when using the internal PLL mode. The EXTLO pin must be open when using this mode.
- **NCO**– When set, enables NCO.
  - **NCO Gain**– Sets NCO gain resulting in a 2x increase in NCO output amplitude. Except for $F_s/2$ and $F_s/4$ mixing NCO frequencies, this selection can result in saturation for full-scale inputs. Consider using QMC gain for lower gains.
- **QMC**– When set, enables the QMC.
  - **QMCA Gain**– Sets QMC gain A to a range = 0 to 2047. See the data sheet for more information.
  - **QMC B Gain**– Sets QMC gain B to a range = 0 to 2047. See the data sheet for more information.
  - **QMC Phase**– Sets QMC phase to a range = -512 to 511. See the data sheet for more information. Used to adjust for I/Q phase imbalance.
- **Mode**– Used to select the coarse mixer mode. See the DAC5687 data sheet for more information.

- **PLL Divider**– Sets VCO divider to div by 1, 2, 4, or 8.
- **Interpolation** – Sets FIR Interpolation factor: {X2, X4, X4L, X8}. X4 uses lower power than 4xL, but F_{dac} = 320 MHz max when NCO or QMC are used.
- **Phstr Init. Phase** – Adjusts the initial phase of the fs/2 and fs/4 cmix block at PHSTR.
- **Sync FIFO**– Sync source selection mode for the FIFO. When a low to high transition is detected on the selected sync source, the FIFO input and output pointers are initialized. See the DAC5687 data sheet for source description.

5.4.3 DAC A(B) Gain

- **DAC Coarse Gain**– Sets coarse gain of DAC A(B) full-scale current. Range is 0 to 15. See the DAC5687 data sheet for full-scale gain equation.
- **DAC Fine Gain**– Sets fine gain of DAC A(B) full scale current. Range is -128 to127. See the DAC5687 data sheet for full-scale gain equation. Used to adjust for I/Q amplitude imbalance.
- **DAC DCOffset**– Sets DAC A(B) dc-offset register. Range is -4096 to 4095. Used to adjust for carrier suppression.
- **Sleep**– DAC A(B) sleeps when set, operational when cleared.

5.4.4 NCO

- **NCO DDS**– Sets NCO DDS registers. See the DAC5687 data sheet for formula.
- **NCO Phase**– Sets initial NCO phase registers. See the DAC5687 data sheet for more information.
- **F_{DAC} (MHz), NCO IF (MHz)**– Used to calculate the required NCO DDS value.

5.4.5 Additional Control/Monitor Registers

- **Version**– Displays the version of the silicon. If a version of 0 is read then the communication is not functioning and an error message will be displayed.

6 Board Setup

6.1 Jumper Settings

The TSW3000 Demo Kit has on-board jumpers that allow the user to selectively disengage devices as desired. The unit is shipped with jumpers in place that activate all of the devices on board. Table 3 explains the functionality of the jumpers on the board.

Table 3. Jumper List

JUMPER	LABEL	FUNCTION	CONDITION	DEFAULT
W1	PLL Lock	2-pin access port for monitoring PLL lock of the DAC5687	Open	Installed
W2	PWD	Power down for the TRF370x	Powered	Pin 1, 2
W6	LO Buffer	Disengages power to LO buffer amp	Powered	Installed
W5	IOVDD	Toggles 3.3 V or 1.8 V to IOVDD on the DAC5687	3.3 V Engaged	Pin 1, 2
J15 pin 2	PLLVDD	Toggles power to the DAC PLL	Not Powered	Pin 1, 2
J15 pin 5	SLEEP	Power down for the DAC5687	Open	Removed
J15 pin 8	EXTLO	Toggles internal reference ground	Grounded	Pin 7, 8
J15 pin 11	TXENABLE	Selects interleaved data	Powered	Pin 11, 12
J15 pin 14	TESTMODE	DO NOT POPULATE!	Open	Removed
J15 pin 17	QFLAG	Used to flag the DAC5687 channel B data in interleave mode	Open	Removed
J15 pin 20	CDC_PD	Power down of the CDCM7005	Open	Removed
J15 pin 23	REF_SEL	Selecets reference for CDCM7005	Open	Removed
J15 pin 27	PLL_PWD	Power down the TRF3750	Powered	Pin 26, 27

Table 3. Jumper List (continued)

JUMPER	LABEL	FUNCTION	CONDITION	DEFAULT
J15 pin 29	RESET	Resets the DAC5687 when low	Open	Removed

6.2 Input/Output Connectors

The input and output connections are shown in Table 4.

Table 4. Input/Output Connections

REFERENCE DESIGNATOR	CONNECTOR TYPE	DESCRIPTION
J13	34-pin header	I channel data input
J14	34-pin header	Q channel data input
J9	SMA	RF output
J10	SMA	Optional LO input
J8	SMA	Optional external reference
J2	SMA	Output clock 1 from CDCM7005
J3	SMA	Output clock 2 from CDCM7005
J5	SMA	Optional I out A from DAC5687
J19	SMA	Optional Q out B from DAC5687
J6	SMA	Input for external VCXO for CDCM7005
J7	SMA	PLL lock status on DAC5687
J4	SMA	Phase synchronization on DAC5687

RF shield covers should be in place over the synthesizer section and the RF modulator section. These shields provide isolation of the RF sections on the board.

6.3 Parallel Port

The TSW3000 Demo Kit contains a 25-pin parallel port connector (J1) to interface to a standard computer parallel port. Programming of the CDCM7005, DAC5687, and TRF3750 are accomplished through this port.

6.4 DC Power Requirements

The Demo Kit requires a single dc-voltage supply that is nominally 6 V. From that supply, the 5 V, 3.3 V, and 1.8 V required for the devices on the board are generated internally through linear voltage regulators. It is possible to use a higher input voltage; however, care should be taken not to over dissipate the on-board voltage regulators.

7 Demo Kit Test Configuration

7.1 Test Setup Block Diagram

The test set up for general testing of the TSW3000 Demo Kit is shown in Figure 8.

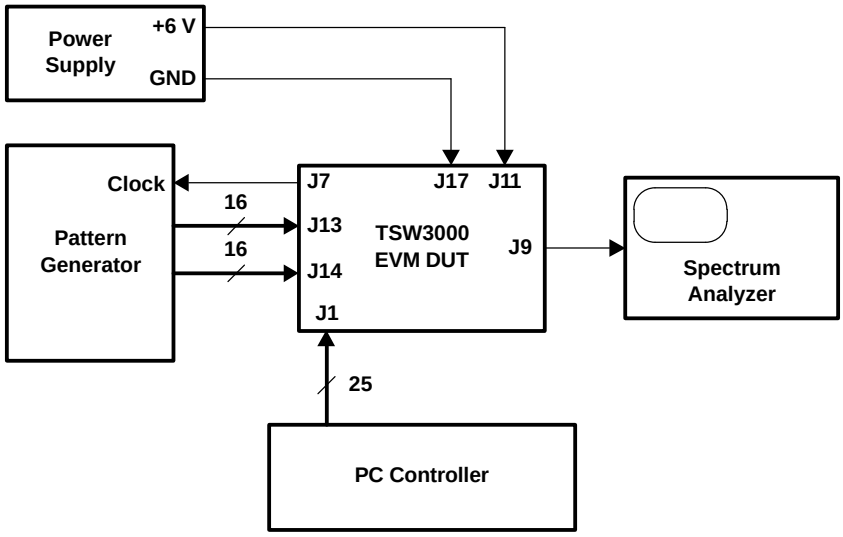

Figure 8. Test System Block Diagram

7.2 Test Equipment

The following is a list of the test equipment required for testing the TSW3000 Demo Kit. Equivalent models may be used for certain applications, but may produce different results due to limitations within the instrument.

- Dual Power Supply: Any with current readout capability
- Spectrum Analyzer: Rhode & Schwartz FSU, Agilent PSA, or equivalent
  This particular piece can measure >70-dBc ACPR with the noise cancellation option active. This amount of dynamic range is required to accurately measure the ACPR of the Demo Kit. Another spectrum analyzer can be substituted if it achieves as good or better dynamic range.
- Pattern Generator: Agilent 16702B
- Oscilloscope: Tektronix 650 or equivalent
  Used to probe clock output signals and for debugging.
- Digital Voltmeter: Agilent 34401A or equivalent

7.3 Calibration

In order to record proper output power the insertion loss of the output cable must calibrated. Measure the insertion loss of the cable from J9 to the spectrum analyzer; set the analyzer's reference level offset to that value.

7.4 Test Specifications

The test specifications are outlined in Table 5.

Table 5. Demo Kit Specifications

	MIN	MAX	UNITS
CURRENT			
+6 V		1.5	A
CW TESTS			

Table 5. Demo Kit Specifications (continued)

	MIN	MAX	UNITS
Carrier suppression	30		dBc
Sideband rejection	25		dBc
Spurious Output			
2nd harmonic	45		dBc
Aliased LSB (pos)	40		dBc
Output clock	40		dBc
Aliased USB	15		dBc
Aliased USB (neg)	8		dBc
WCDMA ACPR			
Channel power		-14	dBm
ACPR -Low	70		dBc
ACPR -High	70		dBc

8 Basic Test Procedure

This section outlines the basic test procedure to get the Demo Kit operational. Disconnect the cables at J13 and J14 that connect to the pattern generator. Connect the power supply cable and the RF output to the spectrum analyzer.

8.1 Initial Inspection

Inspect the board to determine which devices were used.

- Note the VCXO frequency (U10) that is on the board
- Note the VCO frequency band (Y3) that is on the board

8.2 Engage Power Supplies

Engage 6-V power supply

- Verify the current reading is between 0.8 A to 1.3 A when configured with the DAC5687

8.3 Program the CDCM7005

Use the Default Settings on the CDCM7005 GUI (See Section 5.1). This generates a 491.52-MHz clock.

- Set the OUT_MUX_0, 2, 3, 4 to tristate. Only OUT_MUX_1 is used for clocking the DAC5687
- Hit the GUI Send button
- Verify that LEDs D1, D2, and D3 are illuminated

8.4 Program the TRF3750

Use the Default Settings in the TRF3750 GUI (See Section 5.2). This places a carrier at 2.14 GHz

- Hit the GUI send button.
- Verify the LED D4 is illuminated. This indicates lock of the VCXO and TCXO reference.
- Monitor RF output from the spectrum analyzer
- Verify a single frequency tone at the default 2.14 GHz.

Table 6. Frequency Designations

VCO BAND	UMTS	GSM900	PCS	DCS1800
Midband (MHz)	2140	950	1960	1850
Low (MHz)	2110	935	1930	1805
High (MHz)	2170	960	1990	1880

8.5 DAC5687 Program

- Disable the PLL by removing the jumper at J15, pins 2 and 3, if not already removed.
- Verify DACA and DACB Coarse Gain is set to 15
- Set Mode to 0000 (No Coarse Mixing)
- Ensure DAC Offsets and DAC fine gain for both A and B are set to 0
- Set the spectrum analyzer as follows:
  - Center Freq: 2.14 GHz
  - RBW: 30 kHz, VBW: 300 kHz
  - Span: 491.52 MHz
  - Attn: 5 dB
  - Ref Level: 10 dBm

8.6 Carrier Suppression

The carrier suppression can be tuned for better performance by adjusting the dc-offset controls on the DAC5687. The default DAC GUI is shown below with the NCO mixer turned on to output a 61.44-MHz tone. The output spectrum is illustrated in Figure 10.

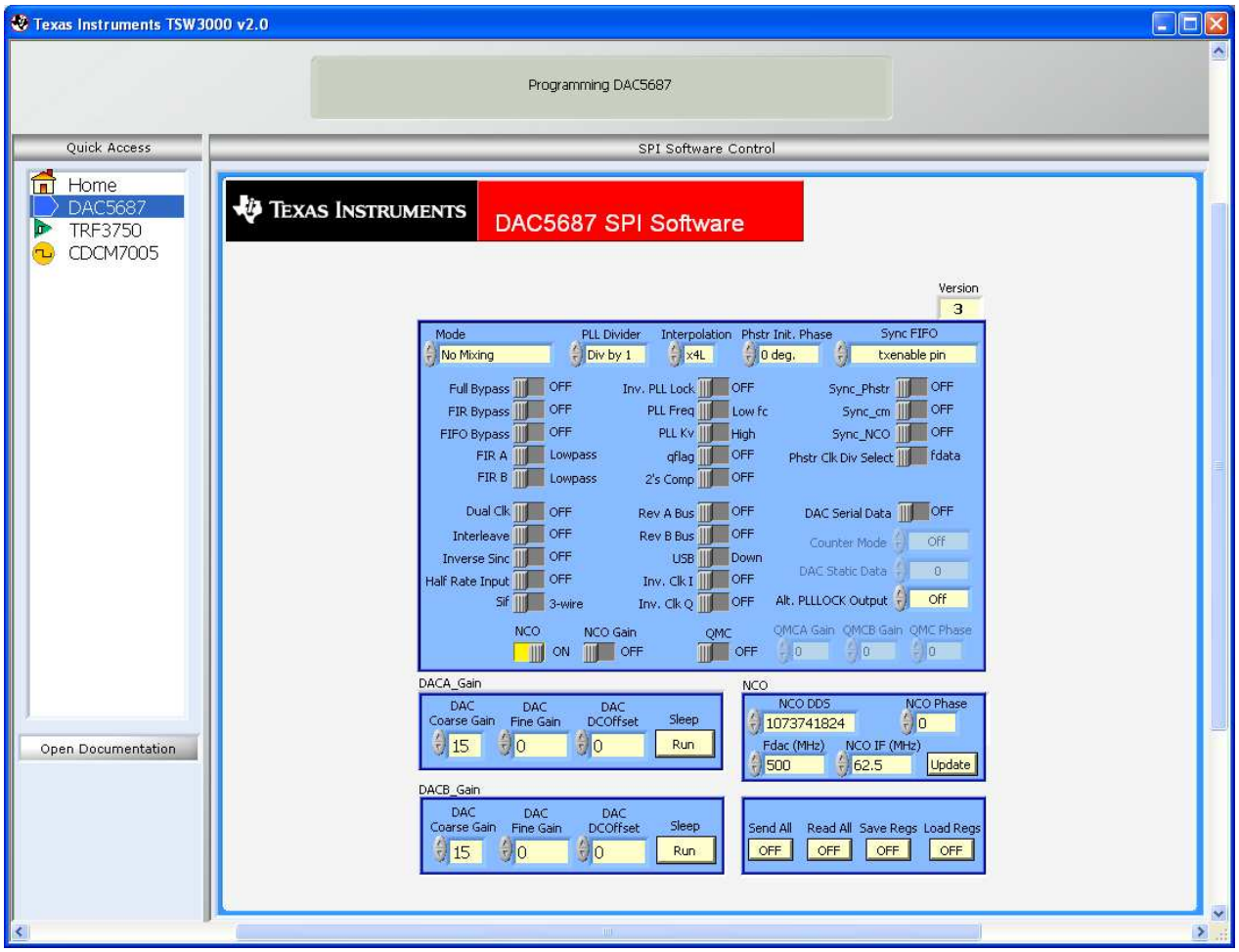

Figure 9. Default DAC GUI With f_{DAC}/8 Tone From NCO

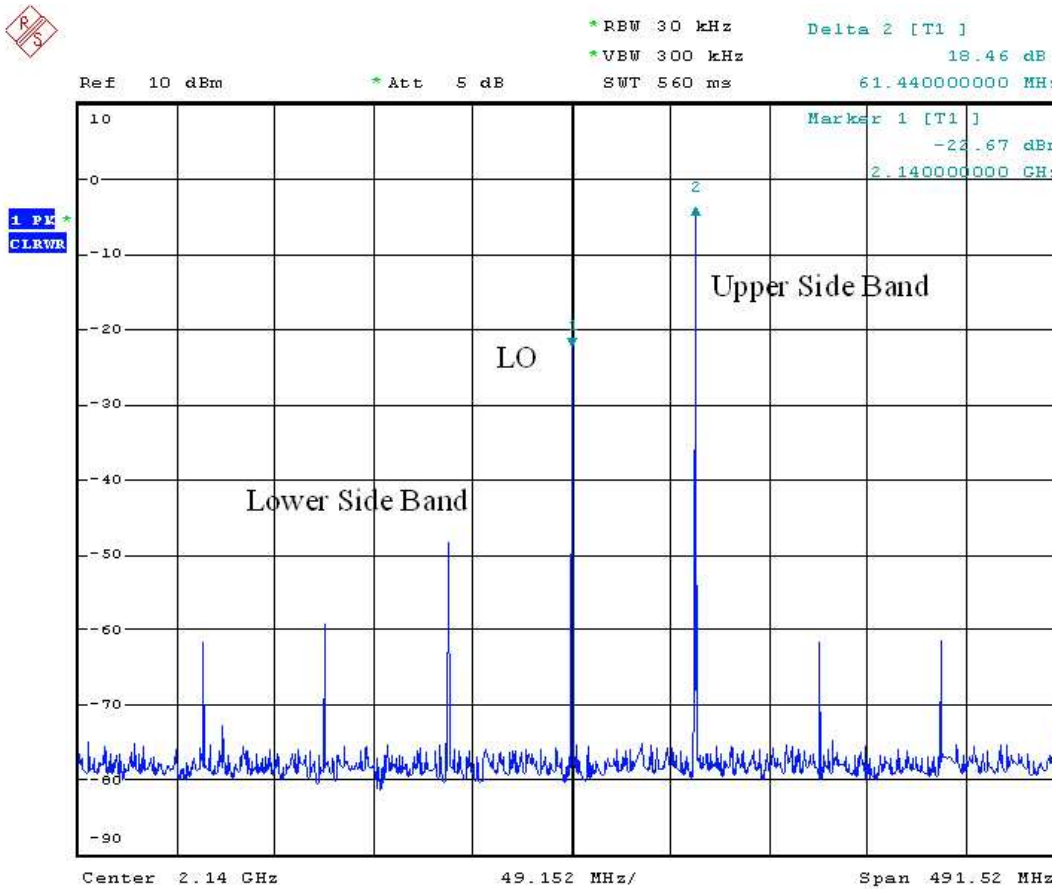

Figure 10. Single Sideband Spectrum Output Before DAC Offset and QMC Adjustments

An iterative process is used to achieve the best performance.

- Place a normal marker at the peak upper sideband, place a delta marker at the carrier signal, and note the initial delta value.
- Set initial DACA offset to 1000 and DACB offset to -1000
- Change DACA offset by 1000 steps and monitor the output performance change.
- If performance gets better, then repeat the process with an additional 1000 steps. If the performance gets worse or doesn't change, then change the offset in the other direction by 1000 steps.
- Once the performance remains basically unchanged, repeat the process on DACB offset with 1000 step changes.
- Once optimized, go back to the A side and repeat the tuning process with a step size of 100.
- Continue tuning. After each complete cycle, reduce the step size down (i.e., to 10, then to 1 if desired).
- A performance greater that 65 dBc should be achievable.

8.7 Sideband Rejection

Sideband rejection is determined by the two quadrature signals to the modulator being exactly 180 degrees out of phase and exactly the same amplitude. Amplitude and phase imbalance between the two paths yield an unwanted lower sideband. The amplitude variation between the two paths can be compensated for by adjusting the DAC fine gain controls or by adjusting the QMC gain controls if the device is operating with the QMC on. The phase can be compensated by using the QMC phase adjustment. Note this is only possible when the coarse mixer is not used in the $f_{DAC}/4$ mode. Coarse mixing in the $f_{DAC}/4$ mode causes the relative phase information between I and Q paths to be mixed. In the $f_{DAC}/2$ mode there are no cross terms (terms are 0) and the relative phase information is maintained between I and Q paths.

- Place marker delta on the lower sideband
- Turn on the QMC. Set the Gain of the QMC to 1024 for gain of 0 dB for I and Q paths. Other initial settings may be needed depending on the state of the NCO gain and signal amplitude.
- Change the phase of the QMC by small increments until the sideband is minimized.
- Change the QMC A or B gains in increments of 1 until the sideband is minimized.
- The overall performance should be greater than 60 dBc from the other sideband with amplitude and phase corrections.
- Re-optimized the dc-offset values as required to maintain carrier suppression performance as specified.

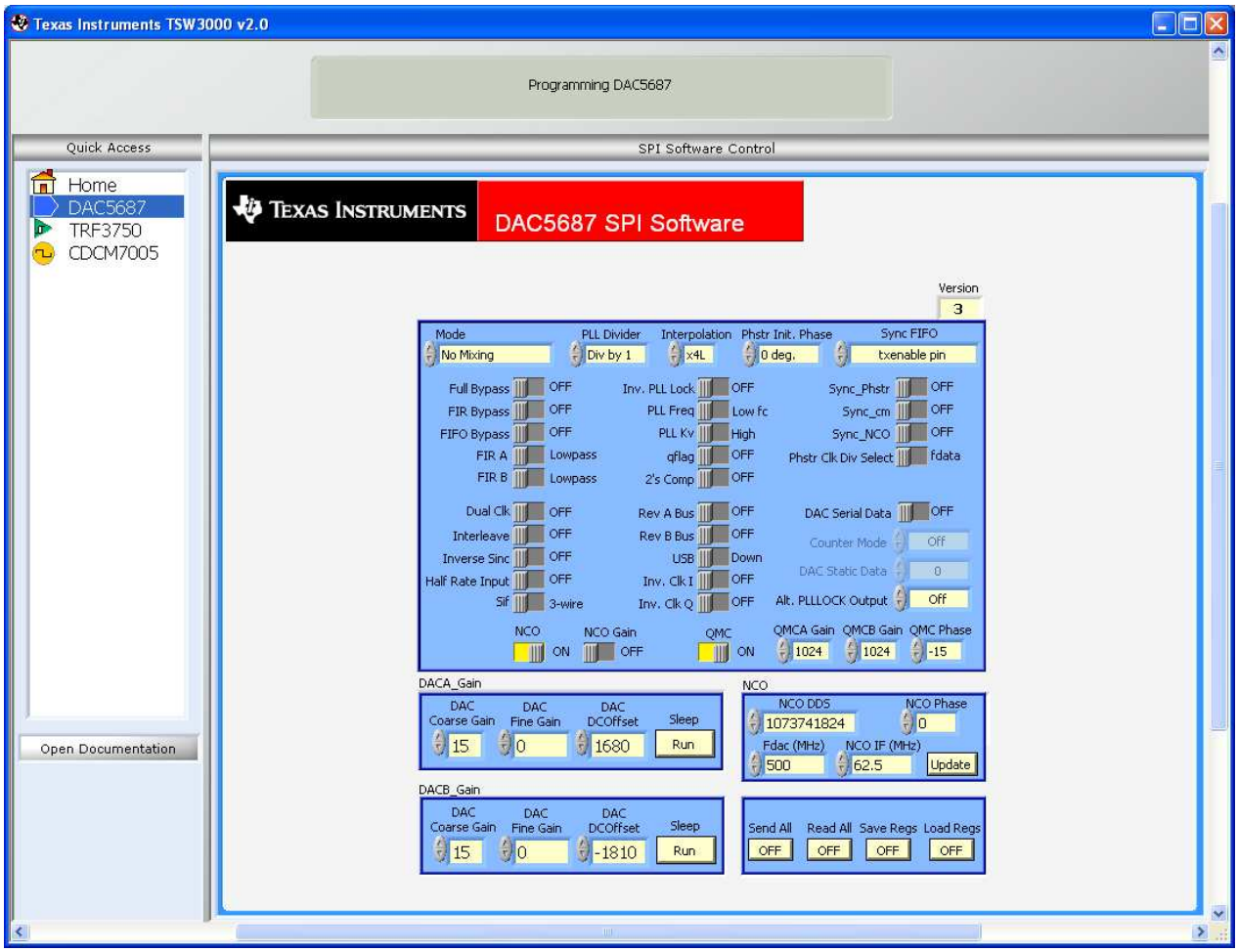

Figure 11. DAC GUI With Typical Settings To Minimize LO and Sideband

Sideband and LO are reduced into the noise floor. Clock related spurs can be filtered out using an RF filter.

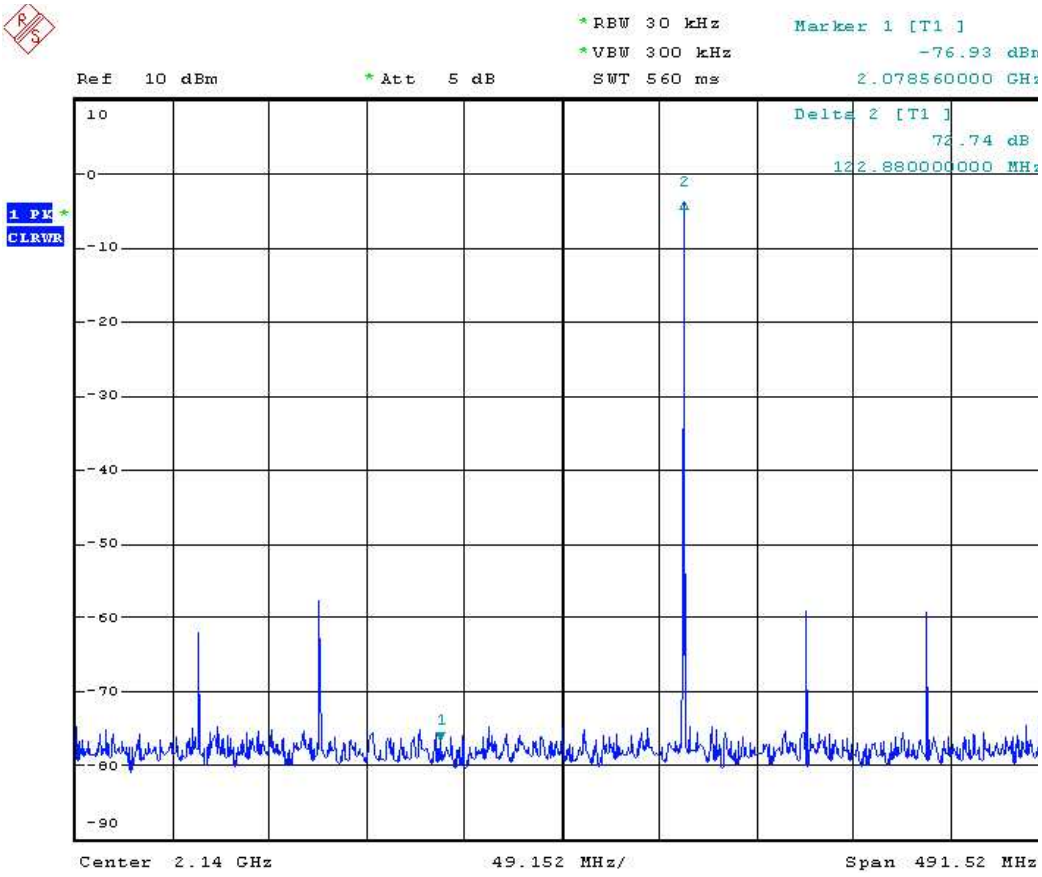

Figure 12. Sideband and LO

9 Optional Configurations

9.1 External LO

To configure the board for external LO implement the following modifications

- Remove R225
- Place R2: 0-Ω resistor, this connects the external LO on J10 to the TRF3702 modulator
- Remove W6 (disengages power to RF amplifier)
- Disable the TRF3750 PLL CE by setting J15-25, 26. This puts GND on CE of the TRF3750 and disables the PLL.

9.2 External Reference

To configure the board for an external reference implement the following modifications.

- Remove R144, this disconnects the on board 10-MHz reference
- Place R201: 0-Ω resistor, external reference can be hooked up to J8

9.3 Monitor DAC Output

9.3.1 Single Ended

To configure the board to monitor the DAC output by utilizing the transformers on board to achieve a single-ended output, implement the following modifications.

- Remove R187, R188, R191, R190, R208, R209, R210, R211
- Place R200, R224, R222, R223: 0-Ω resistors
- Place R179, R183, R212, R213: 100-Ω resistor. This configures the DAC output as in the DAC5687 data sheet for 4:1 impedance transformer.

Monitor outputs at J5 and J19.

10 Filter Specifications

10.1 Baseband Filter

The TSW3000 Demo Kit layout provides the opportunity to place components to realize up to a 7th order LC filter. The Demo Kit is by default populated with a 500-MHz LC low-pass filter to help eliminate DAC images and also out of band clock spurs which may mix into RF frequencies.

10.1.1 RF Filter/Output Match

The TSW3000 Demo Kit layout also provides the opportunity to place a small 3rd order LC filter on the output of the modulator for either filtering or impedance matching purposes. This filter has been disabled by removing the shunt capacitive elements and replacing the series inductor element with a 0-Ω resistor.

11 Layers and Schematics

This chapter contains the layers and schematics for the TSW3000 Demo Kit.

11.1 Bill of Materials

Table 7 lists the parts used in constructing the TSW3000 Demo Kit.

Table 7. Bill of Materials

Value	QTY	Part Number	Vendor	Ref Des	Not Installed
CAPACITORS					
TANT 47 µF, 10%, 10 V capacitor	7	ECS-T1AD476R	Panasonic	C25, C67, C70, C74, C105, C124, C160	
TANT 10 µF, 10%, 10 V capacitor	18	ECS-T1AX106R	Panasonic	C24, C35, C37-C41, C51, C83, C99, C116, C117, C121, C123, C129, C153, C156, C161	
TANT 10 µF, 10 V, 10% capacitor	2	T491C106K010AS	Kemet	C22, C101	
TANT 22 µF, 10 V, 10% capacitor	1	T491C226K010AS	Kemet	C96	
1 µF, 25 V, 10% capacitor	6	ECJ-3YB1E105K	Panasonic	C47, C50, C53, C54, C144, C159	
0.01 µF, 50 V, 10% capacitor	5	ECJ-2VB1H103K	Panasonic	C57, C60, C64, C102, C109	
0.1 F, 16 V, 10% capacitor	8	ECJ-2VB1C104K	Panasonic	C20, C21, C23, C26, C27, C75, C81, C106	
1 pF, 50 V, ±0.25 pF capacitor	4	ECJ-2VC1H010C	Panasonic	C30, C32, C125, C126	
2.2 pF, 50 V, ±0.25% capacitor	3	08055A2R2CAT2A	AVX	C19, C31, C68	
0.0018 µF, 50 V 5% capacitor	0	ECJ-2VC1H182J	Panasonic		C66, C72
6.8 pF, 50 V, ±0.25% capacitor	2	08055A6R8CAT2A	AVX	C63, C65	
47 pF, 50 V, 5% capacitor	0	ECJ-2VC1H470J	Panasonic		C93, C95
1 µF, 16 V, 10% capacitor	1	ECJ-1VB1C105K	Panasonic	C91	

Table 7. Bill of Materials (continued)

Value	QTY	Part Number	Vendor	Ref Des	Not Installed
0.1 µF, 16 V, 10% capacitor	16	ECJ-1VB1C104K	Panasonic	C28, C43-C45, C48, C76, C78-C80, C82, C87, C89, C90, C134, C151, C152	
0.01 µF, 16 V, 10% capacitor	5	ECJ-1VB1C103K	Panasonic	C46, C52, C56, C62, C130	
10 pF, 50 V, ±0.5 pF, capacitor	8	ECJ-1VC1H100D	Panasonic	C61, C97, C107, C108, C111, C127, C128, C158	
22 pF, 50 V, 5%, capacitor	3	ECJ-1VC1H220J	Panasonic	C146, C148, C149	
33 pF, 50 V, 5%, capacitor	0	ECJ-1VC1H330J	Panasonic		C142
0.47 µF, 6.3 V, 10%, capacitor	1	ECJ-1VB0J474K	Panasonic	C92	
1 pF, 50 V, 5%, capacitor	0	ECJ-1VC1H010C	Panasonic		C98
82 pF, 50 V, 5%, capacitor	1	ECJ-1VC1H820J	Panasonic	C141	
100 pF, 50 V, 5%, capacitor	5	ECJ-1VC1H101J	Panasonic	C132, C133, C135-C137	
330 pF, 50 V, 5%, capacitor	1	ECJ-1VC1H331J	Panasonic	C33	
560 pF, 50 V, 5%, capacitor	1	ECJ-1VC1H561J	Panasonic	C110	
1000 pF, 50 V, 5%, capacitor	4	ECJ-1VC1H102J	Panasonic	C88, C139, C140, C147	
0.1 µF, 10 V, 10% capacitor	34	ECJ-0EB1A104K	Panasonic	C1-C18, C29, C36, C49, C58, C69, C73, C84, C85, C86, C100, C104, C112-C115, C120	
0.01 µF, 16 V, 10% capacitor	2	ECJ-0EB1C103K	Panasonic	C71, C122	
0.001 µF, 25 V, 10% capacitor	2	ECJ-0EB1E102K	Panasonic	C119, C131	
0.033 µF, 10 V, 10% capacitor	1	ECJ-0EB1A333K	Panasonic	C34	
RESISTORS					
2 kΩ resistor, 1/10 W, 1%	2	ECJ-0EB1C103K	Panasonic	R8, R11	
10 kΩ resistor, 1/10 W, 1%	6	ERJ-6ENF1002V	Panasonic	R17, R34-37, R155	
47.5 Ω resistor, 1/10 W, 1%	2	ERJ-6ENF47R5V	Panasonic	R146, R147	
10 Ω resistor, 1/10 W, 1%	1	ERJ-6ENF10R0V	Panasonic	R3	
0 Ω resistor, 1/10 W, 5%	16	9C06031A0R00JLHFT	Yageo	R6, R9, R47, R110, R114, R133, R144, R171, R172, R178, R189, R193, R225, R232, R247, R249	R10, R14, R48, R109, R124, R145, R181, R182, R200-R202, R222-R224, R228, R229, R245, R250
1 kΩ resistor, 1/16 W, 1%	3	ERJ-3EKF1001V	Panasonic	R1, R4, R226	R7, R44
2 kΩ resistor, 1/16 W, 1%	1	ERJ-3EKF2001V	Panasonic	R227	
3.92 kΩ resistor, 1/16 W, 1%	1	ERJ-3EKF3R92V	Panasonic	R135	
4.75 kΩ resistor, 1/16 W, 1%	2	ERJ-3EKF4751V	Panasonic	R125, R141	
10 kΩ resistor, 1/16 W, 1%	9	ERJ-3EKF1002V	Panasonic	R115, R116, R149, R151, R195, R196, R199, R218, R248	
20 kΩ resistor, 1/16 W, 1%	1	ERJ-3EKF2002V	Panasonic	R136	
100 kΩ resistor, 1/16 W, 1%	6	ERJ-3EKF1003V	Panasonic	R30, R31, R32, R113, R130, R131	
15 Ω resistor, 1/16 W, 1%	4	ERJ-3EKF15R0V	Panasonic	R187, R188, R190, R191	
18.2 Ω resistor, 1/16 W, 1%	1	ERJ-3EKF18R2V	Panasonic	R122	
22.1 Ω resistor, 1/16 W, 1%	4	ERJ-3EKF22R1V	Panasonic	R16, R18, R197, R237	
5.62 Ω resistor, 1/10 W, 1%	3	RC0603FR-075R62L	Yageo	R137, R138, R148	
49.9 Ω resistor, 1/16 W, 1%	9	ERJ-3EKF49R9V	Panasonic	R13, R39, R40, R43, R46, R238, R239, R243, R244	R12
82.5 Ω resistor, 1/16 W, 1%	6	ERJ-3EKF82R5V	Panasonic	R126, R127, R161, R162, R163, R164	
100 Ω resistor, 1/16 W, 1%	10	ERJ-3EKF1000V	Panasonic	R19, R20, R21, R22, R27, R28, R29, R45, R140, R150	R2, R5, R179, R183, R212, R213
110 Ω resistor, 1/16 W, 1%	0	ERJ-3EKF1100V	Panasonic		R235
130 Ω resistor, 1/16 W, 1%	6	ERJ-3EKF1300V	Panasonic	R19, R20, R21, R22, R27, R28, R29, R45, R140, R150	
150 Ω resistor, 1/16 W, 1%	2	ERJ-3EKF1500V	Panasonic	R15, R221	R33, R38

Table 7. Bill of Materials (continued)

Value	QTY	Part Number	Vendor	Ref Des	Not Installed
162 Ω resistor, 1/16 W, 1%	1	ERJ-3EKF1620V	Panasonic	R142	
200 Ω resistor, 1/16 W, 1%	2	ERJ-3EKF2000V	Panasonic	R132, R134	
221 Ω resistor, 1/16 W, 1%	4	ERJ-3EKF2210V	Panasonic	R208-R211	R236
274 Ω resistor, 1/16 W, 1%	2	ERJ-3EKF2740V	Panasonic	R119, R121	
27.4 Ω resistor, 1/16 W, 1%	1	ERJ-3EKF27R4V	Panasonic	R139	
475 Ω resistor, 1/16 W, 1%	1	ERJ-3EKF4750V	Panasonic	R117	R118, R123
750 Ω resistor, 1/16 W, 1%	3	ERJ-3EKF7500V	Panasonic	R23, R24, R26	
825 Ω resistor, 1/16 W, 1%	2	ERJ-3EKF8250V	Panasonic	R111, R112	
93.1 Ω resistor, 1/16 W, 1%	1	ERJ-3EKF93R1V	Panasonic	R25	
15.8 Ω resistor, 1/16 W, 1%	1	ERJ-3EKF1582V	Panasonic	R41	
30.1 Ω resistor, 1/16 W, 1%	1	ERJ-3EKF3012	Panasonic	R42	
10 Ω resistor, 1/16 W, 1%	1	ERJ-2RKF10R0X	Panasonic	R255	
Surface Mount Socket strips	4	310-93-164-41-105000	Mill-Max	RP5- RP8	
51 Ω resistor pack	0		CTS		RP5-RP8
22 Ω resistor pack	4	4816P-001-220	Bourns	RP1, RP2, RP3, RP4	
INDUCTORS					
Ferrite Bead	11	EXC-ML32A680U	Panasonic	FB1, FB3, FB6, FB,7 FB10, FB11, FB14-FB18	
	5	EXC-ML20A390U	Panasonic	FB2, FB4, FB8, FB9, FB12	
	1	623-2773021447	Mouser	FB13	
Inductor, 18 nH	4	LLQ2012-F18NG	Toko	L9, L11, L13, L14	
Inductor, 2.7 nH	4	LLQ2012-F2N7J	Toko	L10, L12, L15, L16	
0 Ω resistor, 1/8 W, 5%	5	9C08052A0R00JLHFT	Yageo	L2, L4, L7, L8, L17	
2.2 nH Inductor	0	LL2012-FH2N2S	Toko		L19
22 nH Inductor	1	0805CS-220X_B_	Coilcraft	L18	
IC'S ETC.					
DAC5687IPZP	1	DAC5687IPZP	Texas Instruments	U1	
CDCM7005RGZ	1	CDCM7005RGZ	Texas Instruments	U12	
CDCV304PW	1	CDCV304PW	Texas Instruments	U17	
TRF3702IRHC	1	TRF3702IRHC	Texas Instruments	U11	
TRF3750IPW	1	TRF3750IPW	Texas Instruments	U14	
THS4221DBVR	1	THS4221DBVR	Texas Instruments	U18	
TPS76750QPWP	1	TPS76750QPWP	Texas Instruments	U6	
TPS76733QPWP	1	TPS76733QPWP	Texas Instruments	U7	
TPS76701QPWP	1	TPS76701QPWP	Texas Instruments	U8	
SN74HC241DW	1	SN74HC241DW	Texas Instruments	U4	
SN74LV125AD	1	SN74LV125AD	Texas Instruments	U13	
Amplifier DC-5000 MHz	1	SGA-5386	Sirenza	U15	
VCO	1	ROS-2170-7	Mini-Circuits	Y3	
VCXO	1	TC0-2111-491.52	Toyocom	U10	
Crystal Oscillator	1	OSC3B0 at 10 MHz	Vectron	Y2	
4:1 Transformer	2	T4-1-KK81	Mini-Circuits	T1, T2	
Black Test Point	1	5011K	Keystone	TP12	
Red Test Point	4	5000K	Keystone	E1, TP1, TP18, TP19	
CONNECTORS, JUMPERS, ETC.					
SMA Plug W/Stand Off	3	901-144-8RFX	AMP	J4, J5, J19	
SMA connectors	7	16F3627	Newark	J2, J3, J6-J10	
Switch	1	EVQ-PJX04M	Panasonic	S1	
Red Banana Jack	1	ST-351A	Allied	J11	

Table 7. Bill of Materials (continued)

Value	QTY	Part Number	Vendor	Ref Des	Not Installed
Black Banana Jack	1	ST-351B	Allied	J17	
Green SM_LED_1206	4	CMD15-21VGC/TR8	Panasonic	D1, D2, D3, D4	
30 Pin Header	1	HTSW-120-07-L-T	Samtec	J15	
34 Pin Header	2	TSM-117-01-S-DV-LC	Samtec	J13, J14	
Connectors	1	745536-2	AMP	J1	
Nuts	2			J1	
Mounting screws	2			J1	
Unformed Fence 0.13 in with 0.5 in spacing no standoff	2	14R-CBSU-24	Leader-Tech	N/Q	
3POS power jack	1	RAPC722	Switchcraft	J12	
3POS_header	2	HTSW-150-07-L-S	Samtec	W2, W5	
2POS_header	2	HTSW-150-07-L-S	Samtec	W1, W6	
MECHANICAL ASSEMBLY AND REWORKS					
Fence cover	1		Leader-Tech		
	1				
Screws	6				
Stand Off Hex (1/4 x 0.5")	6	1902CK-ND	Allied		
Jumper	1			W1	
	1			W2 - Connect pins 1 and 2	
	1			W5 - Connect pins 1 and 2	
	1			W6 - Placed	
	1			J15 - Conn. pin 7 and 8 (ExtLO)	
	1			J15 - Conn. pin 1 and 2 (PLL_VDD)	
	1			J15 - Conn. pin 11 and 12 (TXEnable)	
	1			J15 - Conn. pin 23 and 24 (REF_SEL)	
	1			J15 - Conn. pin 26 and 27 (PLL_PWD)	

11.2 Layers

The Demo Kit is constructed on a 6-layer, 6.2 inch x 8 inch, 0.062-inch thick PCB using FR-4 material. See Figure 13 through Figure 22 show the PCB layout for the Demo Kit.

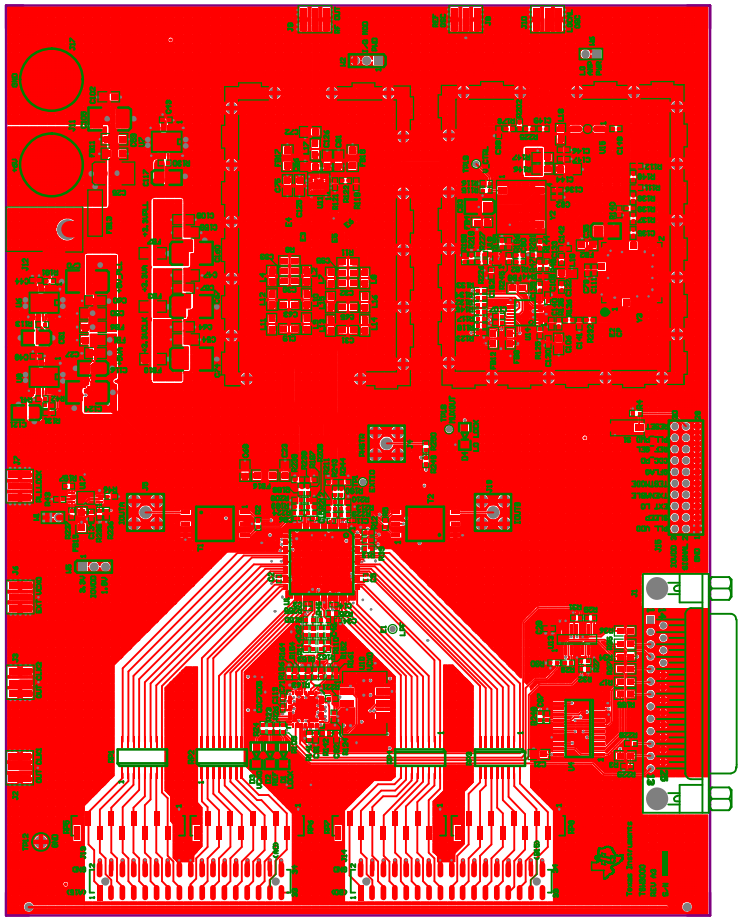

Figure 13. Top Layer

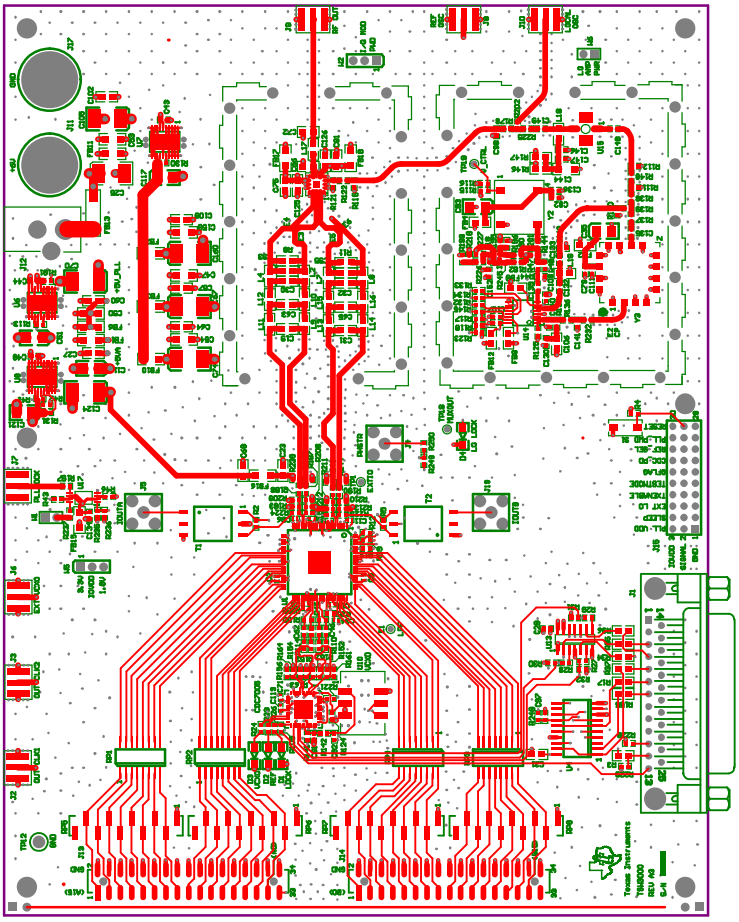

Figure 14. Top Layer (NH)

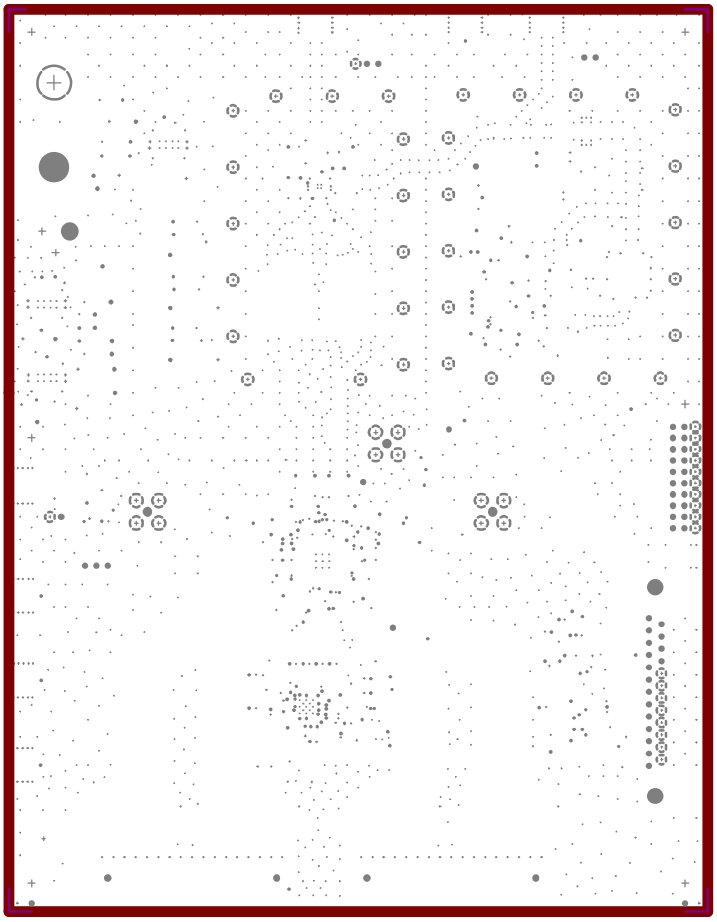

Figure 15. Layer 2

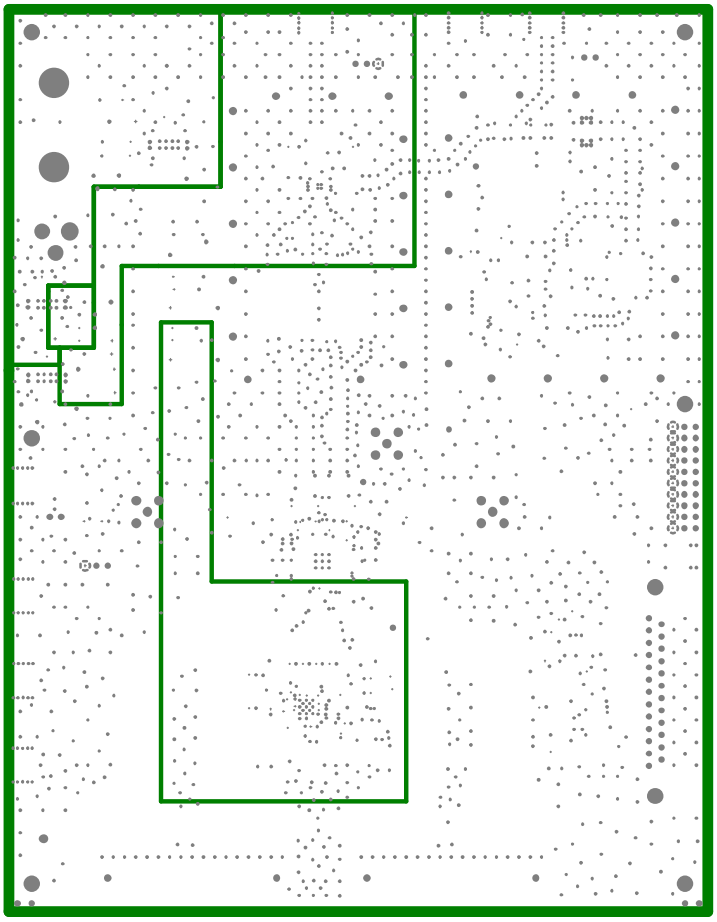

Figure 16. Layer 3

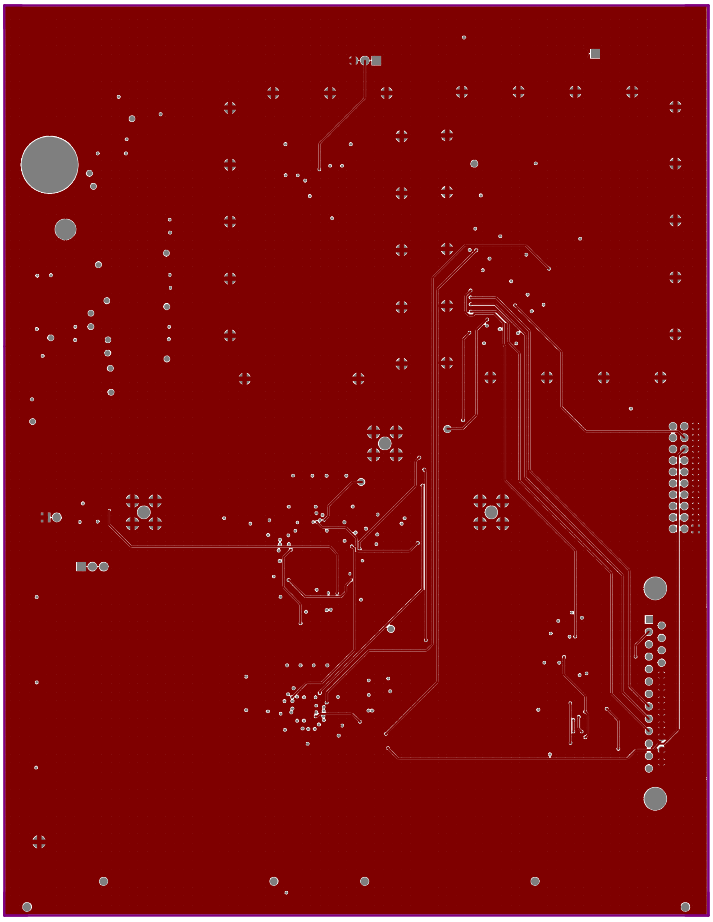

Figure 17. Layer 4

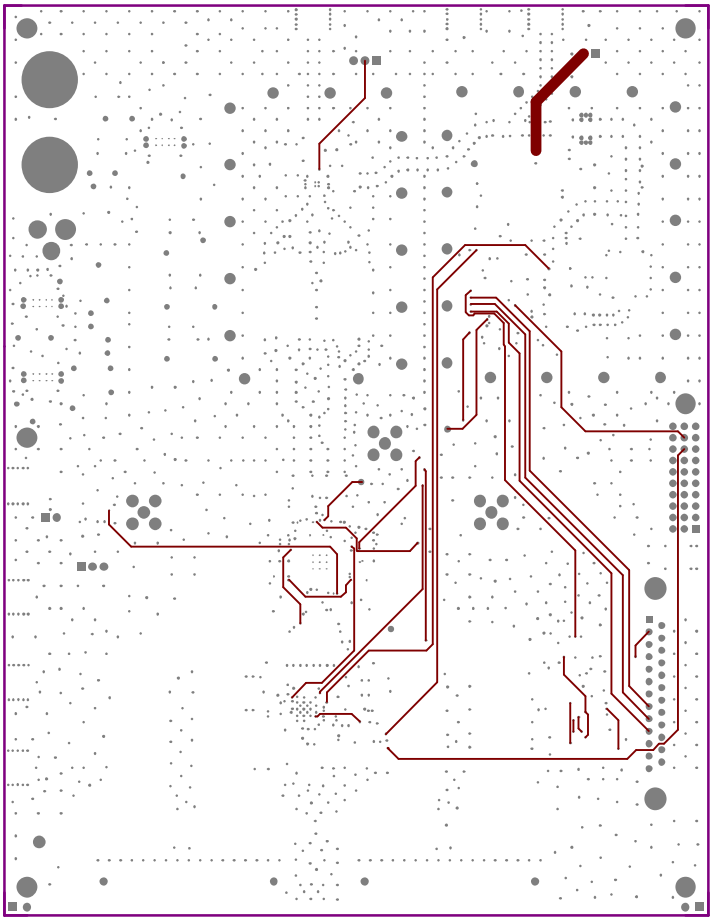

Figure 18. Layer 4 (NH)

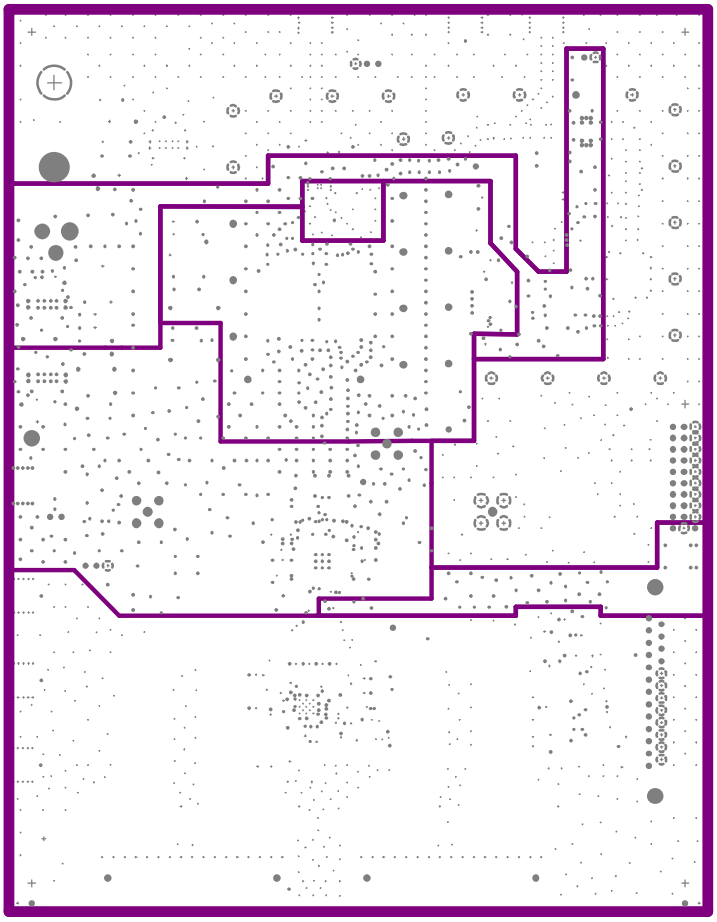

Figure 19. Layer 5

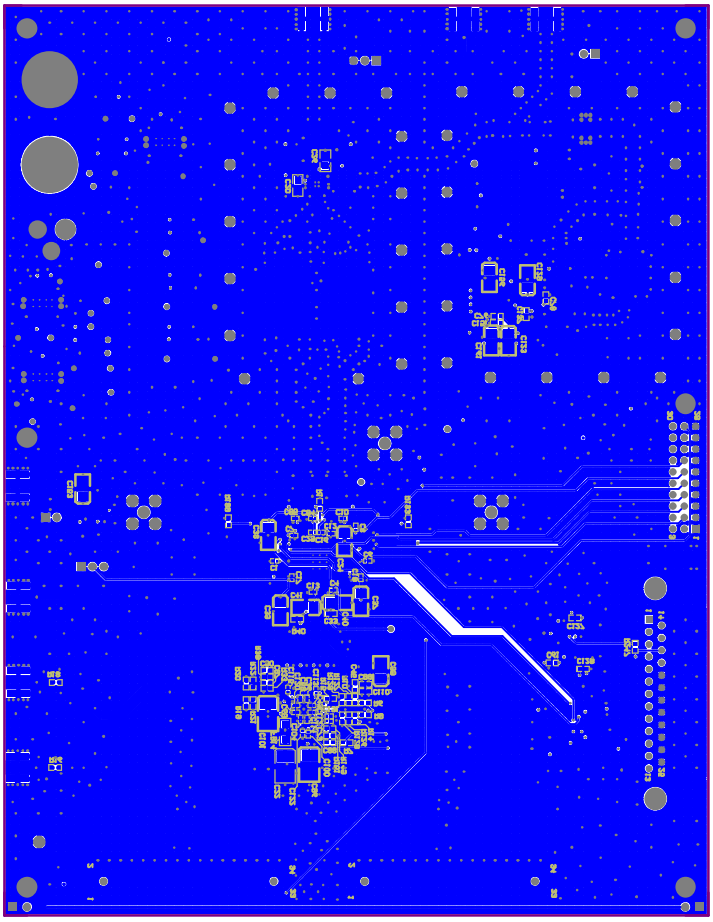

Figure 20. Bottom Layer

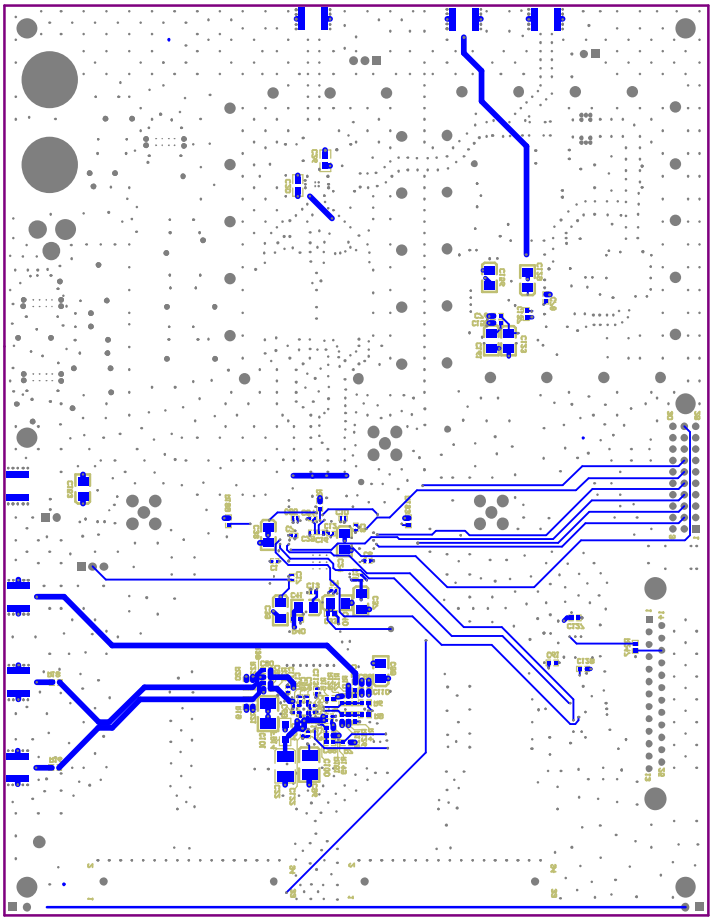

Figure 21. Bottom Silkscreen

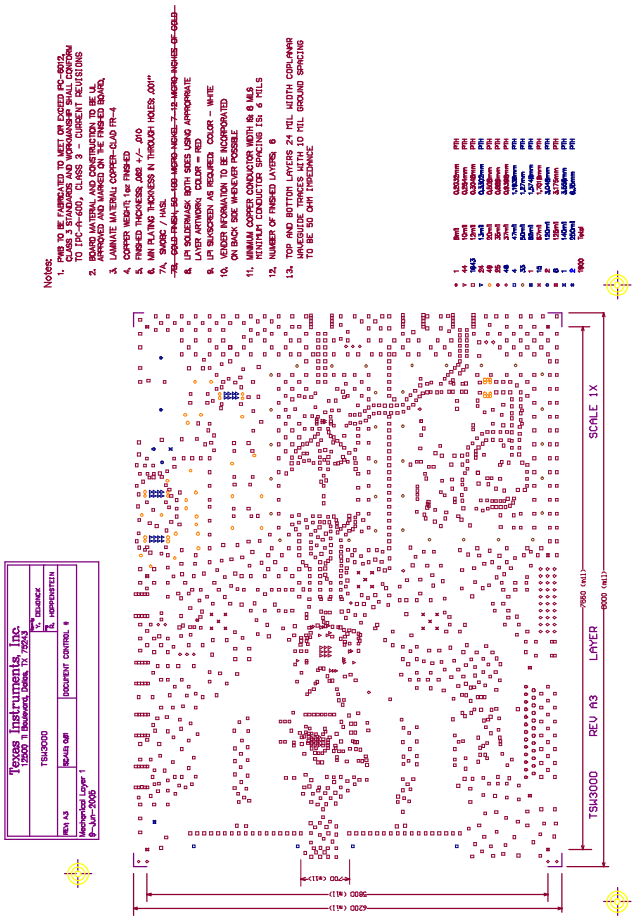

Figure 22. Drill Drawing

11.3 Schematics

The following figures show the schematic for the TSW3000 Demo Kit.

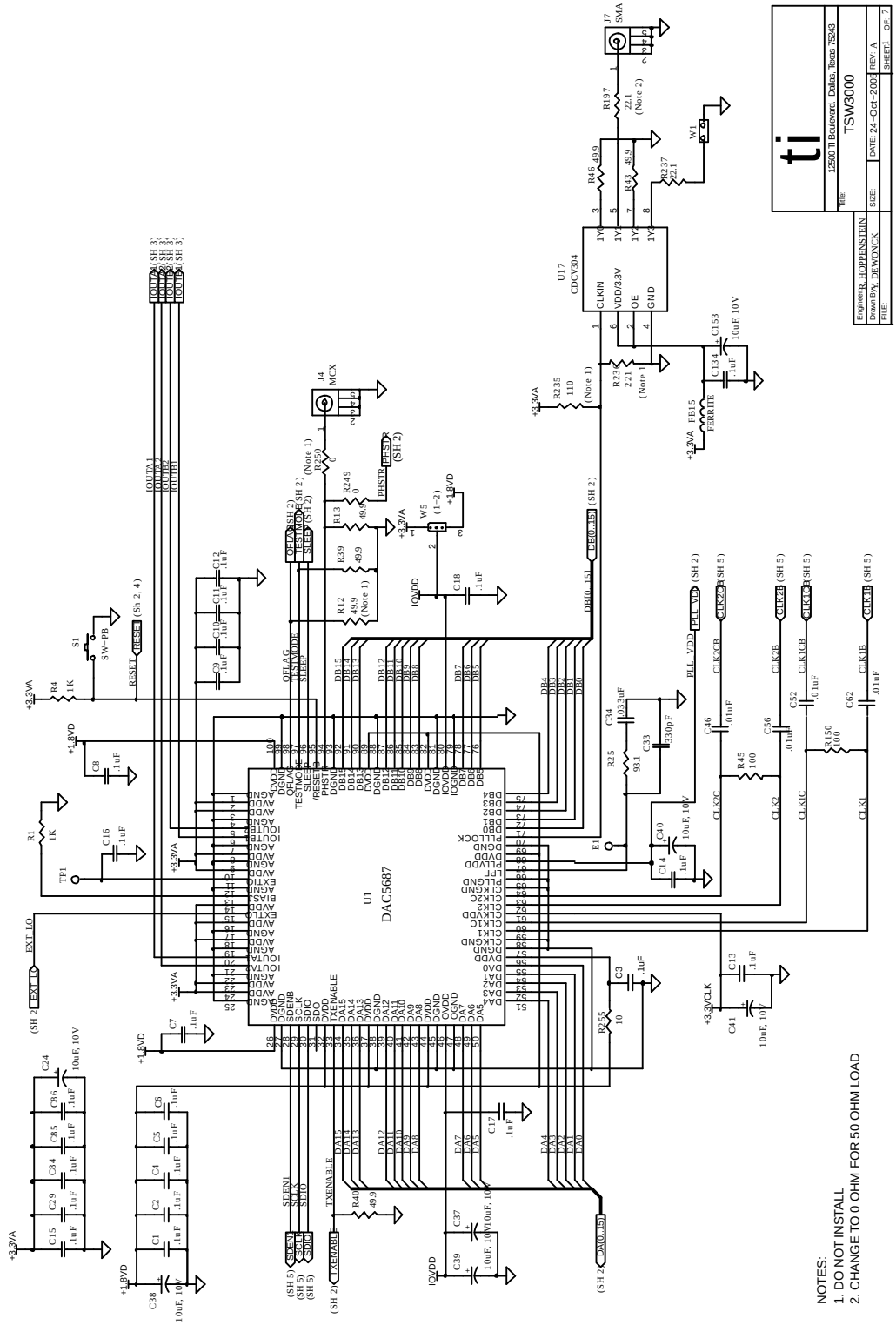

Figure 23. Schematic - Page 1

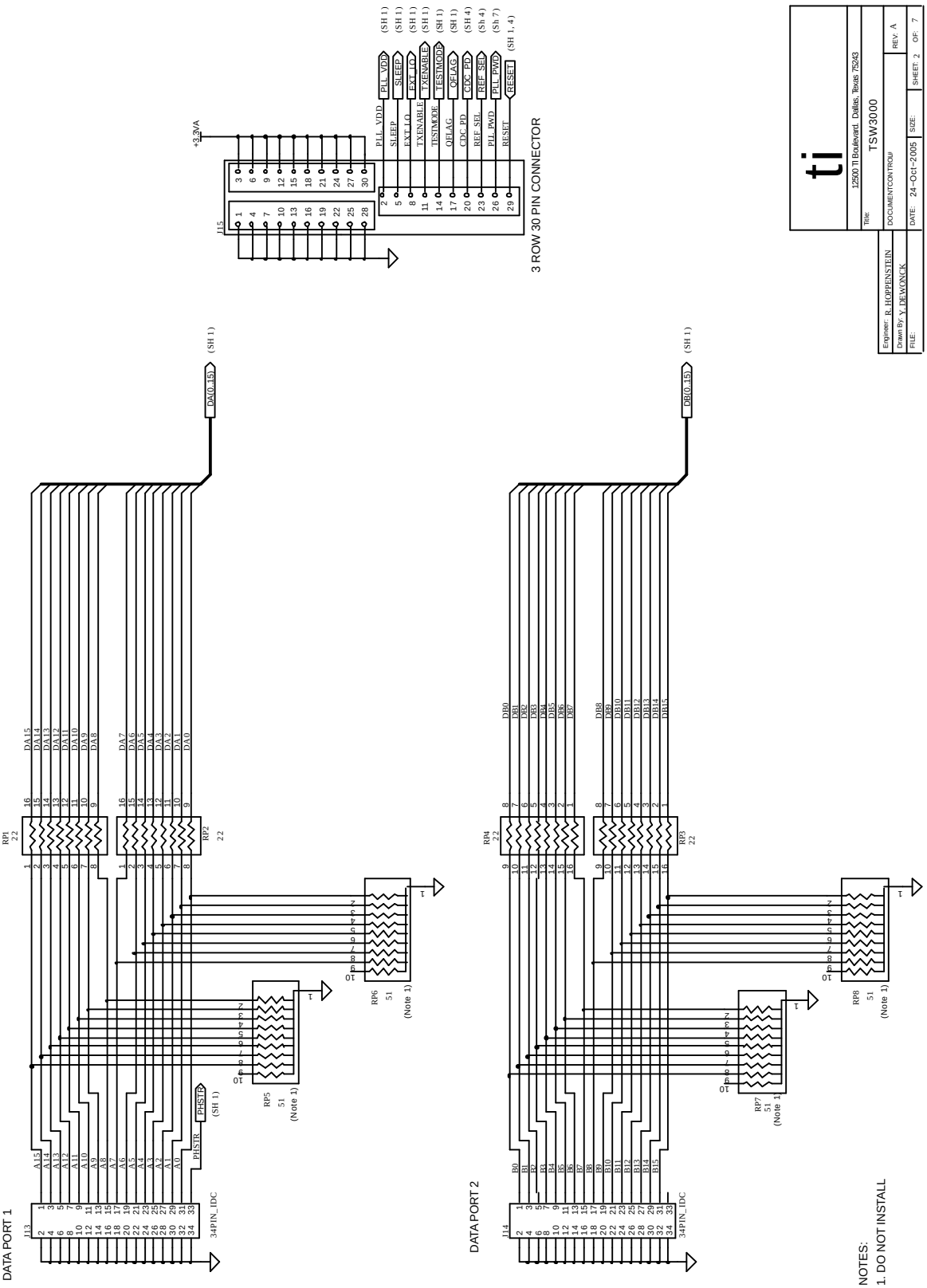

Figure 24. Schematic - Page 2

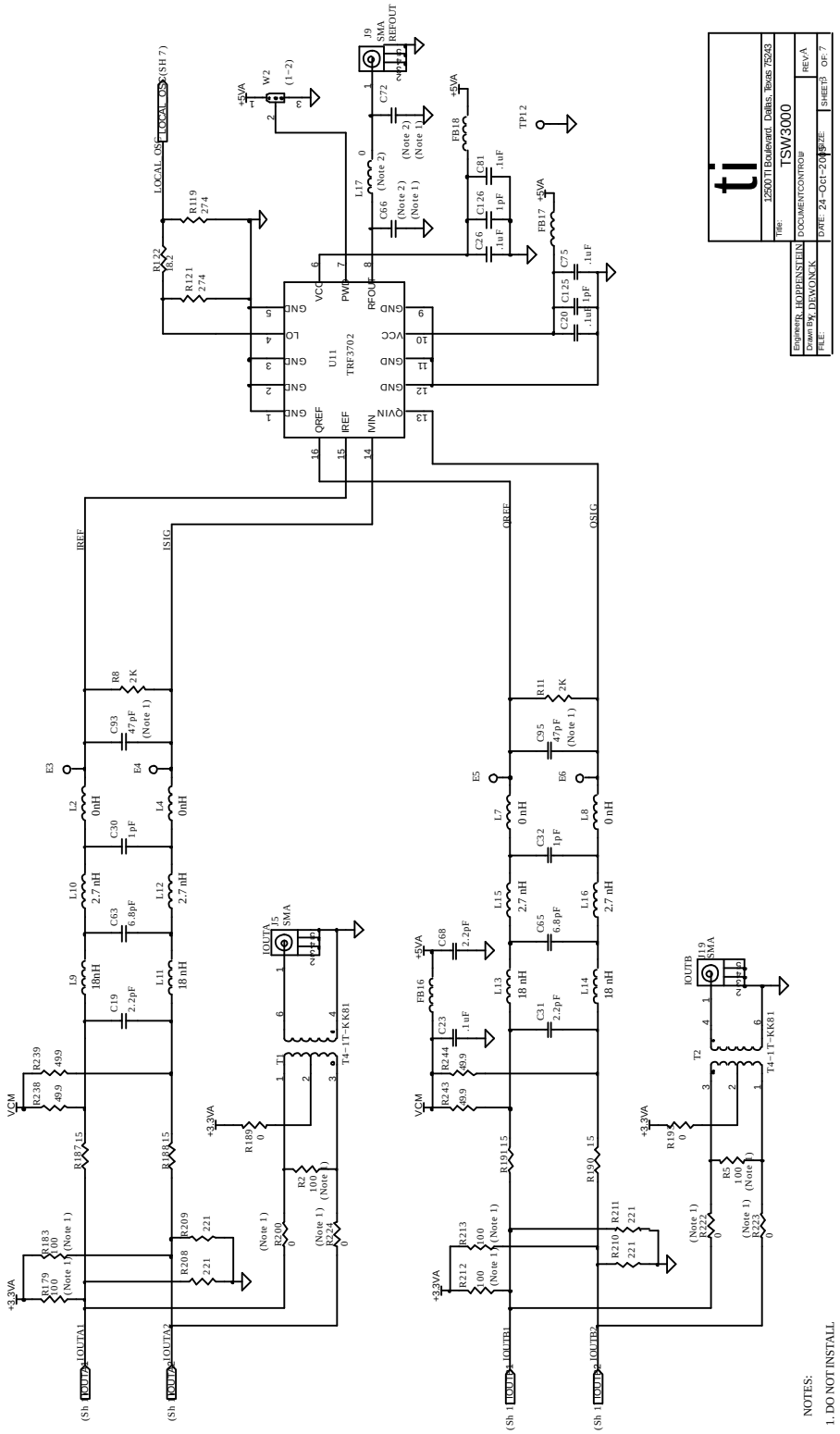

Figure 25. Schematic - Page 3

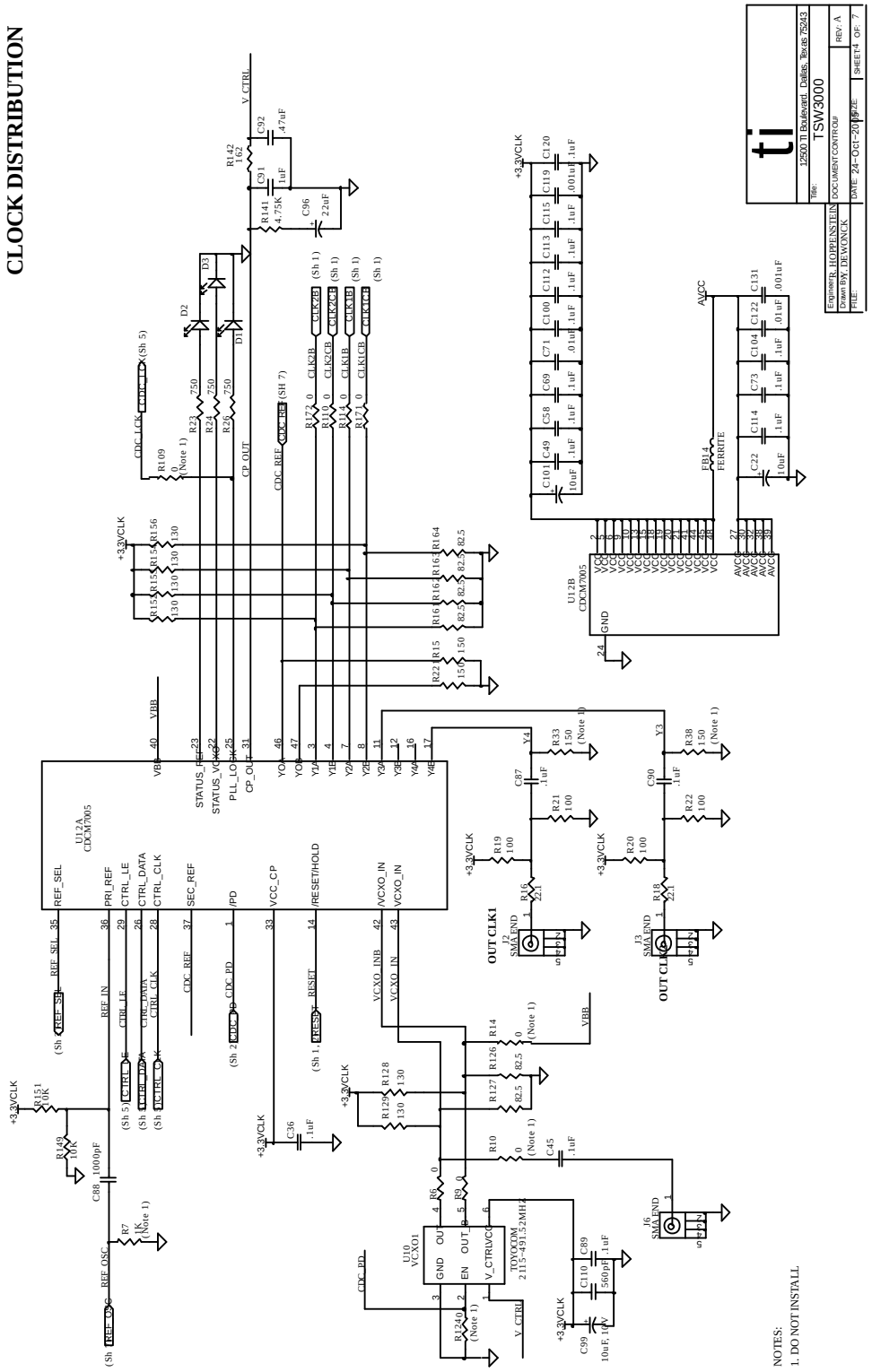

Figure 26. Schematic - Page 4

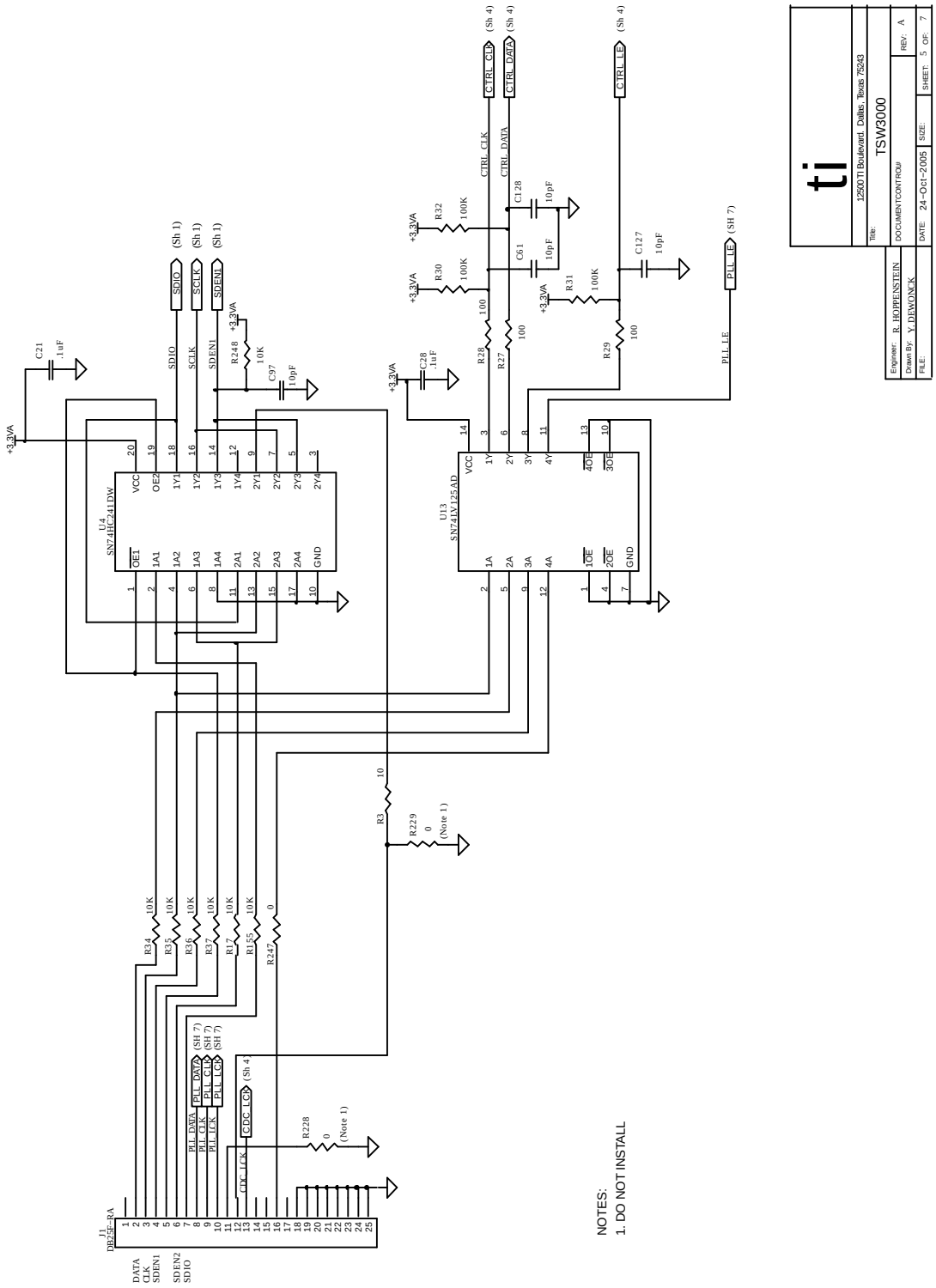

Figure 27. Schematic - Page 5

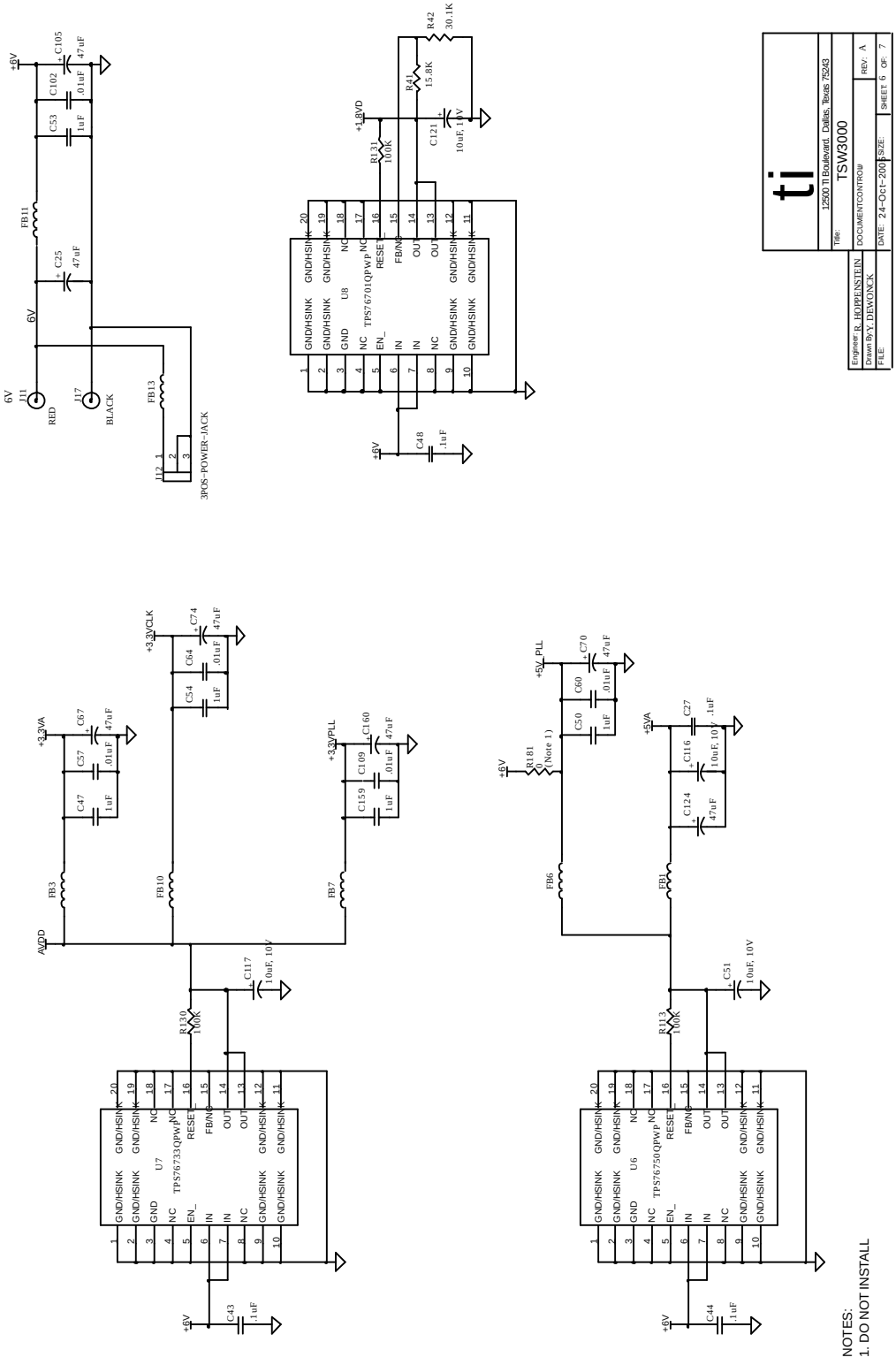

Figure 28. Schematic - Page 6

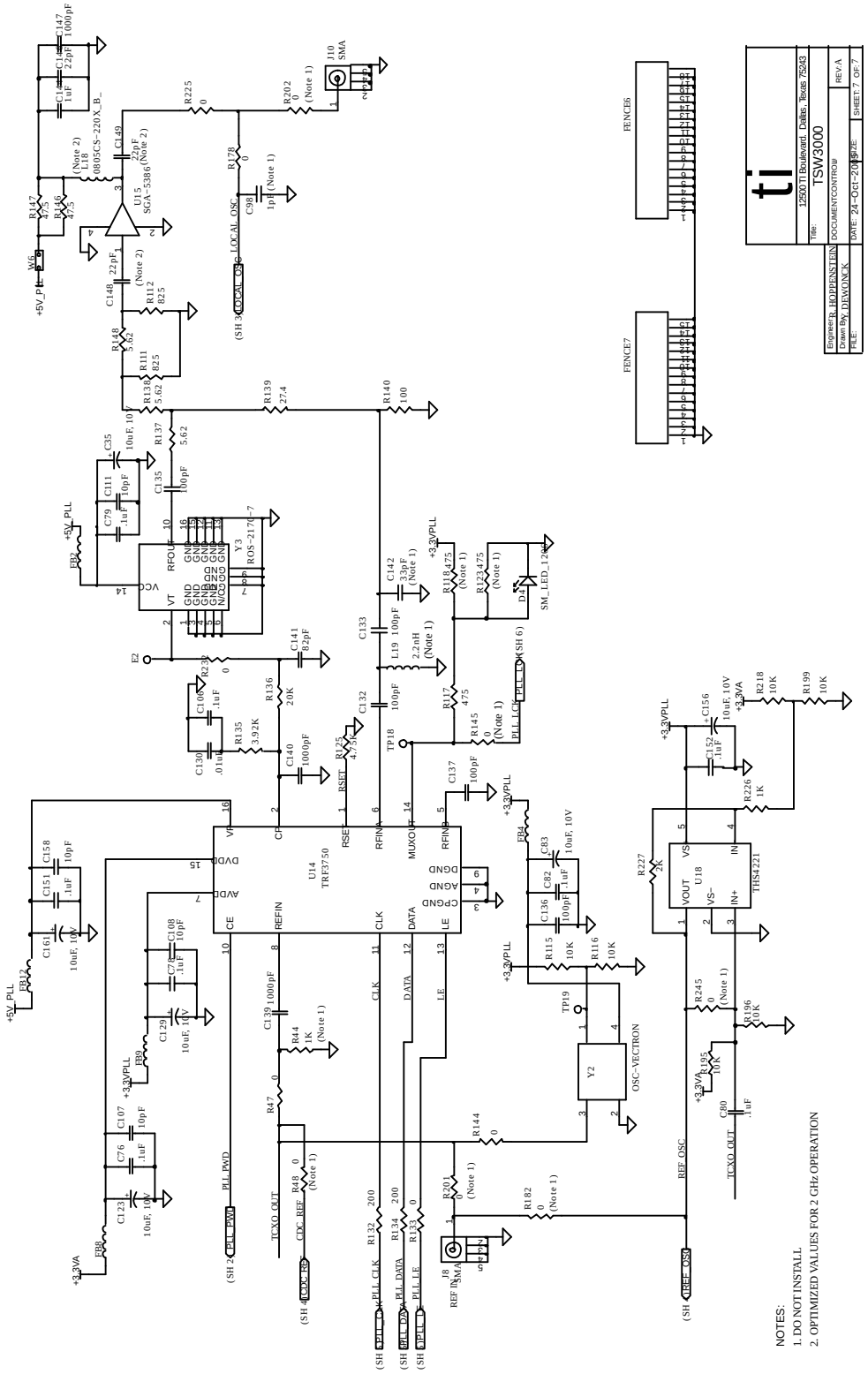

Figure 29. Schematic - Page 7

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