Application Report
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DC Offset Auto-Calibration of TRF371x

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ABSTRACT

The TRF371x family provides an automatic calibration circuit to minimize the DC offset imbalance in the baseband outputs. This eliminates the dc signal at the ADC output which eats into the valuable dynamic range of the ADC device. This report breaks down the operation of the dc offset calibration and provides the recommended register settings for optimum performance. The convergence time of the calibration is presented along with the trade-offs between faster convergence time and accuracy. In addition, guidelines for when to recalibrate are provided.

Introduction

In a direct-conversion receiver, one of the limiting performance parameters is the dc suppression provided by the quadrature demodulator. This parameter is analogous to the carrier feedthrough performance of the quadrature modulator in the transmitter. With the quadrature modulator, dc imbalances on the input in-phase (I) and quadrature-phase (Q) baseband paths result in a carrier component on the output. Similarly, dc offset imbalance on the I and Q paths of the demodulator results in a dc component (i.e., 0 Hz) at the output. There is no information contained in this component. If left untreated, the dc level consumes valuable dynamic range of the analog-to-digital converter (ADC).

One option for removing the dc offset is to ac-couple to the input of the ADC. This eliminates the dc component to the ADC but introduces a couple of unwanted side effects. One, the coupling capacitor in conjunction with the load impedance of the ADC creates a high-frequency corner which not only blocks the dc component, but also blocks low frequencies that are part of the desired signal. Conceivably, the capacitor values could be kept large, on the order of 1 to 10 µF, to bring the high-pass corner below 10 kHz, where little to none of the desired signal resides; however, high-value capacitors lead to longer transient effects. In a TDD system where the signal is constantly turning on and off, the delay introduced by the filter can be an obstacle.

An alternative option is to balance the dc offset levels at the output I and Q paths. This maintains the dc path to the ADC and does not introduce the capacitor and the high-frequency corner or its associated delay. The TRF371x direct-conversion receiver employs an automatic dc offset calibration, initiated via serial programming interface (SPI) commands that typically balance the dc offset within 10 mV. This technique provides a lot of flexibility to pass a variety of modulation schemes and standards.

DC Offset Resolution

The automatic dc offset correction in the TRF371x direct-conversion receiver employs an 8-bit DAC register to adjust dc offset at the I and Q channels independently. The 8-bit DAC provides 256 individual steps of adjustment capability. The resolution of each DAC step is adjustable via SPI commands on the *IDet* register. This allows for either finer resolution or greater range, depending on the application. Table 1 shows the approximate DAC-voltage step size for each of the resolution settings when the device is at maximum gain. This step size varies slightly between units.

Table 1. DC Offset Resolution

RESOLUTION SETTING	APPROXIMATE STEP [mV]
50 µA	3.5
100 µA	6.5
150 µA	10
200 µA	13

In nominal conditions, the inherent dc balance of the mixer and baseband section is usually good, so there is not a need for a significant amount of range. Further, it is desirable to minimize the dc component. To accomplish this, the smallest resolution setting of 50 µA is recommended. Ideally, this should translate to less than 2 mV of error, but in practice, the error with this resolution is less than 10 mV under nominal conditions.

It is possible that the smallest resolution does not adequately converge to the optimum point. A convenient way to monitor this situation is if the dc offset DACs are railed high (255) or low (1). This can be monitored by the Readback feature of the TRF371x device. Assuming the LO power is injected, if the device rails, then the resolution can be incremented one step and the dc offset recalibrated.

How It Works

Each I/Q path is differential and has a set common-mode voltage. Generally, this voltage is provided by the ADC device to the Vcm pin of the TRF371x and is usually 1.5 V. The goal is to maintain all four outputs (I and Q differential paths) at the same exact common-mode voltage. Variations from the ideal common-mode voltage translate to a dc component at the ADC output. For each path, the goal is to keep the differential dc voltage between I/Q-positive and I/Q-negative equal to zero. The difference voltage is the residual voltage difference between I/Q positive and negative ports.

$V_D = V^+ – V^–$

The auto-calibration uses a binary search algorithm to determine the optimum correction setting. Initially, the DAC registers are set at midscale. The dc offset for each branch is monitored and a difference voltage is generated. Ideally, the difference voltage should be zero, but small imbalances in the mixers and baseband circuitry skew the output such that the difference voltage is either positive or negative. The sign of the difference voltage determines which half of the range to use. The algorithm continues to narrow down the range by half until there are no more steps. For the 256 steps, this process takes 8 iterations. The flow chart in Figure 1 illustrates the process of calibration.

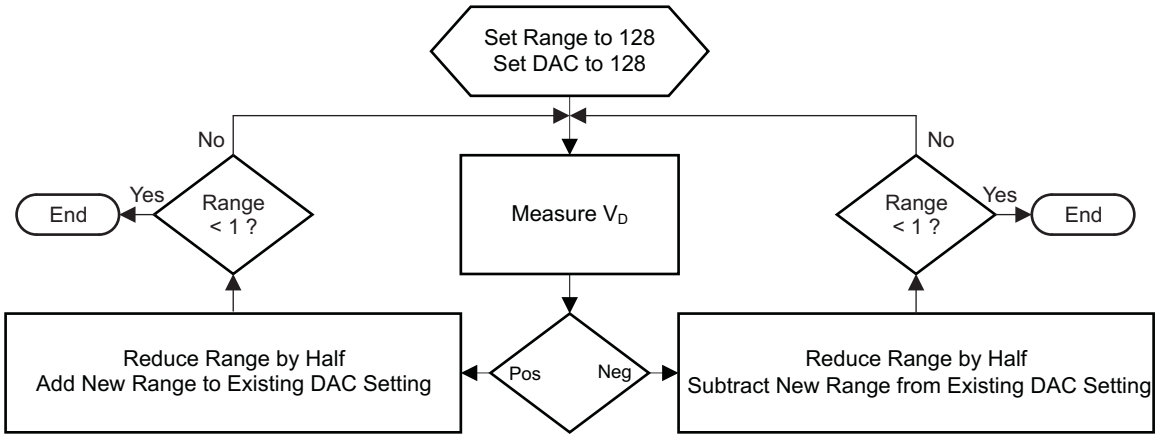

Figure 1. DC Offset Correction Flowchart

The following example of a sample device is shown to further illustrate the process. Initially, the DAC is set to mid scale, 128, and the differential voltage is measured.

Iteration 1: DAC setting: 128 V_D = 21 mV

Because the voltage is positive, the algorithm reduces the range in half to 64 and adds it to the previous DAC setting.

Iteration 2: DAC setting: 192 V_D = –194 mV

Now the difference voltage is negative so the range is halved again to 32 and subtracted from the current setting

Iteration 3: DAC setting: 160 V_D = –84 mV

The difference voltage is still negative, so continue with the same process of dividing the range by two and subtracting from the existing DAC setting.

Iteration 4: DAC setting: 144 V_D = –30 mV
Iteration 5: DAC setting: 136 V_D = –3 mV
Iteration 6: DAC setting: 132 V_D = 11 mV

Now the difference voltage is positive, so the range is again reduced in half and now added to the existing DAC setting.

Iteration 7: DAC setting: 134 V_D = 4 mV
Iteration 8: DAC setting: 135 V_D = 1 mV

The device converged to about 1 mV. Notice that in the last four iterations, the dc offset performance is around 10 mV or better, as the algorithm focuses in on the optimum setting.

DC Offset Calibration Variables

There are three main variables used in the auto-calibration process that affect the convergence time and accuracy of the algorithm: the clock frequency, the clock divider, and the detector filter. The algorithm requires a clock to regulate the binary search process. The TRF371x device is able to use an internal oscillator for this clock or use an externally supplied clock fed to the SPI clock pin. The internal oscillator frequency can be changed from nominally 300 kHz to 1.8 MHz. Note this oscillator frequency is not tightly controlled. The actual frequency of operation may shift ±35% due to process variations. The internal clock oscillator can be monitored on the READBACK pin by toggling the *Osc_Test* switch on the TRF371x GUI. Alternatively, an external clock can be provided through the SPI clock pin. The speed of this clock can be increased up to the limit of the SPI interface circuitry, which is about 20 MHz.

The detection filter is used to filter the signal and noise from impacting the dc detection operational-amplifier circuitry. For the accuracy of the detector, the more filtering the better; however, with increased filtering, more averaging is required to get usable results. The clock divider setting is used to provide additional averaging time for the detector. The clock divider must be increased as the detector bandwidth is reduced. It is desirable to use the minimum detector bandwidth of 1 kHz. This allows the auto dc offset calibration to take place with the RF signal applied and minimizes wide-bandwidth noise. With this detection filter setting, the dc offset calibration can be completed on-the-fly whenever external conditions, like a temperature change, warrant.

The recommended setting for optimum results is to use the detection filter at its lowest setting: 1 kHz. The clock divider should be set at 1024. The clock frequency can be chosen to be the fastest setting to minimize the convergence time.

DC Offset Calibration Convergence Time

The dc offset convergence time is dependent on the oscillator frequency and the clock divider setting. The time duration of a cycle in the process is defined by:

$$\tau_{Cycle} = \frac{Clk\_Divider}{Osc\_Frequency}$$

Note the oscillator frequency in the preceding equation reflects the exact, measured oscillator frequency and not necessarily the nominal setting as shown in the data sheet.

The anatomy of the calibration with respect to time is shown in Figure 2. For illustration purposes, the step size was set at its coarsest resolution (200 µA) and the DAC registers were initially set away from midscale in a non-optimized location. This shows the steps in the calibration routine more clearly.

Section A last for about 1 cycle. No activity occurs in this section. The delay allows time for the internal oscillator to start up and run smoothly. In section B, the DAC registers are set to midscale. This section lasts for about 4 cycles. The delay allows time for the dc offset circuitry to power up and become stable before the algorithm begins. Section C employs the aforementioned binary search algorithm. This section lasts for 8 cycles. Due to the coarse resolution, seven of the eight cycles in the binary search can be seen.

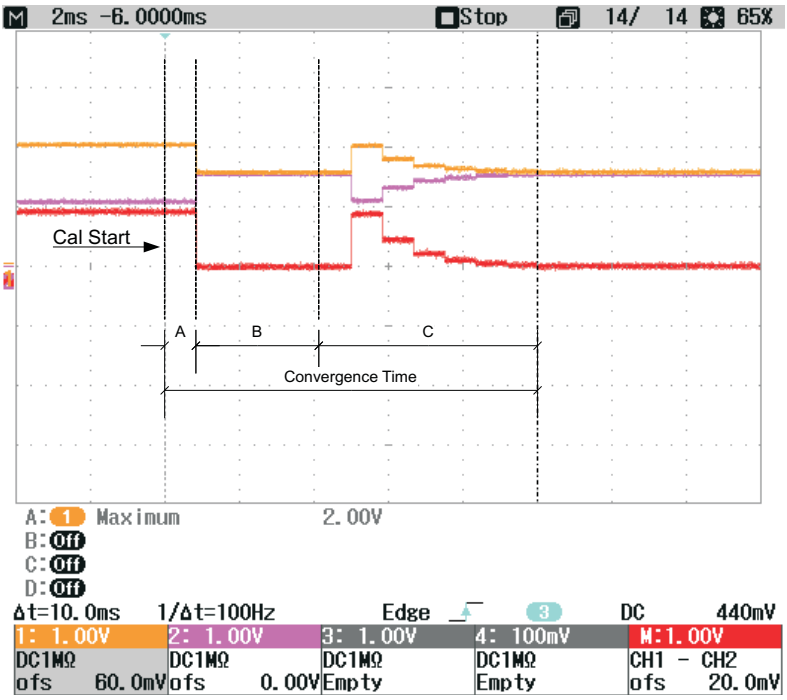

Figure 2. Anatomy of the DC Offset Calibration Over Time (Exaggerated)

Technically, the entire convergence time takes about 13 cycles. As seen previously, the last four cycles of the binary search represent a small change in the output performance. For practical considerations, these last few cycles can be neglected, and the total convergence time can be estimated by nine cycles.

$$\tau_{Convergence} = 9 \times \tau_{Cycle} = \frac{9 \times Clk\_Divider}{Osc\_Frequency}$$

A more realistic case is shown in Figure 3. In this setup, the clock oscillator is nominally set to 900 kHz. The detector bandwidth is 1 kHz, and the clock divider is set to 1024. The resolution is set to 50 µA. Once the auto-calibration is engaged, the algorithm converges in less than 10 ms. Further, notice that because the device is starting at a nearly optimized value which is near midscale and the resolution is small, the brief shift away from optimization during the calibration process is small, and it quickly converges back to the optimized state.

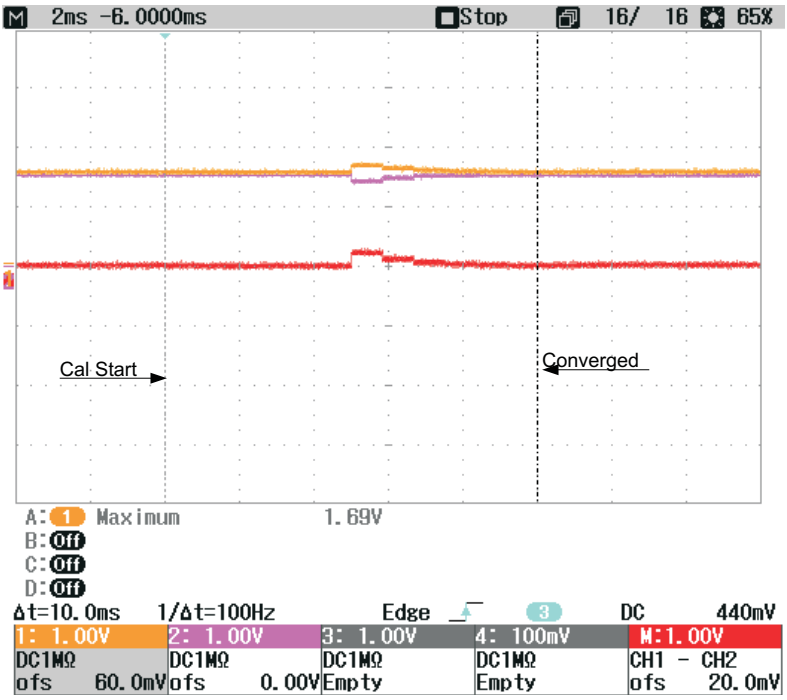

Figure 3. Realistic Auto-Cal Performance Over Time

Optimizing Convergence Time

In practical applications, the convergence time may need to fit within a certain time window to facilitate calibration during normally off states of the receiver, as in a TDD system. As such, the luxury of maintaining a high average time set by the clock divider may not be possible.

In the recommended configuration the detector bandwidth is set to 1 kHz and the clock divider is set to 1024. The clock oscillator can be set to its maximum value of 1.8 MHz; however, the actual frequency is not certain to be this value. Assuming a worst-case 35% process variation, the minimum oscillator frequency at the highest internal setting is 1.17 MHz. With this situation, the convergence time is estimated at:

$$\tau_{Convergence} = \frac{9 \times 1024}{1.17\ MHz} = 7.9\ ms \quad (1)$$

If this convergence time is deemed too long, the settings can be adjusted to reduce the time. The internal clock could be substituted with a faster external clock. This would give the user flexibility on the convergence time and not be subjected to the process variations of the internal oscillator. Alternatively, moving to the next-lower clock divider value, 256, reduces the convergence time four-fold. In the example above, the convergence time would be reduced to just under 2 ms. Though the convergence time is reduced, there is more opportunity for error due to the lower averaging time. The settings for the detection bandwidth and clock divider can be adjusted to provide the best trade-off between convergence time and dc offset accuracy. With the recommended settings of 1 kHz detector bandwidth and 1024 clock divider, the DAC step error after calibration is expected to be zero. This roughly corresponds to an actual dc offset error of ±10 mV when the device resolution is at its smallest value and the PGA gain is at maximum. The calibration was conducted with a 5-MHz WiMAX signal at –40 dBm input power at the RF input to simulate a real-world situation. Other combinations of the clock divider and detector BW are shown in Table 2, along with the maximum DAC step error and corresponding maximum dc offset error. Note, these errors are not a given, just an indication of the maximum error that could occur.

Table 2. Max Error from Optimum Set-point

Clock Divider	Detector BW	Maximum Error From Optimized Value	Maximum DC Offset Error (Maximum Gain)
1024	1 kHz	±0 steps	±10 mV
256	1 kHz	±4 steps	±24 mV
128	1 kHz	±6 steps	±31 mV
1024	10 kHz	±0 steps	±10 mV
256	10 kHz	±2 steps	±17 mV
128	10 kHz	±2 steps	±17 mV
16	10 kHz	±6 steps	±31 mV
1024	10 MHz	± 4 steps	±24 mV
256	10 MHz	±4 steps	±24 mV
128	10 MHz	±8 steps	±31 mV
16	10 MHz	±10 steps	±45 mV

From the table, the minimum error corresponds to the 1-kHz detector bandwidth and the 1024 clock divider. The next smallest error corresponds to a 10-kHz detector bandwidth and the 256 clock divider. This setting reduces the convergence time by a factor of four and potentially introduce ±7 mV of additional error.

Figure 4 shows the convergence condition using a 10-kHz detector bandwidth with a 256 clock divider. The internal clock oscillator was measured at just under 1.2 MHz, which is roughly equivalent to the expected worse case frequency when the oscillator is set to 1.8 MHz. The auto-calibration can be shown to converge in less than 2.3 ms as expected.

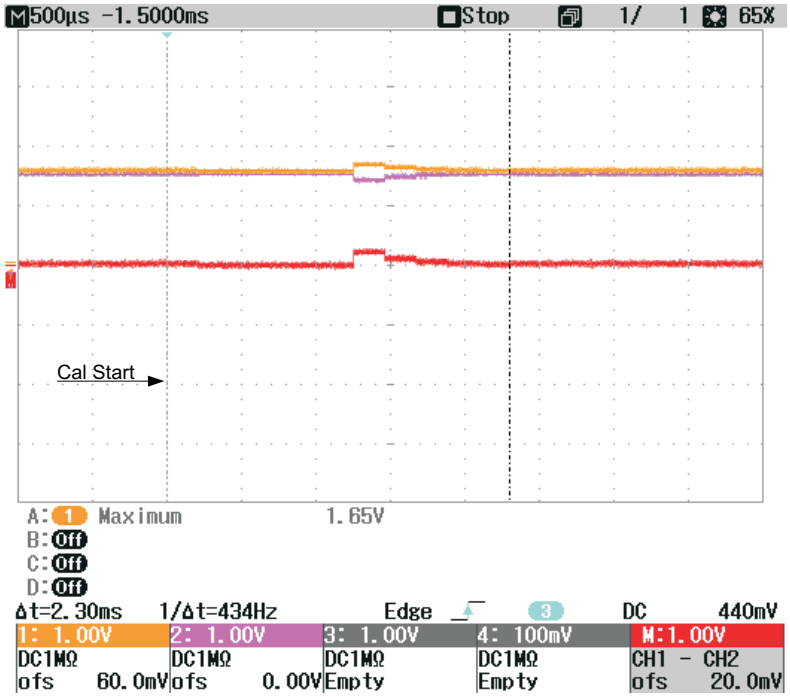

Figure 4. Auto-cal Performance Over Time With Clk_Div = 256

How Often to Recalibrate

The benefit of the auto-calibration on the TRF371x device is that it minimizes the dc offset balance within 10 mV typically, and with the proper setup can be initiated at any time, even with the signal applied. Once calibrated, how often does the device need to be recalibrated? There are a few known environmental or operational conditions that impact the dc offset performance. The system can be designed to trigger a recalibration when these conditions are experienced.

The PGA gain setting impacts the dc offset performance. It is recommended to recalibrate if the PGA gain setting is changed. This is primarily a concern if increasing the PGA gain. If the PGA gain is reduced, the residual dc offset imbalance generally decreases.

Temperature also impacts the dc offset balance performance. Figure 5 shows the dc offset performance of a sample unit that has been calibrated at room temperature and then not modified as the ambient temperature is changed. If not recalibrated, the dc offset imbalance can degrade to over 20 mV at the temperature extremes. It is generally recommended to recalibrate at every 10°C change in temperature, but this can be relaxed depending on the amount of dc offset imbalance that can be tolerated.

The LO frequency impacts the dc offset imbalance performance due to the change in operating conditions of the mixers. Recalibration should occur whenever the LO frequency is modified.

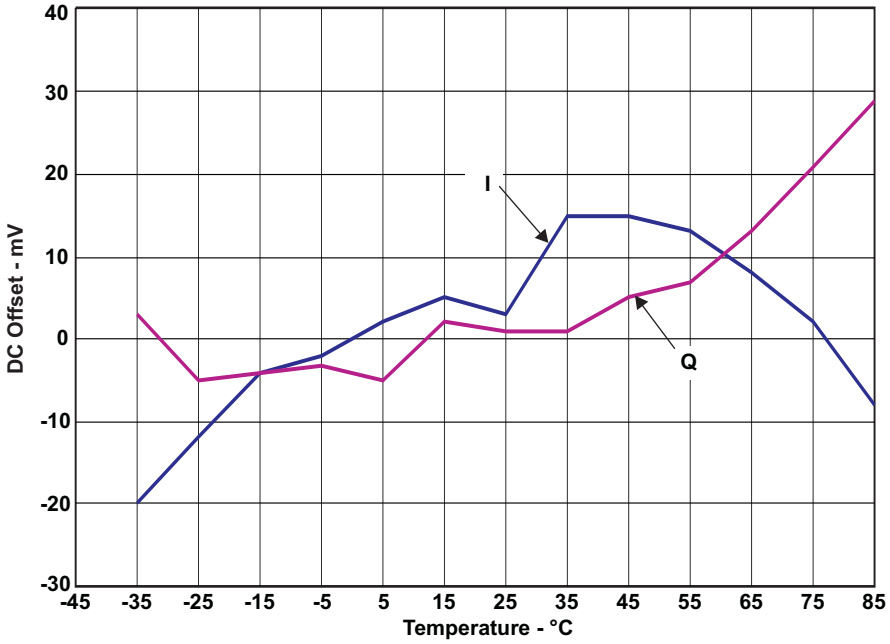

Figure 5. Sample DC Offset Variation Over Temperature

Conclusion

The TRF371x auto dc offset calibration provides a convenient way to minimize the dc offset imbalance in the direct conversion receiver so that the dynamic range of the ADC is not degraded. The optimum settings for the device calibration are to set the IDet resolution to 50 µA, the *Det Filter* to 1 kHz, and the *Clk Div* to 1024. This provides the best performance. If convergence time is a factor, the settings can be adjusted to decrease the convergence time at the expense of accuracy. Once calibrated, it is recommended to recalibrate after either a 10°C change in temperature, a change in LO frequency, or a change in PGA gain setting.

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