EVM User's Guide: TPS65215Q1EVM

TPS65215-Q1 Evaluation Module

Description

The TPS65215Q1EVM is a fully assembled platform for evaluating the performance and functionality of the TPS65215-Q1 power management IC (PMIC). The EVM includes an onboard USB-to-I^{2}C adapter, power terminals, and jumpers for all DC regulator inputs and outputs, as well as test points for common measurements.

Features

- GUI support to read and write to device registers along with being able to view and export register data
- USB2ANY adapter port for I2C communication with host computer
- Optional support for USB-A to Micro-USB connection for I2C communication

TPS65215Q1EVM

1 Evaluation Module Overview

1.1 Introduction

The TPS65215-Q1 EVM is designed for evaluating the TPS65215-Q1 PMIC. The EVM operates with an input voltage range of 2.5V to 5.5V. The evaluation module has a graphical user interface (GUI) used to read and write to device registers and perform non-volatile memory (NVM) programming.

CAUTION

To minimize the risk of damaging LDO1, operate the EVM strictly at 3.3V input voltage when VINLDO1 is set to VSYS and the VSEL jumper is configured as high.

This user's guide describes the characteristics, operation, and use of the TPS65215-Q1 EVM. This document includes a schematic, reference printed circuit board (PCB) layouts, and a complete bill of materials (BOM).

1.2 Kit Contents

- TPS65215Q1EVM Circuit Board
- USB-A to Micro-USB cable

1.3 Specifications

Figure 1-1 shows the functional block diagram of the TPS65215-Q1 PMIC.

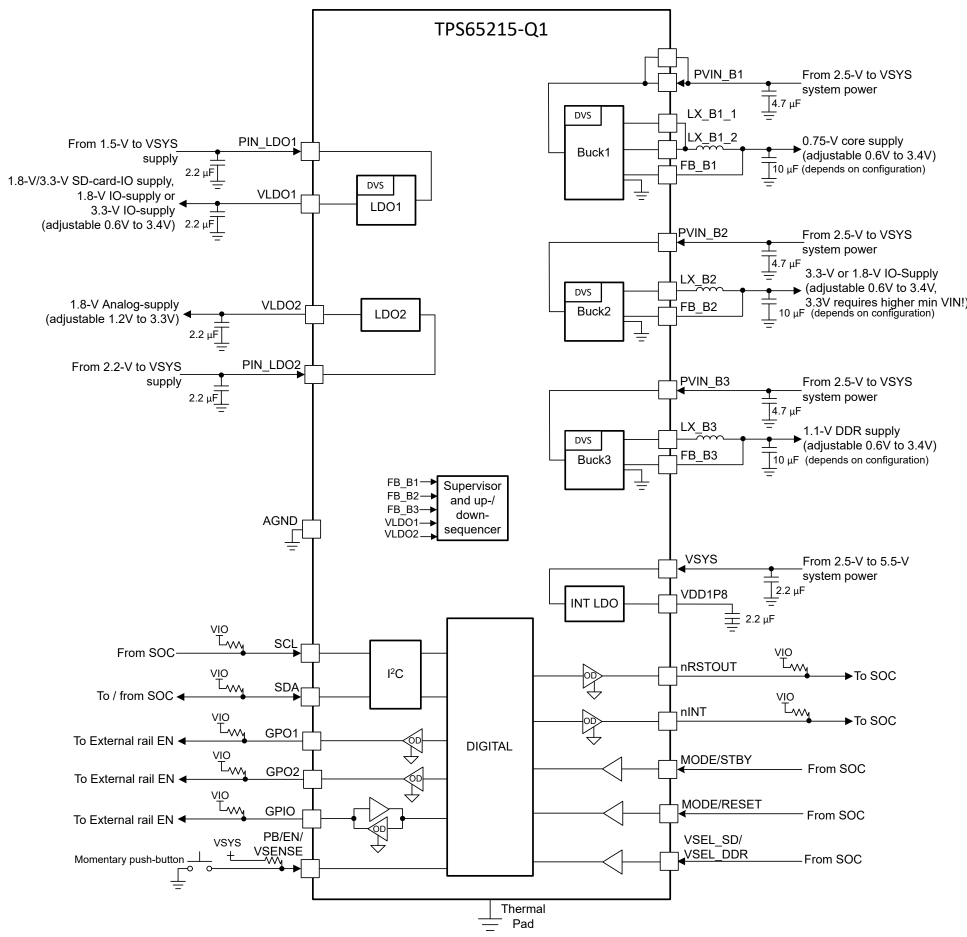

Figure 1-1. TPS65215-Q1 Functional Block Diagram

1.4 Device Information

The TPS65215-Q1 PMIC is a highly integrated power management design for Arm® Cortex®-A53 Processors and FPGAs. This device combines three step down converters and two low-dropout (LDO) regulators. The Buck1 step down converter supports a load current of up to 3.5A, designed for the core rail of a processor. All three step down converters support non-fixed switching frequency or fixed frequency mode. LDO1 is configurable in both load switch and bypass-mode to support SD-Card configuration. All LDO voltage inputs cascade off the system power or the step down converter outputs to enable maximum design and sequencing functionality. Complete with one GPIO, two GPOs, and three Multi-Function-Pins (MFPs), TPS65215-Q1 offers the complete package for full control of the power and sequencing of a System on Chip (SoC).

1.5 Caution

CAUTION

Read the user's guide before use.

CAUTION

Hot surface. Contact can cause burns. Do not touch!

2 Hardware

2.1 Setup

The minimum hardware requirements are needed to operate the EVM:

- EVM
  – The TPS65215-Q1 evaluation board.
- Host computer
  – A computer with an available USB port is required to make use of the EVM software. The EVM software runs on the computer and communicates with the EVM via a USB-A to micro-B cable.
- Power supply
  – An input voltage source capable of supplying 3.3V.

2.2 TPS65215-Q1 Resources Overview

The TPS65215-Q1 PMIC contains five regulators; 3 buck regulators and 2 low drop-out regulators (LDOs). The buck converters are capable of supporting up to 3.5A for buck1, and 1.5A each for the remaining buck regulators. LDO1 (400mA) is configurable as an LDO, load switch, or bypass mode. LDO2 (300mA) is configurable as an LDO or load switch. With a VIN range of 2.5V to 5.5V, the PMIC supports a common 3.3V system voltage. When VSEL jumper is set to high, LDO1 is set to bypass 3.3V input from the system voltage. Set the VSEL jumper low to set LDO1 to a fixed 1.8V LDO. Table 2-1 shows a summary of the voltage and current capabilities for each of the analog resources. With an I^2C interface, three GPIO pins, and three multi-function-pins, the TPS65215-Q1 PMIC provides the full power package to meet the requirements of a variety of SoCs.

Table 2-1. TPS65215-Q1 Power Resources

	Input Voltage	Output Voltage	Current Capability	Comments
BUCK1	2.5V - 5.5V	0.6V - 3.4V	3.5A	• 2.3MHz switching frequency. • Dynamic voltage scaling. • Programmable power sequencing and default voltages. • Integrated voltage supervisor for undervoltage.
BUCK2	2.5V - 5.5V	0.6V - 3.4V	1.5A	
BUCK3	2.5V - 5.5V	0.6V - 3.4V	1.5A	
LDO1	1.5V - 5.5V (LDO, Load-Switch) 1.5V - 3.4V (bypass)	0.6V - 3.4V (LDO) 1.5V - 3.4V (bypass)	400mA	• Programmable power sequencing and default voltages. • Configurable as load switch and bypass-mode. • Integrated voltage supervisor for undervoltage.
LDO2	2.2V - 5.5V	1.2V - 3.3V	300mA	• Programmable power sequencing and default voltages. • Configurable as load switch. • Integrated voltage supervisor for undervoltage.

2.3 EVM Configuration

Configure the TPS65215Q1EVM as follows. The following sections outline how to configure the TPS65215Q1EVM for general experimentation.

1. Configure regulator input supply rails for the expected application using the jumpers indicated in the *Supply Voltage Setup*.
2. Configure the multi-function pins externally using the mode configuration descriptions indicated in *ulti-Function Pin Setup*. Please note that the default configuration for regulator choice in SD or DDR voltage selection differs for each individual NVM configuration (polarity is configurable).
3. Connect VSYS to a power supply capable of supporting the application and enable the supply.
4. If using a version of TPS65215-Q1 configured for first supply detection (FSD), then the power-up sequence is executed as soon as a valid supply is connected to VSYS.

2.3.1 Default EVM Configuration

This section describes the default configuration programmed on the TPS65215-Q1 PMIC.

The TPS65215Q1EVM comes with the TPS6521501-Q1 PMIC installed, which is one of the orderable part numbers of the TPS65215-Q1 device family. The default output voltages for the Bucks and LDOs are shown in Figure 2-1. This information is based on the programmed default configuration on the TPS65215-Q1EVM. Refer to the device data sheet for more information about the settings that are reconfigurable, and the associated I^{2}C registers.

Note

The TPS65215Q1EVM is designed to demonstrate some of the potential uses of the PMIC family. The EVM has more limitations than the TPS65215-Q1 device.

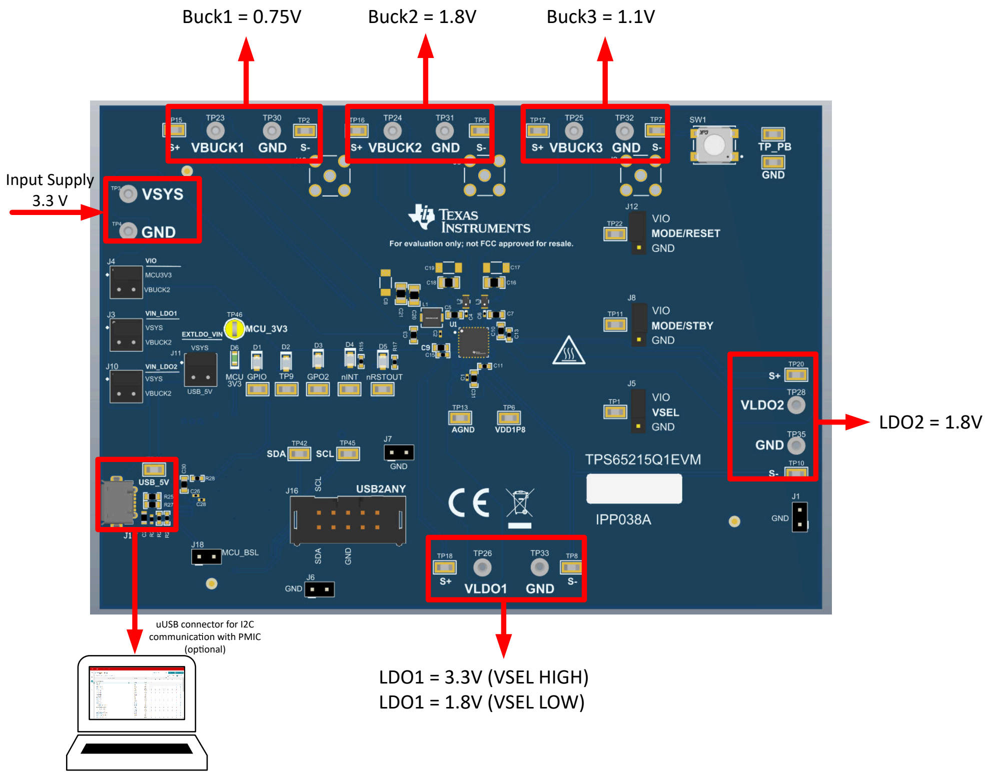

Figure 2-1. TPS65215Q1EVM Default Configuration - Output Voltages

Use the multiple headers of the TPS65215Q1EVM to change the input supply for some of the power rails. The PCB also includes headers that allow for changing specific functions of the PMIC using the multi-function pins. An overview of the jumper options for each header is shown in Figure 2-2. All the headers and the expected configuration for each selection are listed in Table 2-2.

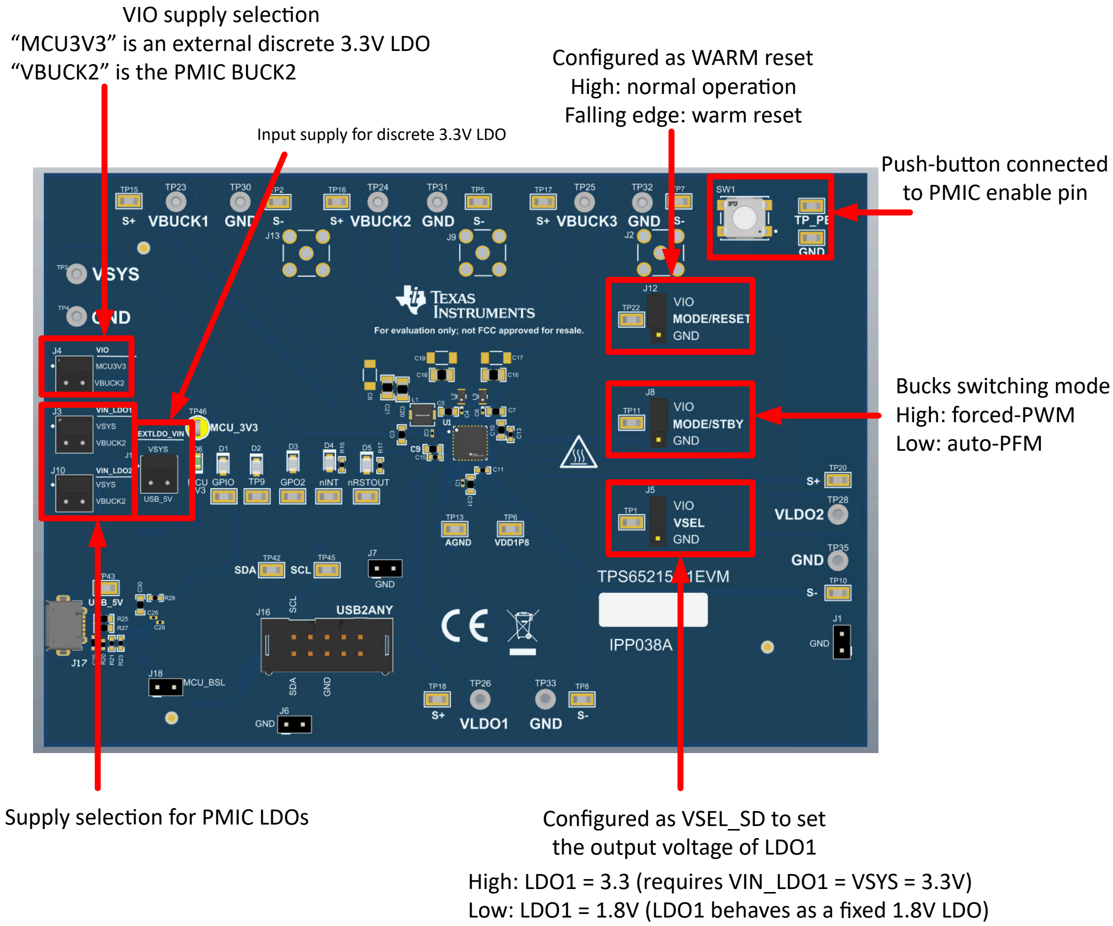

Figure 2-2. TPS65215Q1EVM Default Configuration - Jumpers

Table 2-2. TPS65215Q1EVM Default Jumper Configuration

	Header		Jumper Default Position
Supply voltage setup	J3	VIN_LDO1	Supply selection for LDO1 Default: setup to supply LDO1 with VSYS
	J10	VIN_LDO2	Supply selection for LDO2 Default: setup to supply LDO2 with VSYS
	J11	EXTLDO_VIN	Supply selection for the external discrete LDO. Default: setup to supply the discrete 3.3V LDO with VSYS
	J4	VIO	VIO supply selection Default: setup to use external 3.3V discrete LDO as the pull-up supply for the I^2C pins and digital input pins)
Multi-function pin setup	J5	VSEL	High = sets 3.3V output voltage on LDO1 if the LDO is supplied by a 3.3V source. (default EVM config) Low = sets 1.8V output voltage on LDO1
	J8	MODE/STBY	Bucks switching mode High = forced-PWM (default EVM config) Low = auto-PFM
	J12	MODE_RESET	High = normal operation (default EVM config) Low = performs a warm reset (reset target voltage and Bypass mode configs to the default NVM values)

2.3.2 Test Points

The TPS65215Q1EVM EVM contains multiple test points for various measurements. Trace assignments to the test points are shown in the table below.

Table 2-3. TPS65215-Q1 EVM Test Points

Test Point	Associated Trace
TP1	VSEL_SD/VSEL_DDR
TP2	GND
TP3	VSYS
TP4-5	GND
TP6	VDD1P8
TP7-10	GND
TP11	MODE/STBY
TP12	GND
TP13	GND
TP14	PB / EN
TP15	Buck 1 Output SENSE
TP16	Buck 2 Output SENSE
TP17	Buck 3 Output SENSE
TP18	LDO 1 Output SENSE
TP20	LDO 2 Output SENSE
TP22	MODE/RST
TP23	Buck 1 Output
TP24	Buck 2 Output
TP25	Buck 3 Output
TP26	LDO 1 Output
TP28	LDO 2 Output
TP30-36	GND
TP37	GPIO
TP38	GPO1
TP39	GPO2
TP40	nINT
TP41	nRSTOUT
TP42	SDA
TP43	USB_5V
TP44	GND
TP45	SCL
TP46	MCU3V3

3 Software

3.1 Graphical User Interface (GUI)

This section covers the usage and capabilities of the TPS65215 Graphical User Interface (GUI) tool from Texas Instruments.

Use the TPS65215-GUI in your browser or as a standalone application. This software provides a simple way to communicate with the device via I^2C using the built-in USB2ANY utilizing an on-board MSP430.

3.1.1 Getting Started

Getting started involves the following steps:

1. Find the GUI within the Gallery
2. Download the required software
    a. GUI composer Runtime for running the GUI from a web browser
    b. An offline copy of the GUI
3. Launch the GUI

3.1.1.1 Finding the GUI

The PMIC GUI is based upon GUI Composer which is compatible with either Chrome® (version 46+) or Firefox® (version 38+). The Chrome web browser is recommended and used throughout this document for demonstration. The PMIC GUI is also compatible with Microsoft Edge® (as of version 111.0.1661.41). The GUI is found through the TI Development tools at TI DevTools page. Navigating to the Gallery from the Tools tab, highlighted in blue in Figure 3-1, is one way to enter the Gallery.

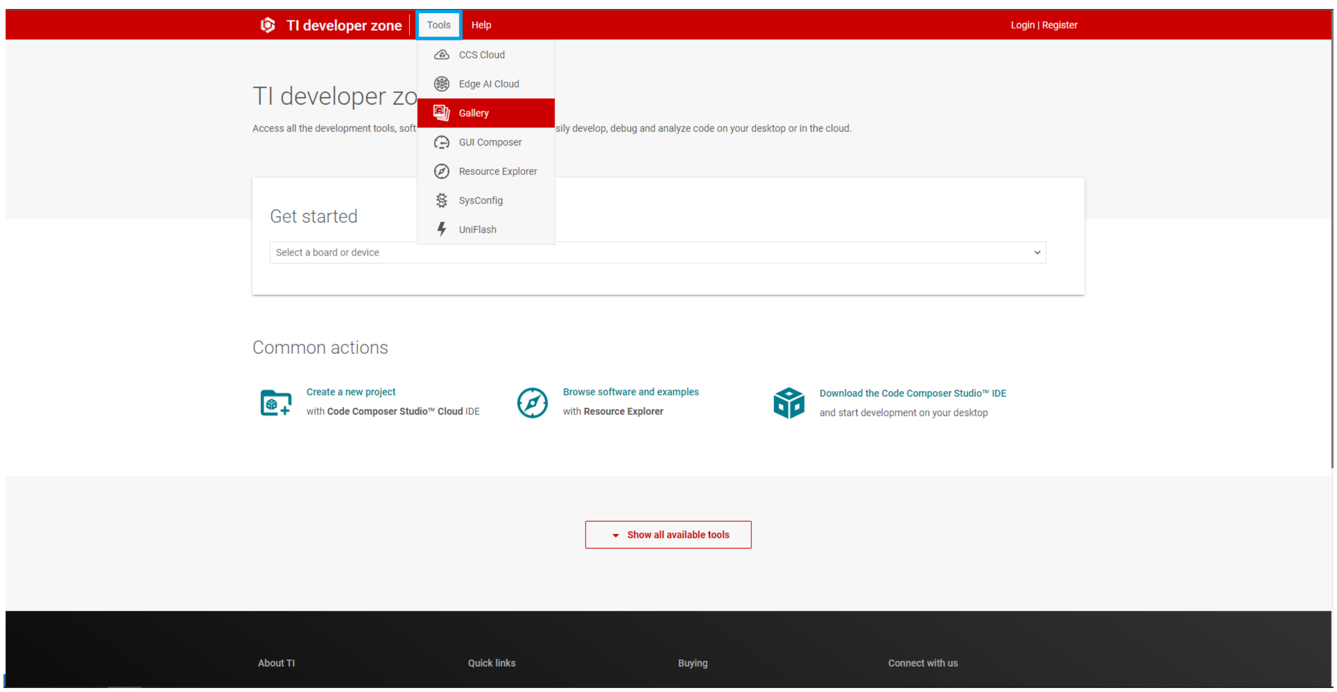

Figure 3-1. GUI Composer Gallery

In the gallery, locate the TPS65215_GUI panel shown in Figure 3-2 by using the search bar and entering TPS65215_GUI.

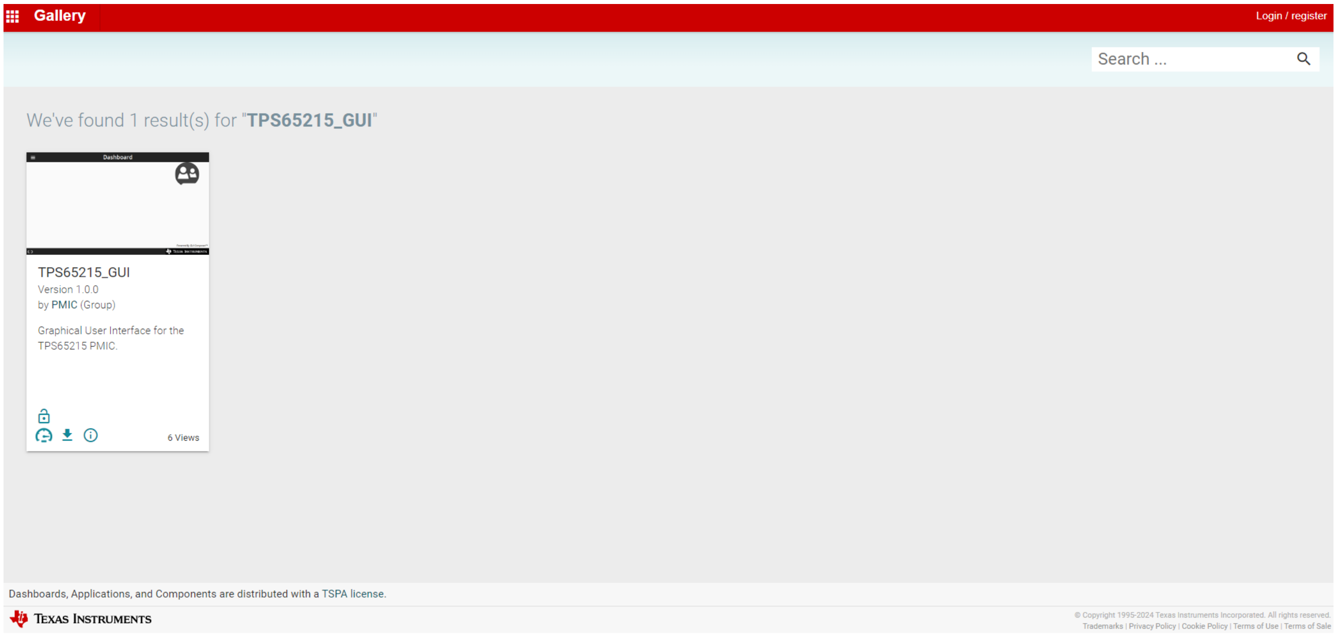

Figure 3-2. Locating the PMIC GUI in the Gallery

3.1.1.2 Downloading the Required Software

Both the standalone GUI and the GUI Composer Runtime are available from the PMIC panel. Again, the GUI Composer Runtime enables the GUI to be run through a web browser but requires an internet connection to be able to run the GUI. By contrast, the standalone GUI is much larger but does not require an internet connection.

The download options are found in the pop-up window, as shown in Figure 3-3, when the cursor is placed on the download icon. The upper three options offer a standalone download for the appropriate operating system, while the lower three are for the GUI Composer Runtime.

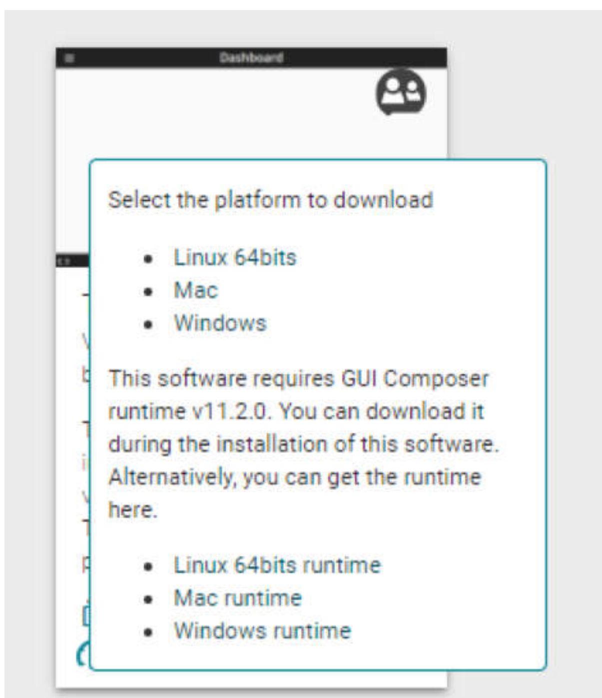

Figure 3-3. GUI Software Download Options

3.1.1.3 Launching the GUI

After the appropriate software has been downloaded, the locally launch the GUI from the PC application or from the TI Cloud using the Gallery. To use the TI Cloud version of the GUI, simply click anywhere in the panel, shown in Figure 3-4, that is not associated with the download or information icons.

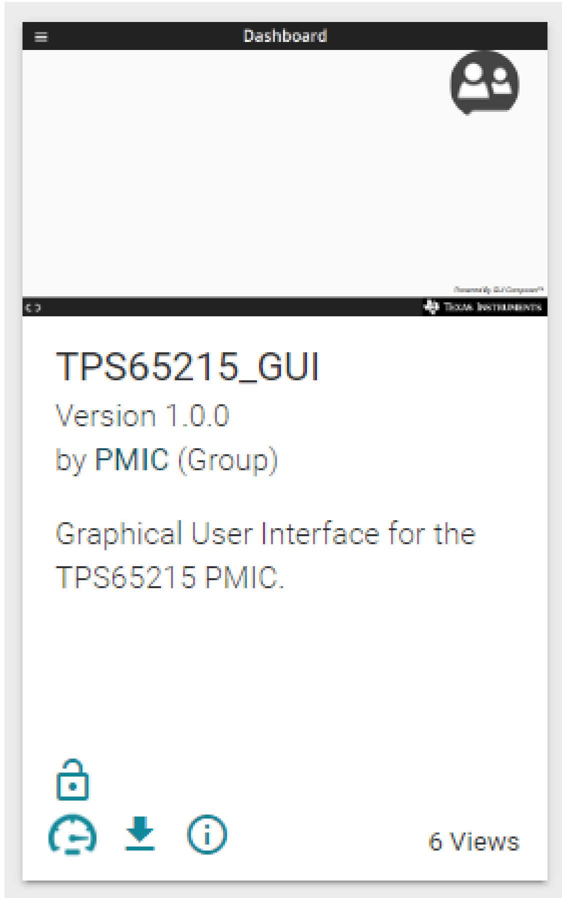

Figure 3-4. GUI Panel Within the Gallery

3.1.1.4 Connecting to the EVM

The README text box helps users connect the EVM board to the computer. Use the *Help* tab in the top left of the GUI dashboard to access the README text box and the *About* option for information about the GUI version and additional documentation regarding the GUI.

After users have dismissed the README message box, the GUI displays the Home page, shown in Figure 3-5, with an overview of the TPS65215-Q1 block diagram.

At the bottom of the Home page, navigate to the other GUI pages, which are described in the subsequent sections. These pages are also found on the left side of the GUI interface.

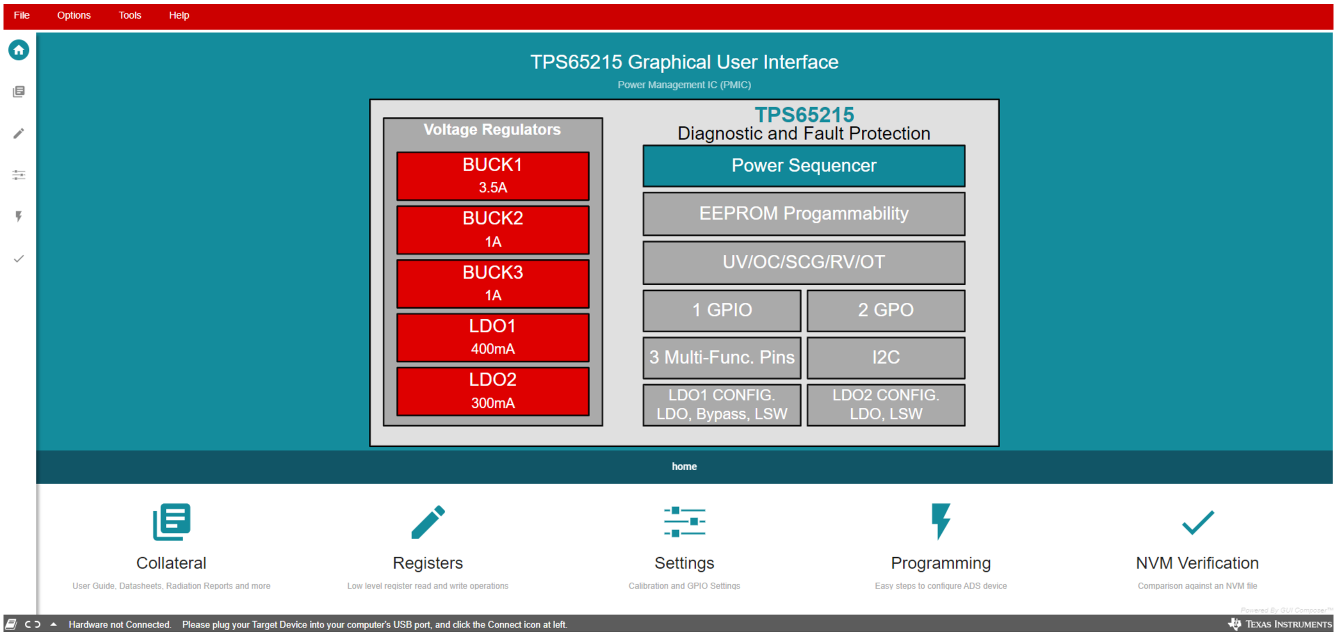

Figure 3-5. GUI Home Page

3.1.2 Collateral Page

The collateral page, shown in Figure 3-6, contains relevant documentation for using the TPS65215-Q1 PMICs. The collateral page contains links to the EVM User's Guide and TPS65215-Q1 data sheets.

At the bottom of the page, there is a link to our E2E forums for technical questions about the GUI or PMIC.

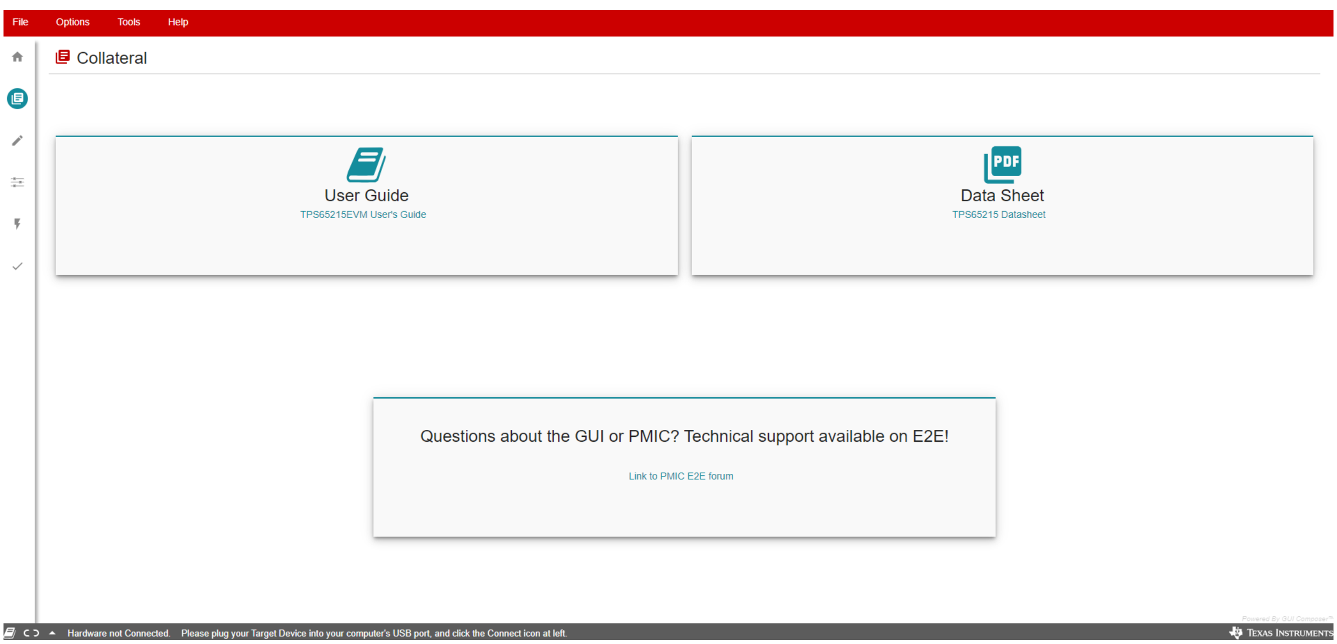

Figure 3-6. Collateral Page

3.1.3 Register Map Page

The register map page lists the different registers available for configuration and is intended for direct reads and writes to the PMIC registers, as shown in Figure 3-7. Reading and writing registers are either done individually or all at once. Enable the Auto Read feature by using the drop-down menu next to the *READ ALL REGISTERS* button to select an automatic read timing. Use the search bar at the top of the page to search registers by name or address.

The first three columns under the search bar show the name of each register, followed by the hexadecimal address and data value. The *Bits* column contains the bit values for each register and can be hidden by unchecking the *Show Bits* box at the top of the page, under the *READ ALL REGISTERS* button. Double-clicking a bit in this section changes the bit value.

The Field View section on the right side of the page shows register bits grouped by the respective control blocks. Click on any bit field box to see the corresponding bits highlighted in yellow in the *Bits* column. Each field has a name shown by the blue text at the top of each box. Find these names using the search bar by checking the *Search Bitfields* box (next to *Show Bits*).

In the *Immediate Write* mode (drop-down option located at the top right of the page), write buttons are grayed out since individual registers are written immediately with each change in the Field View, change in bits, or change in hexadecimal value. In *Deferred Write* mode, the writing of a single register or all registers is deferred until the *WRITE REGISTER* or *WRITE ALL REGISTERS* button is selected.

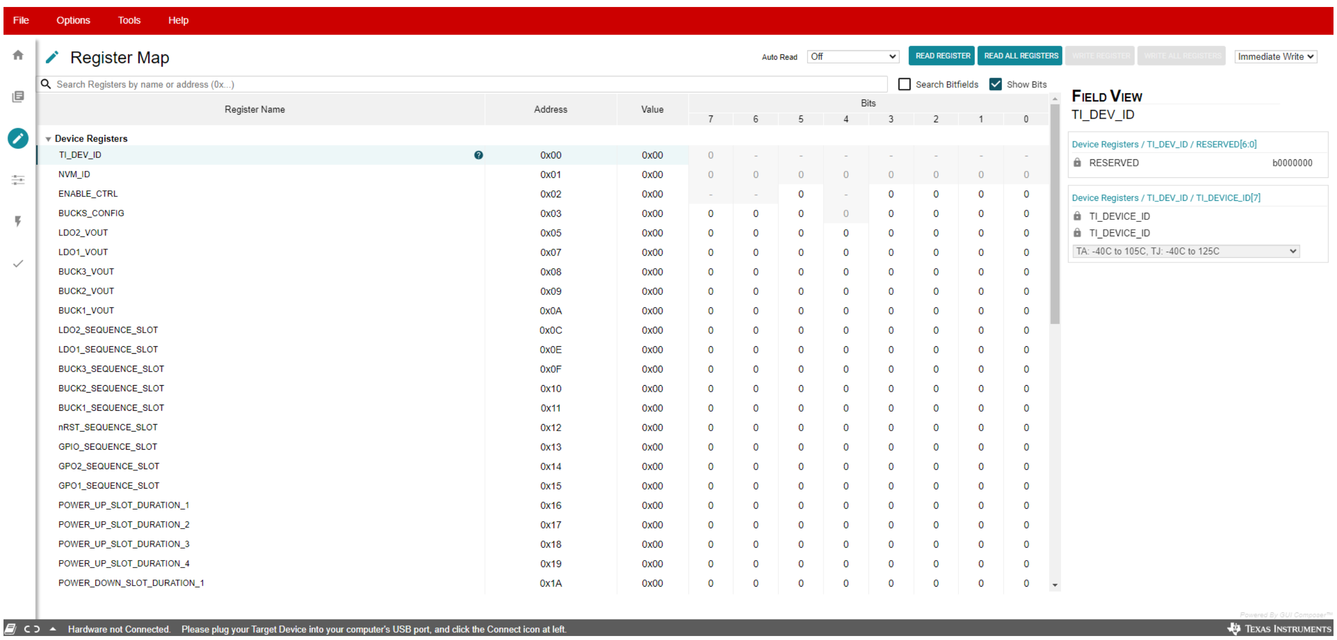

Figure 3-7. Register Map Page

Note

Although visible from the Register Map, not all registers are editable from this page. Attempting a write to a read-only register does not generate an error. Since each write is comes with an associated read, the Register Map display is updated to reflect that the bits were not changed by the write attempt.

3.1.4 NVM Configuration Page

The NVM Configuration page (shown in Figure 3-8) is the main feature of the GUI and highlights the configurability of the PMIC. On this page, register fields are grouped according to the use case and are labeled to indicate which part of the PMIC is controlled by each block. The NVM configuration page also provides the interface to save a custom configuration or load an existing configuration into the NVM of the target device. A full register read is done using the *READ ALL REGISTERS* button in the top left of the page.

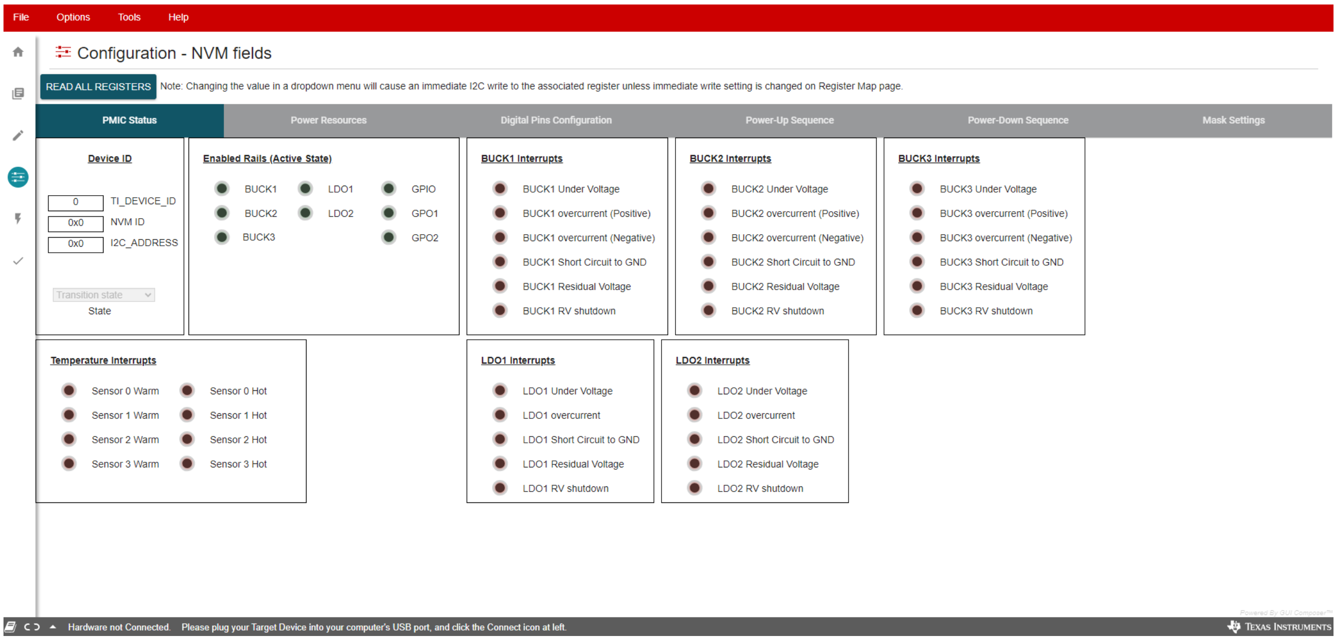

Figure 3-8. NVM Configuration Page

3.1.4.1 NVM Fields

Register settings are editable on the NVM Configuration Page and follow the register write setting specified on the Register Map page (Immediate or Deferred).

The *PMIC Status* tab holds a collection of read-only status registers that show the Device ID values as well as all the power rail enables and interrupts, which are displayed as digital LEDs. This section provides fast visual feedback on the PMIC and the operating conditions.

The *Power Resources* tab holds register settings for each power rail of the PMIC. Here, users also find a reference table for LDO1 and LDO2 configuration settings (for more information on the Load Switch and BYPASS modes, refer to the device data sheet which is included on the Collateral page).

The *Sequence* tab is used to control power rail sequence and timing registers for both power-up and power-down.

The *Digital Pins Configuration* tab is used to control settings for digital I/O pins (for details on multi-function pins, see the PMIC data sheet).

The *Mask Settings* tab allows users to control fault reporting for PMIC protection features, which includes masking for undervoltage, temperature, and interrupt signals.

3.1.4.2 Create and Load a Custom Configuration

The NVM Configuration page does not require hardware to develop an NVM configuration. Connection with an actual device is needed only when attempting to upload to a target device.

Once the registers are set to your desired configuration, use the *Register File Format* option, under the *File* tab at the top of the screen, to select a format for your configuration file (shown in Figure 3-9). Save the register configuration in either a CSV (Comma Separated Values) or a JSON (Javascript Object) format. Next, use the *Save Registers As…* option to save your configuration in your selected format. Once the file is created, save any changes you make to the register configuration using the *Save Registers* option. This option saves to the currently loaded configuration.

To load an existing configuration into the NVM, use the *Load Registers* option and browse to the configuration file location.

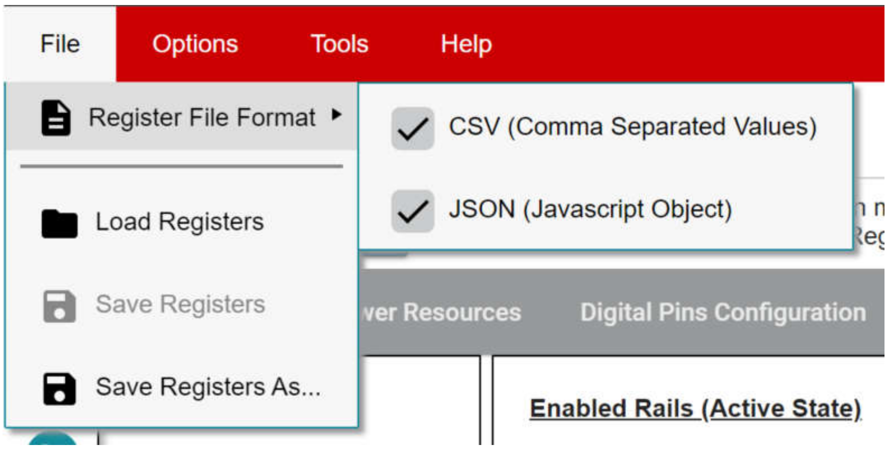

Figure 3-9. Save/Load Register Options

3.1.5 Sequence Configuration

The TPS65215-Q1 GUI features sequence configuration tabs for modifying and plotting the power-up and power-down sequences. The *power-up sequence* and *power-down sequence* tabs plot the voltage level of each signal as a function of time based on the corresponding settings.

Plotting Features

The features of the sequence configuration tabs is demonstrated in Figure 3-10.

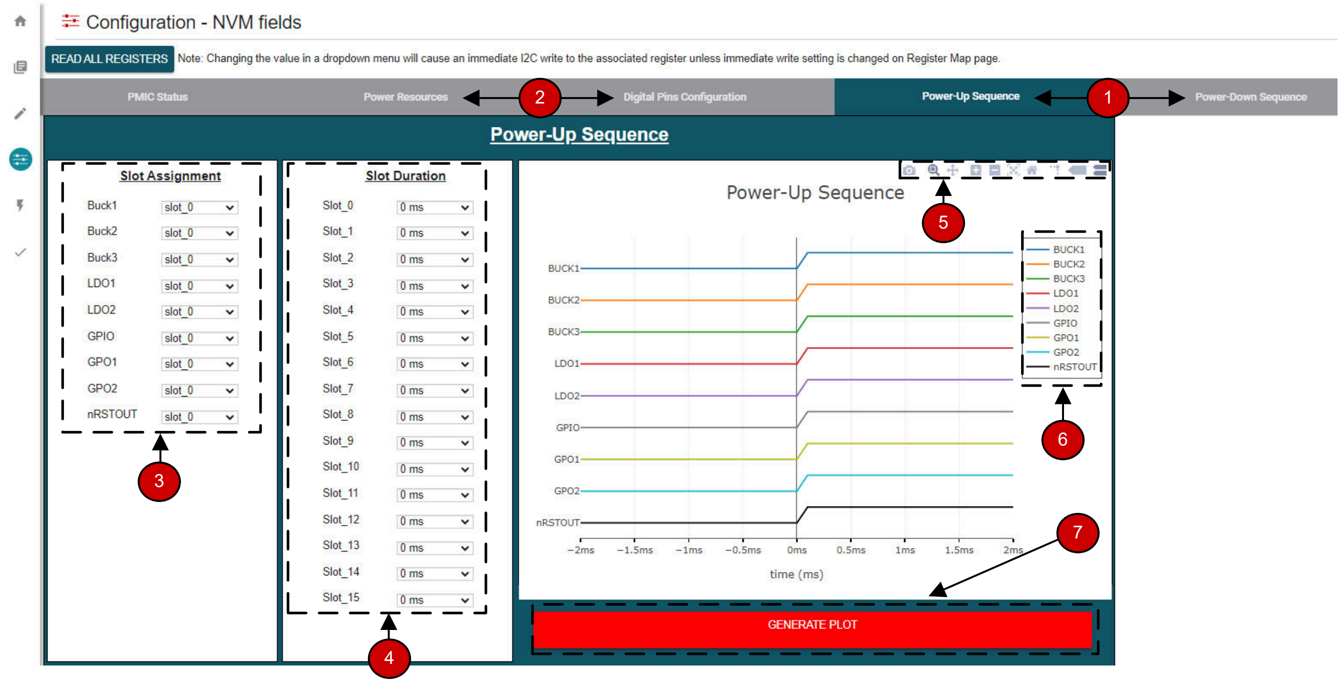

Figure 3-10. Sequence Plotting Tool

Note

Graph rise and fall time durations are not accurate. The actual rise and fall times dependent on load capacitance and other variables.

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1. *Power-up sequence* and *power-down sequence* plotting tabs.
2. Rails disabled in active state always remain low when plotted. Configure these settings in the "*Power Resources* or *Digital Pins Configuration* tab.
3. Slot Assignment: There are 16 possible slot assignments (Slot 0 to Slot 15) assigned to each rail for flexible power sequences.
4. Slot Duration: There are four possible slot durations (0ms, 1.5ms, 3ms, 10ms) assigned to each slot for flexible power sequences.
5. Plot menu bar appears upon hovering over graph. This feature is explained in Menu Bar Options
6. Click on a signal in the legend to change the visibility.
7. Plot the design by pressing the *Generate Plot* button. Signal order is sorted based on which signals rise or fall first

Menu Bar Options

The plot menu bar has several settings including:

- Camera: download plot as PNG
- Zoom: left click and drag the mouse on the graph to zoom into the selected area. Enabled by default.
- Pan: left click and drag the mouse to navigate the plot.
- Zoom in
- Zoom out
- Auto-scale graph
- Reset axis
- Toggle like spikes
- Show closest data on hover

- Compare data on hover. Enabled by default.

3.1.6 NVM Programming Page

The NVM Programming page allows re-programming the device NVM memory to change the default register settings. This page includes four main functions that correspond to the buttons shown in Figure 3-11. The first two steps *I2C OFF REQUEST* and *ENABLE I2C COMMUNICATION* are only needed when re-programming the PMIC from the Initialize state (PMIC rails OFF).

- The **I2C OFF REQUEST** button triggers an OFF request though I2C and sends the PMIC to INITIALIZE state.
- The **ENABLE I2C COMMUNICATION** button enables I2C communication in INITIALIZE state.
  - Once I2C communication is enabled, go to the NVM configuration page to select the desired register settings or use the *File* tab options to load a pre-configured JSON or CSV file.
- The **NVM PROGRAMMING** button programs the selected register settings into the NVM.
- The **VALIDATE NVM PROGRAMMING** button reads the NVM content and compares with the selected register settings. The result (PASS or FAIL) is stored in register 0x34, field 7 *NVM_VERIFY_RESULT*.

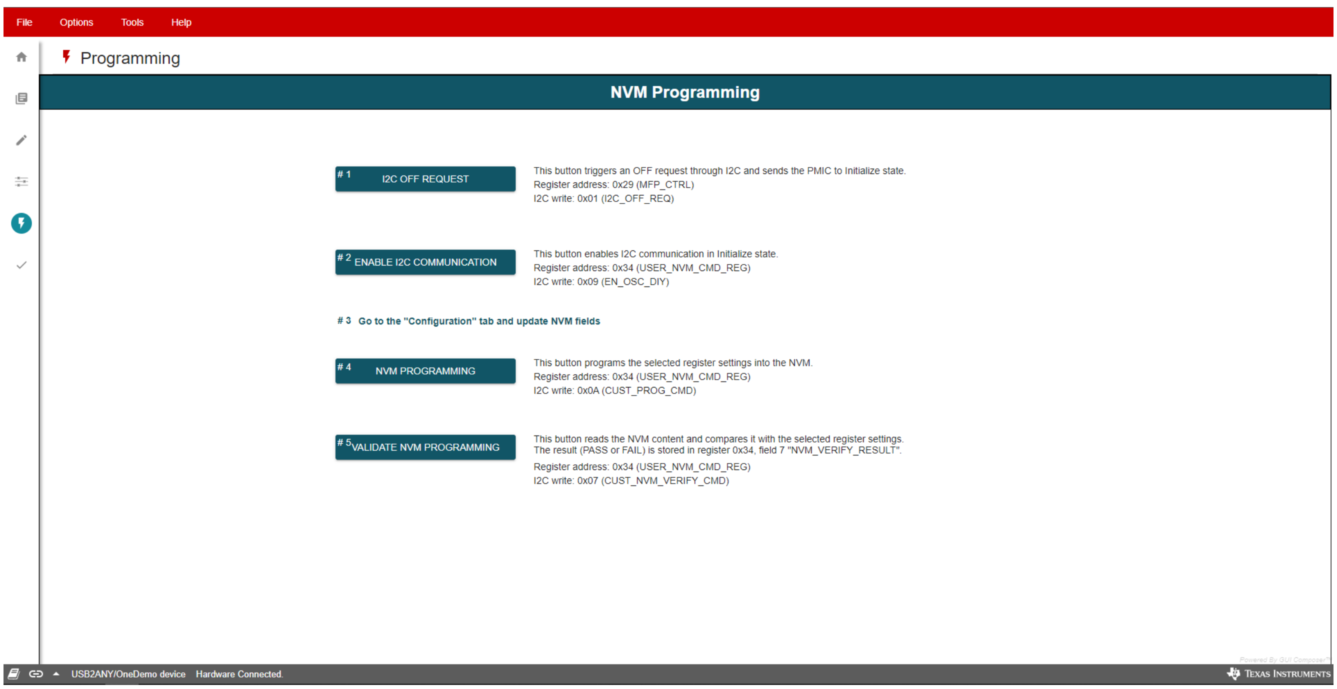

Figure 3-11. NVM Programming Page

3.1.7 Additional Features

In the Options tab at the top of the GUI interface, select *Serial Port…* to display information about the EVM connection to the computer.

The *Tools* tab includes the *Log pane* option. Select this option to open a window that lists recent messages and warnings from the GUI application. These reports are marked with the date and time that each one was received. In the top right of the log window, filter out the different information types, save the list of events, and clear or close the log window.

4 Hardware Design Files

4.1 TPS65215Q1EVM Schematic

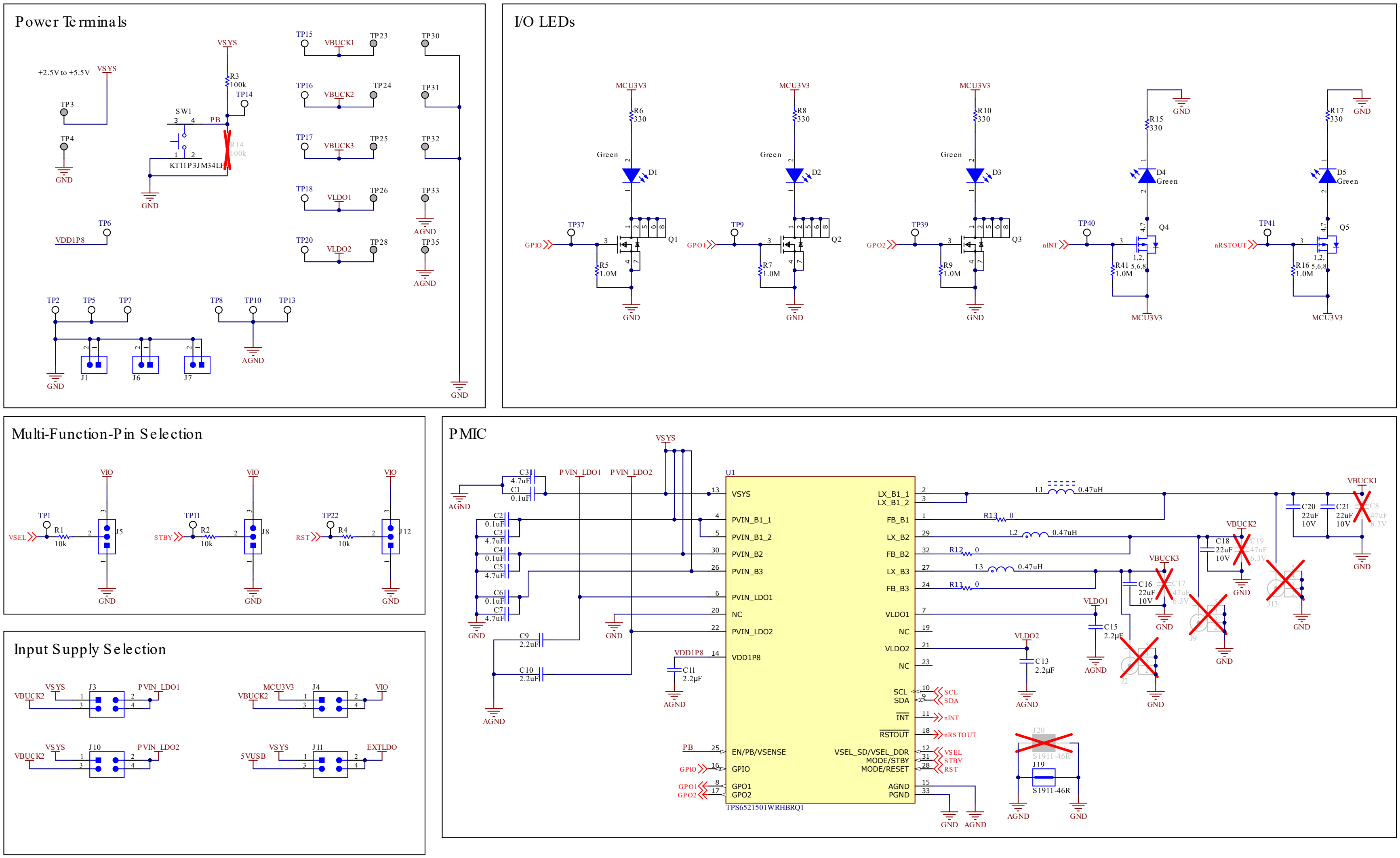

Figure 4-1. TPS65215Q1EVM, Schematic Page 1

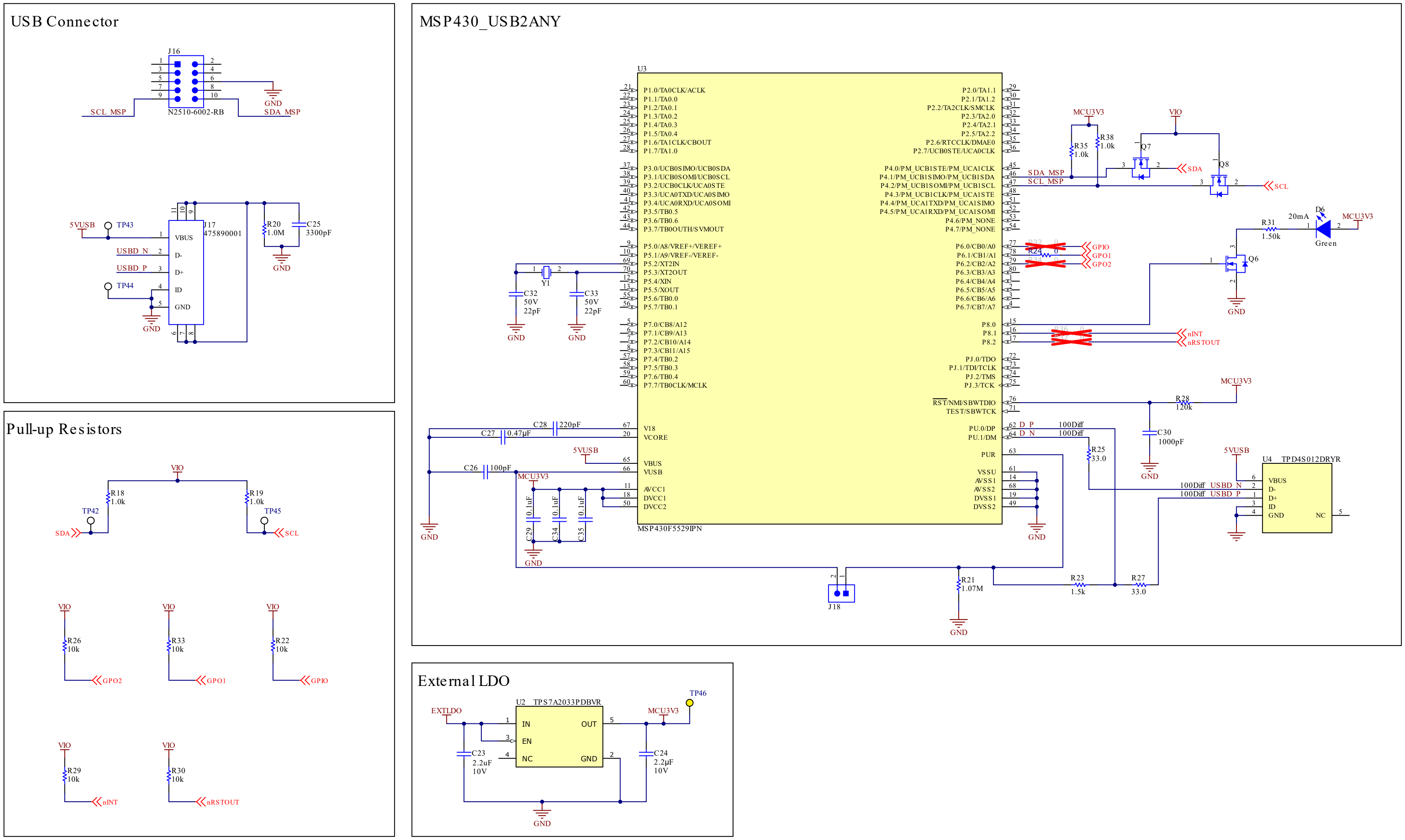

Figure 4-2. TPS65215Q1EVM, Schematic Page 2

4.2 TPS65215Q1EVM PCB Layers

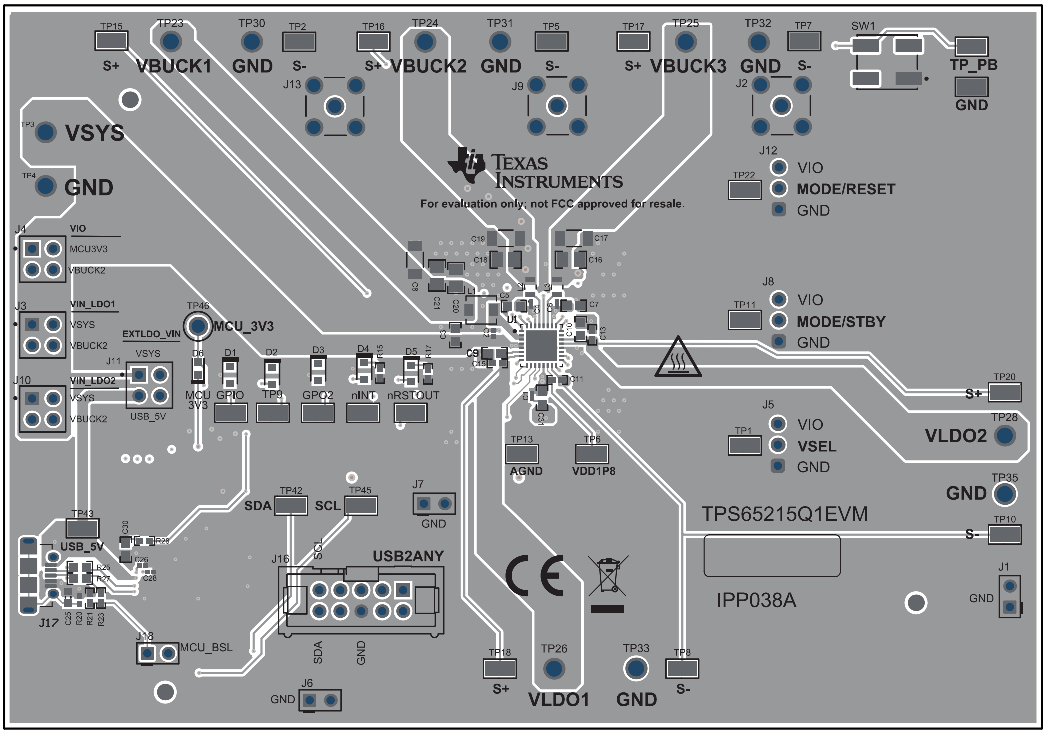

Figure 4-3. TPS65215Q1EVM Top Layer

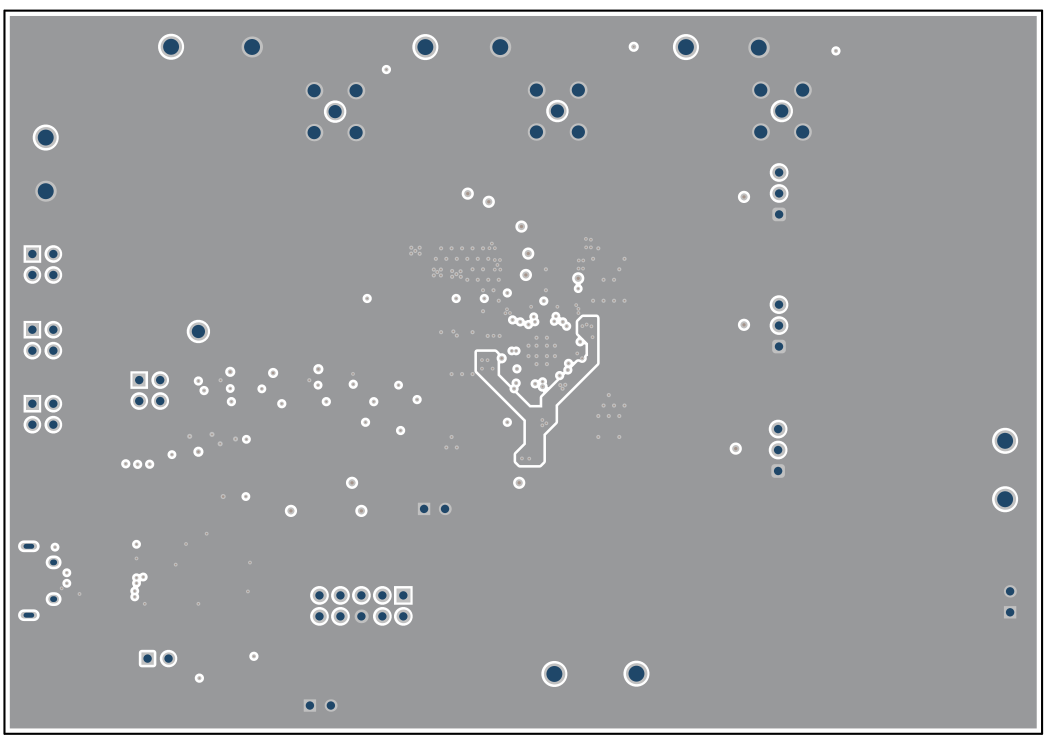

Figure 4-4. TPS65215Q1EVM - Signal Layer1

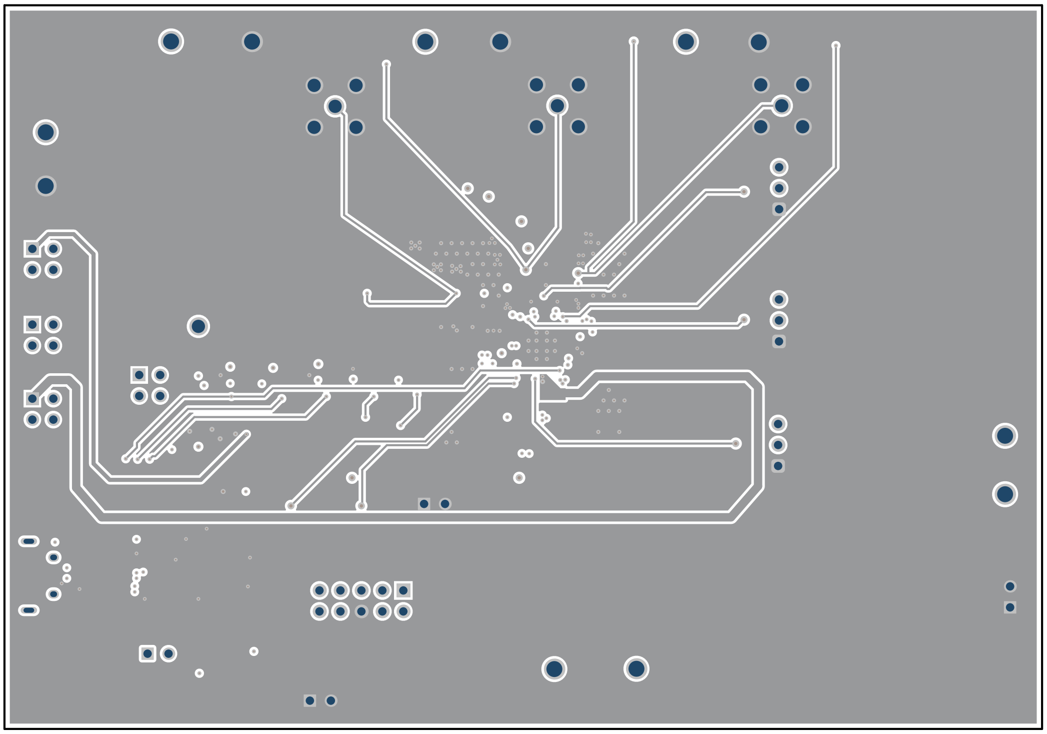

Figure 4-5. TPS65215Q1EVM - Signal Layer2

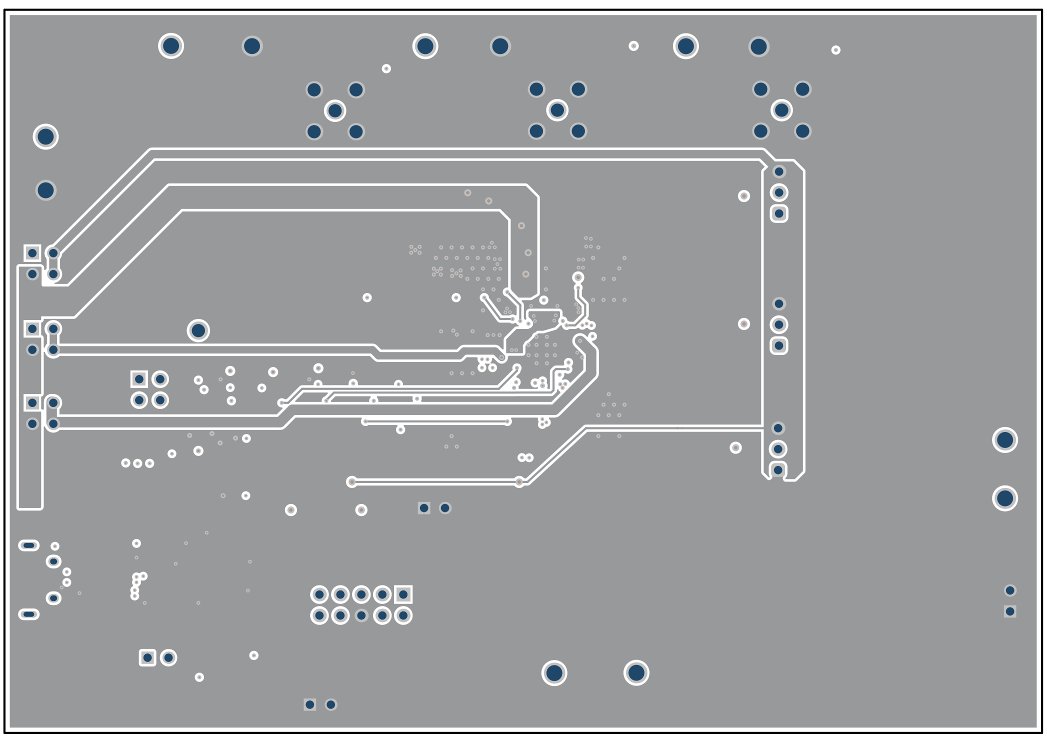

Figure 4-6. TPS65215Q1EVM - Signal Layer3

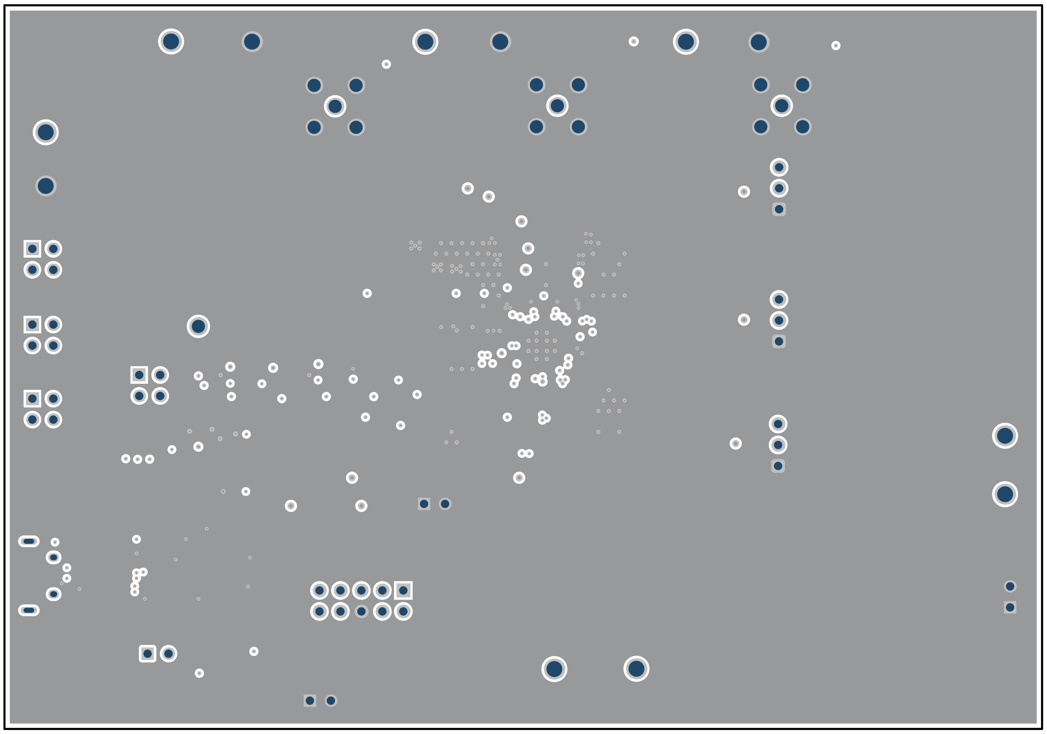

Figure 4-7. TPS65215Q1EVM - Signal layer4

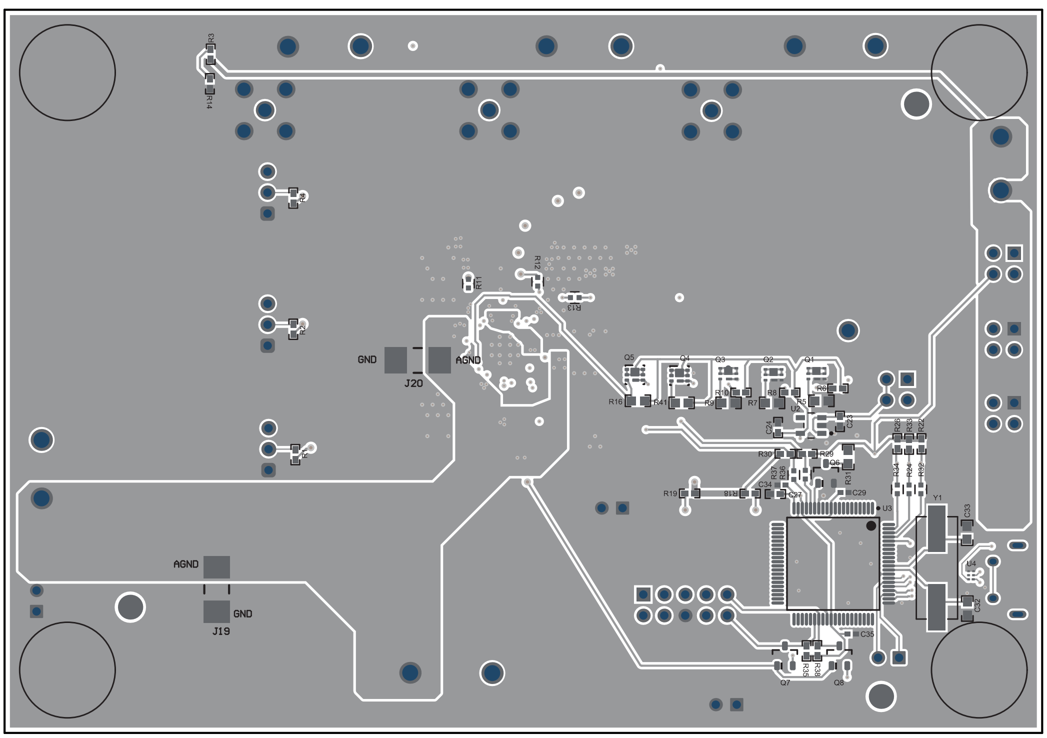

Figure 4-8. TPS65215Q1EVM - Bottom Layer

4.3 TPS65215Q1EVM Bill of Materials

Table 4-1. Bill of Materials

DESIGNATOR	QUANTITY	VALUE	DESCRIPTION	PART NUMBER	MANUFACTURER
C1, C2, C4, C6	4	0.1uF	CAP, CERM, 0.1uF, 10V,+/- 10%, X7S, 0201	GRM033C71A104KE14D	MuRata
C3, C5, C7, C9, C10, C31	6	4.7uF	CAP, CERM, 4.7uF, 10V, +/- 10%, X7S, 0603	C1608X7S1A475K080AC	TDK
C11, C13, C15, C23, C24	5	2.2uF	CAP, CERM, 2.2uF, 10V, +/- 10%, X7S, 0402	C1005X7S1A225K050BC	TDK
C16, C18, C20, C21	4	22uF	CAP, CERM, 22uF, 10V, +/- 20%, X7R, 0805	GRM21BZ71A226ME15L	MuRata
C25	1	3300pF	CAP, CERM, 3300pF, 50V, +/- 10%, X7R, 0603	C0603C332K5RACTU	Kemet
C26	1	100pF	CAP, CERM, 100pF, 16V, +/- 10%, X7R, 0201	GRM033R71C101KA01D	MuRata
C27	1	0.47uF	CAP, CERM, 0.47µF, 16V,+/- 10%, X7S, 0402	CGA2B1X7S1C474K050BE	TDK
C28	1	220pF	CAP, CERM, 220pF, 16V, +/- 10%, X7R, 0201	GRM033R71C221KA01D	MuRata
C29, C34, C35	3	0.1uF	CAP, CERM, 0.1uF, 16V, +/- 10%, X7R, 0402	GCM155R71C104KA55D	MuRata
C30	1	1000pF	CAP, CERM, 1000pF, 50V, +/- 10%, X7R, 0603	C0603C102K5RACTU	Kemet
C32, C33	2	22pF	CAP, CERM, 22pF, 50V, +/- 5%, C0G/NP0, 0603	06035A220JAT2A	AVX
D1, D2, D3, D4, D5	5	Green	LED, Green, SMD	LG M67K-G1J2-24-Z	OSRAM
D6	1	Green	LED, Green, SMD	150060VS75000	Wurth Elektronik
H1, H2, H3, H4	4		Bumpon, Hemisphere, 0.44 X 0.20, Clear	SJ-5303 (CLEAR)	3M
J1, J6, J7, J18	4		Header, 100mil, 2x1, Tin, TH	PEC02SAAN	Sullins Connector Solutions
J3, J4, J10, J11	4		Header, 100mil, 2x2, Tin, TH	PEC02DAAN	Sullins Connector Solutions
J5, J8, J12	3		Header, 100mil, 3x1, Gold, TH	TSW-103-07-G-S	Samtec
J16	1		Header (shrouded), 100mil, 5x2, High-Temperature, Gold, TH	N2510-6002-RB	3M
J17	1		Connector, Receptacle, Micro-USB Type AB, R/A, Bottom Mount SMT	475890001	Molex
J19	1		JUMPER TIN SMD	S1911-46R	Harwin
L1	1	0.47uH	470nH Shielded Wirewound Inductor 7A 23mOhm Max 2-SMD	SRP3020TA-R47M	Bourns
L2, L3	2	0.47uH	Thin Film Power Inductor 0.47uH 20% 4.5A 29mOhm 0805	TFM201208BLE-R47MTCF	TDK
LBL1	1		Thermal Transfer Printable Labels, 0.650" W x 0.200" H - 10,000 per roll	THT-14-423-10	Brady
Q1, Q2, Q3	3		30V N-Channel NexFET™ Power MOSFET	CSD17318Q2	Texas Instruments
Q4, Q5	2	-20V	MOSFET, P-CH, -20V, -20A, DQK0006C (WSON-6)	CSD25310Q2	Texas Instruments
Q6	1	50V	MOSFET, N-CH, 50V, 0.22A, SOT-23	BSS138	Fairchild Semiconductor
Q7, Q8	2	50V	MOSFET, N-CH, 50V, 0.22A, SOT-23	BSS138	Fairchild Semiconductor
R1, R2, R4, R22, R26, R29, R30, R33	8	10k	RES, 10k, 5%, 0.063W, AEC-Q200 Grade 0, 0402	CRCW040210K0JNED	Vishay-Dale

Table 4-1. Bill of Materials (continued)

DESIGNATOR	QUANTITY	VALUE	DESCRIPTION	PART NUMBER	MANUFACTURER
R3	1	100k	RES, 100k, 5%, 0.1W, AEC-Q200 Grade 0, 0402	ERJ-2GEJ104X	Panasonic
R5, R7, R9, R16, R41	5	1.0Meg	RES, 1.0M, 5%, 0.1W, AEC-Q200 Grade 0, 0603	CRCW06031M00JNEA	Vishay-Dale
R6, R8, R10, R15, R17	5	330	RES, 330, 5%, 0.063W, AEC-Q200 Grade 0, 0402	CRCW0402330RJNED	Vishay-Dale
R11, R12, R13, R24	4	0	RES Thick Film, 0Ω, 0.2W, 0402	CRCW04020000Z0EDHP	Vishay Dale
R18, R19, R35, R38	4	1.0k	RES, 1.0k, 5%, 0.063W, AEC-Q200 Grade 0, 0402	CRCW04021K00JNED	Vishay-Dale
R20	1	1.0Meg	RES, 1.0M, 5%, 0.063W, AEC-Q200 Grade 0, 0402	CRCW04021M00JNED	Vishay-Dale
R21	1	1.07Meg	RES, 1.07M, 1%, 0.063W, AEC-Q200 Grade 0, 0402	CRCW04021M07FKED	Vishay-Dale
R23	1	1.5k	RES, 1.5k, 5%, 0.063W, AEC-Q200 Grade 0, 0402	CRCW04021K50JNED	Vishay-Dale
R25, R27	2	33	RES, 33.0, 1%, 0.1W, AEC-Q200 Grade 0, 0603	CRCW060333R0FKEA	Vishay-Dale
R28	1	120k	RES, 120k, 5%, 0.063W, AEC-Q200 Grade 0, 0402	CRCW0402120KJNED	Vishay-Dale
R31	1	1.50k	RES, 1.50k, 1%, 0.1W, AEC-Q200 Grade 0, 0603	CRCW06031K50FKEA	Vishay-Dale
SH-J1, SH-J3, SH-J4, SH-J6, SH-J7, SH-J8, SH-J9	7	1x2	Shunt, 100mil, Flash Gold, Black	SPC02SYAN	Sullins Connector Solutions
SW1	1		Switch Tactile N.O. SPST Round Button J-Bend 32VAC 32VDC 1VA 100000Cycles 3N SMD Tube/T/R	KT11P3JM34LFS	C&K Components
TP1, TP2, TP5, TP6, TP7, TP8, TP9, TP10, TP11, TP13, TP14, TP15, TP16, TP17, TP18, TP20, TP22, TP37, TP39, TP40, TP41, TP42, TP43, TP44, TP45	25		Test Point, Miniature, SMT	5015	Keystone Electronics
TP3, TP4, TP23, TP24, TP25, TP26, TP28, TP30, TP31, TP32, TP33, TP35	12		PCB Pin, Swage Mount, TH	2505-2-00-44-00-00-07-0	Mill-Max
TP46	1		Test Point, Compact, Yellow, TH	5009	Keystone Electronics
U1	1		TPS6521501WRHBRQ1	TPS6521501WRHBRQ1	Texas Instruments
U2	1		300mA, Ultra-Low-Noise, Low-IQ, High PSRR LDO	TPS7A2033PDBVR	Texas Instruments
U3	1		25MHz Mixed Signal Microcontroller with 128KB Flash, 8192 B SRAM and 63 GPIOs, -40 to 85 degC, 80-pin QFP (PN), Green (RoHS & no Sb/Br)	MSP430F5529IPN	Texas Instruments
U4	1		4-Channel USB ESD Solution with Power Clamp, DRY0006A (USON-6)	TPD4S012DRYR	Texas Instruments
Y1	1		Crystal, 24.000MHz, 20pF, SMD	ECS-240-20-5PX-TR	ECS Inc.

5 Additional Information

5.1 Trademarks

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6 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (July 2025) to Revision A (September 2025)	Page
• Added *Setup* section	4
• Updated current capabilities	4
• Updated default configuration of J3	5