*EVM User's Guide: TPS548B23EVM*

# *TPS548B23 Step-Down Converter Evaluation Module*

## Description

The TPS548B23EVM is designed to provide a quick setup to evaluate the TPS548B23 device and gain familiarity with the device. This EVM can deliver a continuous load current of up to 20A, operating within an input voltage range of 8V to 16V (12V nominal) and the output voltage range of 0.5V to 5.5V (1.0V default). The TPS548B23 uses a nominal 12V bus to produce a regulated 1.0V (default) output at up to 20A of load current. The TPS548B23EVM includes jumpers to quickly configure different settings selected by the CFG pins and test points to evaluate the device's performance.

## Get Started

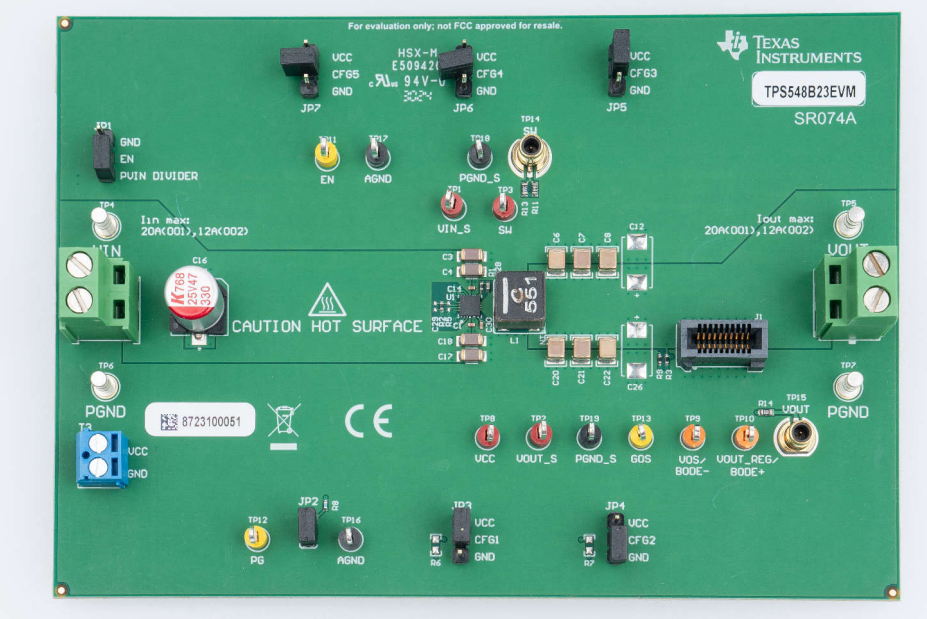
1. Order the TPS548B23EVM.
2. Download the latest TPS548B23 data sheet.

## Features

- Input voltage range: 8V to 16V, 12V nominal
- Output voltage range: 0.5V to 5.5V, 1.0V default
- Output current range: 0A to 20A
- Includes jumpers and resistor placeholders to evaluate different settings selected by the CFG pins
  - Internal feedback configuration:
    - Output voltage: 13 fixed options ranging from 0.8V to 5.0V
    - Operation mode: FCCM or PFM
    - Frequency: 600kHz, 800kHz, or 1200kHz
    - Soft-start: fixed 2ms
    - OCP threshold: 15A, 18A, or 21A
    - Fault recovery: hiccup mode
  - External feedback configuration:
    - Output voltage: adjustable from 0.5V to 5.5V using an external resistor divider
    - Operation mode: FCCM or PFM
    - Frequency: 600kHz, 800kHz, 1000kHz, or 1200kHz
    - Soft-start: 1ms, 2ms, or 3ms
    - OCP threshold: resistor programmable
    - Fault recovery: hiccup mode or latch-off

## Applications

- Rack server and blade server
- Data center switches
- Hardware accelerator and add-in cards
- Industrial PC
- Baseband unit (BBU)



# 1 Evaluation Module Overview

## 1.1 Introduction

The TPS548B23EVM evaluation module (EVM) is built using the TPS548B23 device. The EVM is designed to accommodate various settings by changing only the jumper configurations, and therefore, the design is not optimized for any specific condition. The default jumper settings can be found in Table 1-1. The test data in this user's guide were all collected in this configuration. For design optimization, TI offers a range of resources. Users can start by consulting the data sheet. Additionally, TI provide an Excel design calculator, WEBENCH, and simulation models. Users can also contact the TI field representative or use our E2E design support for additional help.

**Table 1-1. Default Jumper Configuration**

| Jumper | Pin | Connection | Device Configuration |
|---|---|---|---|
| JP3 | CFG1 | VCC | • Internal FB Configuration<br>• $V_{OUT}$: 1.0V<br>• Operation mode: FCCM<br>• $F_{SW}$: 800kHz<br>• OCP threshold: 21A<br>• Fault recovery: Hiccup mode |
| JP4 | CFG2 | GND | |
| JP5 | CFG3 | VCC | |
| JP6 | CFG4 | Float | |
| JP7 | CFG5 | Float | |

The following warnings and cautions are noted for the safety of anyone using or working close to the TPS548B23EVM. Observe all safety precautions.

**WARNING**

The TPS548B23EVM can become hot during operation due to dissipation of power in some operating conditions. Avoid contact with the board. Follow all applicable safety procedures applicable to your laboratory.

**WARNING**

The circuit module has signal traces, components, and component leads on the bottom of the board and can result in exposed voltages, hot surfaces or sharp edges. Do not reach under the board during operation.

**CAUTION**

Some power supplies can be damaged by application of external voltages. If using more than 1 power supply, then check the equipment requirements and use blocking diodes or other isolation techniques, as needed, to prevent damage to the equipment.

## 1.2 Kit Contents

The kit includes the TPS548B23EVM.

## 1.3 Specification

A summary of the TPS548B23EVM performance characteristics is provided in Table 1-2. The TPS548B23EVM is designed and tested for $V_{IN}$ = 8V to 16V. Characteristics are given for an input voltage of $V_{IN}$ = 12V and output voltage of 1V (see Table 1-1), unless otherwise specified. The ambient temperature is room temperature (20°C to 25°C) for all measurements, unless otherwise noted.

**Table 1-2. TPS548B23EVM Performance Specifications Summary**

| SPECIFICATION | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{IN}$ voltage range | | | 8 | 12 | 16 | V |
| Input current | $V_{IN}$ = 8V, $I_{OUT}$ = 20A | | | 3 | | A |
| $V_{IN}$ start voltage | Set by EN pin resistor divider | | | 3.84 | | V |
| $V_{IN}$ stop voltage | $V_{IN}$ falling | | | 3.77 | 3.83 | V |
| Output voltage setpoint | | | | 1 | | V |
| Output current range | $V_{IN}$ = 8V to 16V | | 0 | | 20 | A |
| Line and load regulation | $V_{IN}$ = 8V to 16V, $I_{OUT}$ = 0A to 20A | | | ±0.14 | | % |
| Load transient response | $I_{OUT}$ = 5A to 15A | Voltage change | | -21 | | mV |
| | $I_{OUT}$ = 15A to 5A | Voltage change | | 24 | | mV |
| Output ripple voltage | $I_{OUT}$ = 20A | | | 6.8 | | mVPP |
| Soft-start time | From start of switching to $V_{FB}$ = 0.5V, $t_{SS}$ = 2ms setting | | 1.4 | 2 | 2.6 | ms |
| Current limit | OCP = 21A setting by CFG pin selection | | 19 | 21 | 23 | A |
| Switching frequency ($f_{SW}$) | $f_{SW}$ = 800kHz setting by CFG1-5 pin selection | | | 800 | | kHz |
| Peak efficiency | $I_{OUT}$ = 7.5 | | | 90 | | % |
| IC case temperature | $I_{OUT}$ = 20A, 15-minute soak | | | 77.4 | | °C |

## 1.4 Device Information

The TPS548B23 device is a small, high-efficiency, synchronous buck converter with an adaptive on-time D-CAP4 control mode. The device provides low minimum on-time and fast load-transient response without requiring external compensation. The TPS548B23 is an excellent choice for space-constrained data center applications and features differential remote sense, integrated MOSFETs, and an accurate ±1.0% internal reference. Pinstrap options allow the configuration of various parameters such as overcurrent limit, fault response, and soft start time. Additionally, the device is lead-free and RoHS-compliant without exemption.

Please refer to the TPS548B23 4V to 16V Input, 20A, Remote Sense, D-CAP4, Synchronous Buck Converter data sheet for more information about the device.

# 2 Hardware

## 2.1 Configurations and Modifications

These evaluation modules provide access to the TPS548B23 features with jumpers for testing different configurations. All internal feedback configuration settings can be tested without board modifications, while for external feedback configuration, R6, R7, and the resistor divider network (R2 and R5) need to be installed. Modify the module if the desired performance is not achieved. Use the data sheet equations, WEBENCH, or an Excel design calculator to calculate external component values, verifying sufficient voltage and current ratings for all components.

### *2.1.1 Multifunction Configuration (CFG1-5) Pins Selection*

The multifunction configuration pins (CFG1-5) allow the device to be configured for various operating modes. The CFG1-2 pins set the device switching frequency, overcurrent threshold, soft start time, and either hiccup or latch-up fault recovery operation, while the CFG3-5 pins provide selectability for internal or external feedback as well as FCCM or PFM operation.

When the device is configured for internal feedback operation with the CFG 3-5 pins (see Table 2-3), the switching frequency and current limit are programmed by tying the CFG1-2 pins either high (VCC), low (GND) or left floating based on Table 2-1.

**Note**

When the device is configured for internal feedback operation, the soft start time is set to 2ms, and the fault recovery is configured for hiccup.

**Table 2-1. CFG1-2 Pin Jumper (JP3-4) Selection for Internal Feedback Configuration**

| JP3 (CFG1) | JP4 (CFG2) | SWITCHING FREQUENCY ($f_{SW}$) (kHz) | Valley OCP (A) |
|---|---|---|---|
| VCC | VCC | 600 | 21 |
| VCC(1) | GND(1) | 800 | 21 |
| VCC | Float | 1200 | 21 |
| GND | VCC | 600 | 18 |
| GND | GND | 800 | 18 |
| GND | Float | 1200 | 18 |
| Float | VCC | 600 | 15 |
| Float | GND | 800 | 15 |
| Float | Float | 1200 | 15 |

(1) Default jumper setting

When the device is configured for external feedback operation with the CFG 3-5 pins, the switching frequency, fault recovery mode, overcurrent threshold, and soft start time are programmed by connecting resistors between the CFG1-2 pins and AGND (see Table 2-3). The switching frequency, fault recovery mode, and soft start time are programmed by connecting a resistor (R6) between the CFG1 pin and AGND based on Table 2-2.

**Note**

For external feedback operation, remove jumpers JP3 and JP4 and install R6 and R7.

**Table 2-2. CFG1 Pin Resistor (R6) Selection for External Feedback Configuration**

| R6 (CFG1 PIN RESISTANCE TO AGND)(kΩ) | SWITCHING FREQUENCY ($f_{SW}$) (kHz) | FAULT RECOVERY MODE | SOFT START TIME (ms) |
|---|---|---|---|
| 0 (GND) | 600 | Hiccup | 1 |
| 4.99 | 800 | Hiccup | 1 |
| 7.50 | 1000 | Hiccup | 1 |
| 10.5 | 1200 | Hiccup | 1 |
| 13.3 | 600 | Latch Off | 1 |
| 16.9 | 800 | Latch Off | 1 |
| 21.0 | 1000 | Latch Off | 1 |
| 24.9 | 1200 | Latch Off | 1 |
| 30.1 | 600 | Hiccup | 2 |
| 35.7 | 800 | Hiccup | 2 |
| 42.2 | 1000 | Hiccup | 2 |
| 48.7 | 1200 | Hiccup | 2 |
| 56.2 | 600 | Latch Off | 2 |
| 64.9 | 800 | Latch Off | 2 |
| 75.0 | 1000 | Latch Off | 2 |
| 86.6 | 1200 | Latch Off | 2 |
| 102 | 600 | Hiccup | 3 |
| 118 | 800 | Hiccup | 3 |
| 137 | 1000 | Hiccup | 3 |
| 158 | 1200 | Hiccup | 3 |
| 182 | 600 | Latch Off | 3 |
| 210 | 800 | Latch Off | 3 |
| 243 | 1000 | Latch Off | 3 |
| ≥280 (Float) | 1200 | Latch Off | 3 |

The valley overcurrent protection is programmed with a resistor (R7) between CFG2 and AGND based on Equation 1:

$$R7 = \frac{K_{OCL}}{I_{OCLIM} - \frac{1}{2} \times \frac{(V_{IN} - V_O) \times V_O}{V_{IN}} \times \frac{1}{L \times f_{SW}}} \quad (1)$$

where

- $I_{OCLIM}$ is overcurrent limit threshold for load current in A
- R7 is ILIM resistor value in Ω
- $K_{OCL}$ is a constant of $84 \times 10^3$ for the calculation
- $V_{IN}$ is input voltage value in V
- $V_O$ is output voltage value in V
- L is output inductor value in µH
- $f_{SW}$ is switching frequency in MHz

$$I_{OCLIM} = \frac{K_{OCL}}{R7} + \frac{1}{2} \times \frac{(V_{IN} - V_O) \times V_O}{V_{IN}} \times \frac{1}{L \times f_{SW}} \quad (2)$$

**Note**

TI recommends a ±1% tolerance resistor because a worse tolerance resistor provides less accurate OCL threshold.

To protect the device from an unexpected connection to the ILIM pin, an internal fixed OCL clamp is implemented. This internal OCL clamp limits the maximum valley current on the low-side MOSFET to 21A when the ILIM pin has too small of a resistance to AGND, or is accidentally shorted to ground.

The CFG3-5 pins select the device output voltage configuration as well as FCCM or PFM operation based on Table 2-3.

**Table 2-3. CFG3-5 Pin Jumper (JP5-7) Selections**

| JP5 (CFG3) | JP6 (CFG4) | JP7 (CFG5) | $V_{FB}$ Config | $V_{OUT}$(V) | $F_{SW}$ Mode |
|---|---|---|---|---|---|
| VCC | VCC | VCC | internal | 5.0 | FCCM |
| VCC | GND | VCC | internal | 3.3 | FCCM |
| VCC | Float | VCC | internal | 2.5 | FCCM |
| VCC | VCC | GND | internal | 1.8 | FCCM |
| VCC | GND | GND | internal | 1.5 | FCCM |
| VCC | Float | GND | internal | 1.2 | FCCM |
| VCC | VCC | Float | internal | 1.1 | FCCM |
| VCC | GND | Float | internal | 1.05 | FCCM |
| VCC(1) | Float(1) | Float(1) | internal | 1.0 | FCCM |
| GND | VCC | VCC | internal | 0.95 | FCCM |
| GND | GND | VCC | internal | 0.9 | FCCM |
| GND | Float | VCC | internal | 0.85 | FCCM |
| GND | VCC | GND | internal | 0.8 | FCCM |
| GND | GND | GND | external | 0.5 | FCCM |
| GND | Float | GND | internal | 5.0 | PFM |
| GND | VCC | Float | internal | 3.3 | PFM |
| GND | GND | Float | internal | 2.5 | PFM |
| GND | Float | Float | internal | 1.8 | PFM |
| Float | VCC | VCC | internal | 1.5 | PFM |
| Float | GND | VCC | internal | 1.2 | PFM |
| Float | Float | VCC | internal | 1.1 | PFM |
| Float | VCC | GND | internal | 1.0 | PFM |
| Float | GND | GND | internal | 0.95 | PFM |
| Float | Float | GND | internal | 0.9 | PFM |
| Float | VCC | Float | internal | 0.85 | PFM |
| Float | GND | Float | internal | 0.8 | PFM |
| Float | Float | Float | external | 0.5 | PFM |

(1) Default jumper setting

### 2.1.2 Setting Output Voltage Using External Feedback Configuration

In the External Feedback configuration (see Table 2-3), the output voltage is set by the resistor divider network of R2 ($R_{FBT}$) and R5 ($R_{FBB}$). The FB pin is regulated to the 0.5V reference voltage ($V_{REF}$). To change the output voltage, adjust the values of resistors R2 and R5. The recommended R5 value is 10kΩ, but the range can be from 1kΩ to 15kΩ. The value of R2 for a specific output voltage can be calculated using Equation 3. After changing R2, the feed-forward capacitor (C29) must also be adjusted accordingly.

$$R2 = R5 \times \left(\frac{V_{OUT}}{0.5\,V} - 1\right) \quad (3)$$

# 3 Implementation Results

## 3.1 Test Setup and Results

This section describes how to properly connect, set up, and use the TPS548B23EVM evaluation module. The section also includes test results typical for the evaluation modules. Measurements are taken with the following conditions unless otherwise noted.

- 12V input
- Room temperature (20°C to 25°C)
- The default setting output voltage of 1V, switching frequency of 800kHz, and maximum current limit setting of 21A

### *3.1.1 Input and Output Connections*

The TPS548B23EVM is provided with input connectors, output connectors, and test points as shown in Table 3-1 and Table 3-2.

To support the minimum input voltage with the full rated load on both outputs with the default EVM, a power supply capable of supplying greater than 10A must be connected to the VIN and PGND terminal blocks (T1) through a pair of 18-AWG wires or better.

The load must be connected to T2. A pair of 10AWG wires or better must be used for each connection. With the maximum current limit setting, the maximum load current capability is near **TBD A** before the TPS548B23 goes into current limit. Wire lengths must be minimized to reduce losses in the wires.

**Table 3-1. Connectors and Jumpers**

| REFERENCE DESIGNATOR | NAME | FUNCTION |
|---|---|---|
| T1 | VIN | VIN screw terminal to connect input voltage |
| T2 | VOUT | VOUT screw terminal to connect load to output |
| JP1 | EN | EN pin selection header:<br>• Short EN – PVIN DIVIDER: EN pin connected to VIN pin through resistor divider (default)<br>• Short EN – GND: EN pin shorted to GND<br>• Open: Float EN |
| JP2 | PG | PG pin selection header:<br>• Short: PG pulled up to VCC pin through a 10kΩ resistor (default)<br>• Open: Float PG |
| JP3 | CFG1 | CFG1 selection header. Use shunt to select VCC, GND, or Float |
| JP4 | CFG2 | CFG2 selection header. Use shunt to select VCC, GND, or Float |
| JP5 | CFG3 | CFG3 selection header. Use shunt to select VCC, GND, or Float |
| JP6 | CFG4 | CFG4 selection header. Use shunt to select VCC, GND, or Float |
| JP7 | CFG5 | CFG5 selection header. Use shunt to select VCC, GND, or Float |

**Table 3-2. Test Points**

| REFERENCE DESIGNATOR | NAME | FUNCTION |
|---|---|---|
| TP1 | VIN_S | VIN test point. Use this for efficiency measurements. |
| TP2 | VOUT_S | VOUT test point. Use this for efficiency, output regulation, and bode plot measurements. |
| TP3 | SW | SW node test point |
| TP4 | VIN | VIN test point |
| TP5 | VOUT | VOUT test point |
| TP6 | PGND | PGND test point |
| TP7 | PGND | PGND test point |
| TP8 | VCC | VCC test point |
| TP9 | BODE-/VOS | Test point between voltage divider network and output voltage. Used for Bode plot measurements. |
| TP10 | BODE+/VOUT_REG | Test point between voltage divider network and output voltage. Used for Bode plot measurements. |
| TP11 | EN | EN test point |
| TP12 | PG | PG test point (pulled up to VCC pin through a 10kΩ resistor) |
| TP13 | GOS | GOS test point |
| TP14 | SW | SMB connector to measure SW node. When using this test point, set the scope for 50Ω termination. The combination of 50Ω termination and 450Ω series resistance creates a 10:1 attenuation. |
| TP15 | VOUT | SMB connector to measure output voltage. When using this test point, set the scope for 1MΩ termination. When using 50Ω termination, a 2:1 divider is created. |
| TP16 | AGND | AGND test point |
| TP17 | AGND | AGND test point |
| TP18 | PGND_S | PGND test point. Use this for efficiency measurements. |
| TP19 | PGND_S | PGND test point. Use this for efficiency measurements. |

### 3.1.2 Efficiency

The efficiency on the TPS548B23EVM is shown in Figure 3-1 and Figure 3-2. The test points used for the efficiency measurement are listed in Table 3-3. Use these test points to minimize the contribution of PCB parasitic power loss to the measured power loss.

The following are some additional test setup considerations to minimize external sources of power dissipation.

- Do not measure the SW pin with TP14 while measuring the efficiency. Measuring the SW pin with this test point loads this node with 500Ω and the efficiency measurement includes the power lost in this external resistance.

**Table 3-3. Efficiency Measurement Test Points**

| TEST POINT NAME | REFERENCE DESIGNATOR | FUNCTION |
|---|---|---|
| VIN_S | TP1 | Input voltage test point connected near pins |
| PGND_S | TP18 | PGND reference test point for input voltage |
| VOUT_S | TP2 | Output voltage test point near output inductor |
| PGND_S | TP19 | PGND reference test point for output voltage |

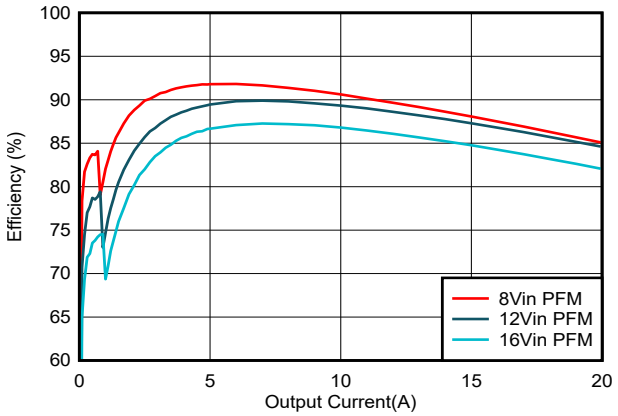



**Figure 3-1. Efficiency – PFM Mode**

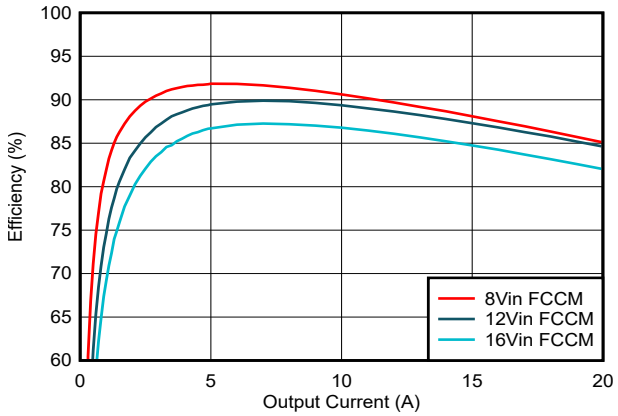



**Figure 3-2. Efficiency – FCCM Mode (Default)**

### 3.1.3 Output Voltage Regulation

The load and line regulation is shown in Figure 3-3 and Figure 3-4. The test points used for the output voltage regulation measurement are shown in Table 3-3.

**Table 3-4. Output Voltage Regulation Measurement Test Points**

| TEST POINT NAME | REFERENCE DESIGNATOR | FUNCTION |
|---|---|---|
| VIN_S | TP1 | Input voltage test point connected near pins |
| PGND_S | TP18 | PGND reference test point for input voltage |
| VOUT_REG/BODE+ | TP10 | Output voltage test point |
| GOS | TP13 | PGND reference test point for output voltage |

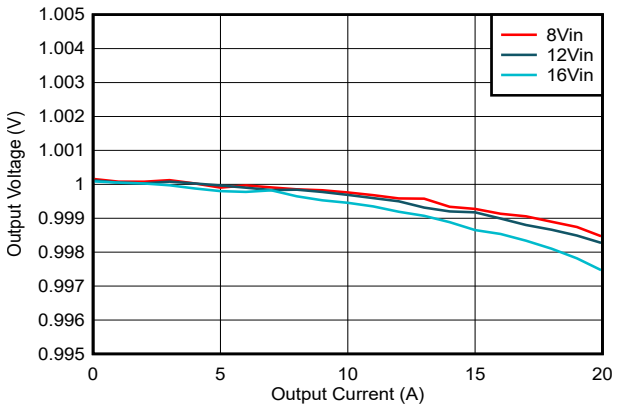



**Figure 3-3. Load Regulation**

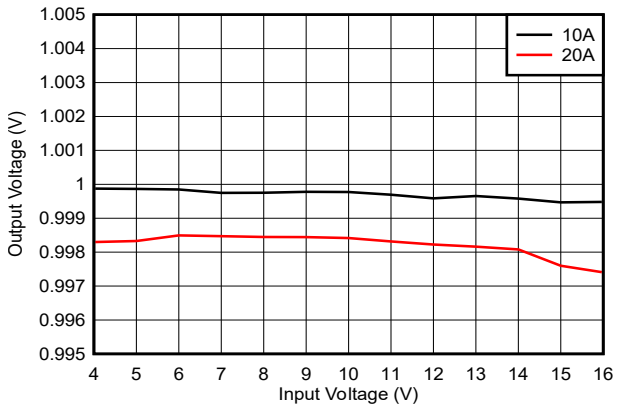



**Figure 3-4. Line Regulation**

### 3.1.4 Load Transient and Loop Response

The response to load transients for both designs is shown in Figure 3-5 and Figure 3-6. The current step is from 5A to 15A and the current step slew rate is 1A/µs. An electronic load is used to provide a DC 5A load and the load transient circuit on the EVM is used to provide a 10A step. The VOUT voltage is measured using TP10.

shows the loop characteristics. Gain and phase plots are shown for $V_{IN}$ voltage of 12V and a 20A load.

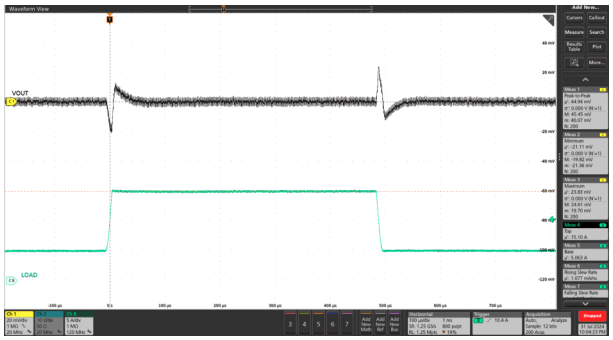



**Figure 3-5. Transient Response**

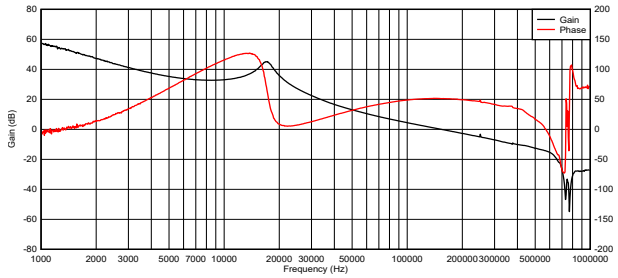



**Figure 3-6. Bode Plot – 10A Load**

### 3.1.5 Output Voltage Ripple

The TPS548B23EVM output voltage ripple is shown in Figure 3-7 through Figure 3-10. The load currents are 10mA, 10A, and 20A. $V_{IN}$ = 12V. The VOUT voltage is measured using TP10.

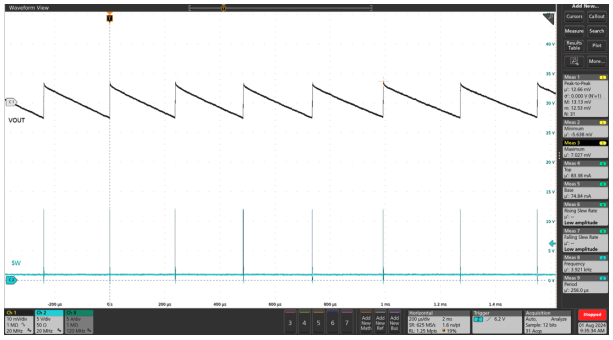



**Figure 3-7. Output Ripple – 10mA Load, PFM Mode**

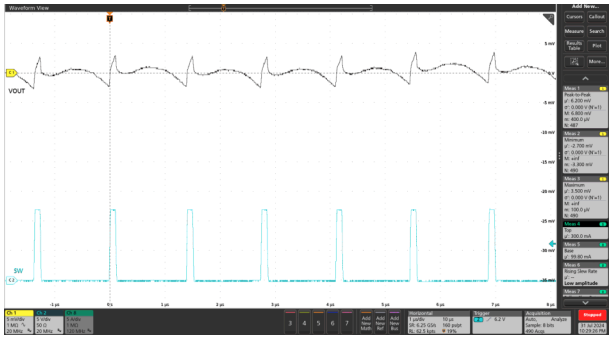



**Figure 3-8. Output Ripple – 10mA Load, FCCM Mode**

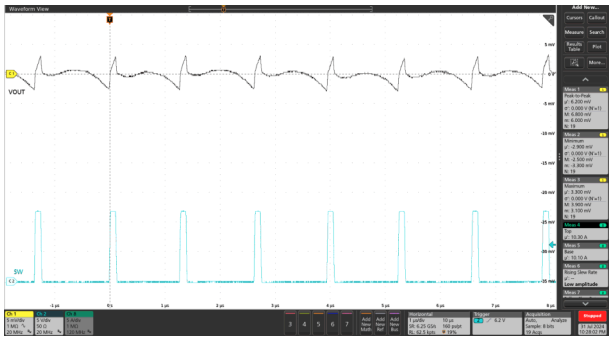



**Figure 3-9. Output Ripple – 10A Load**

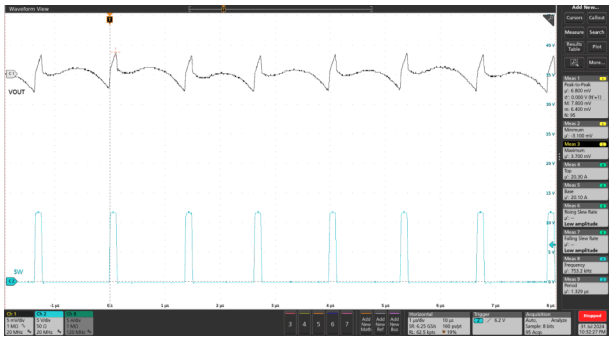



**Figure 3-10. Output Ripple – 20A Load**

### 3.1.6 Start-up and Shutdown with EN

The start-up and shutdown waveforms with EN are shown in Figure 3-11 and Figure 3-12. The input voltage is initially applied and the output is inhibited by pulling EN to GND using an external function generator, as shown in Figure 3-11. When the EN voltage is increased above the enable-threshold voltage, the start-up sequence begins and the output voltage ramps up to the externally set value. The external function generator pulls EN to ground and the TPS548B23 shuts down, as shown in Figure 3-12.

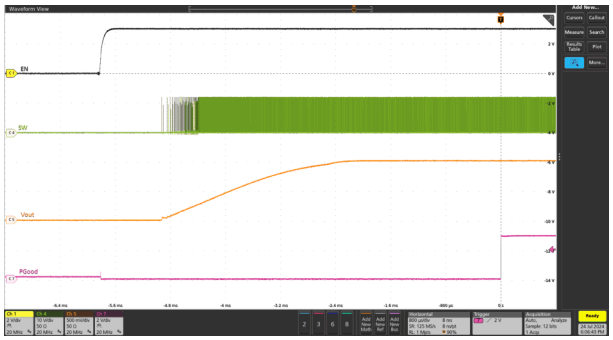



**Figure 3-11. Start-up with EN – 20A Load**

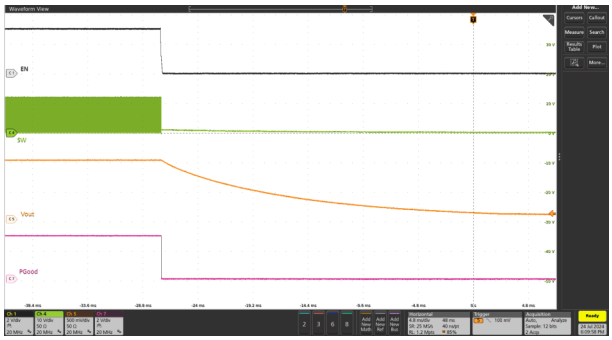



**Figure 3-12. Shutdown with EN – 20A Load**

### 3.1.7 Thermal Performance

The temperature rise of the TPS548B23 ICs at full 20A load is shown in Figure 3-13. A minimum of 10 minutes for soak time was used before taking each measurement.

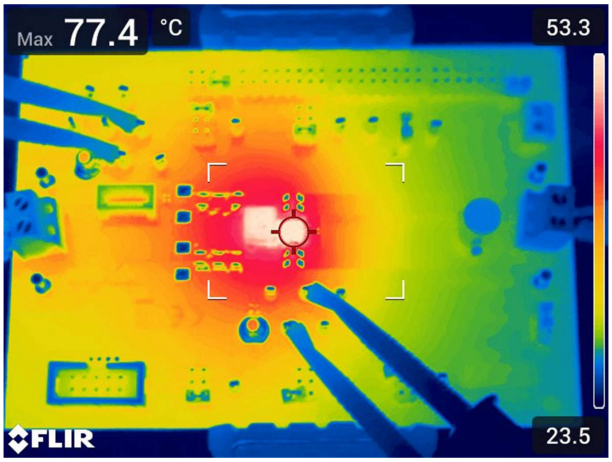



**Figure 3-13. Thermal Performance – 20A Load**

# 4 Hardware Design Files

## 4.1 Schematic

The TPS548B23EVM schematic is shown in Figure 4-1.

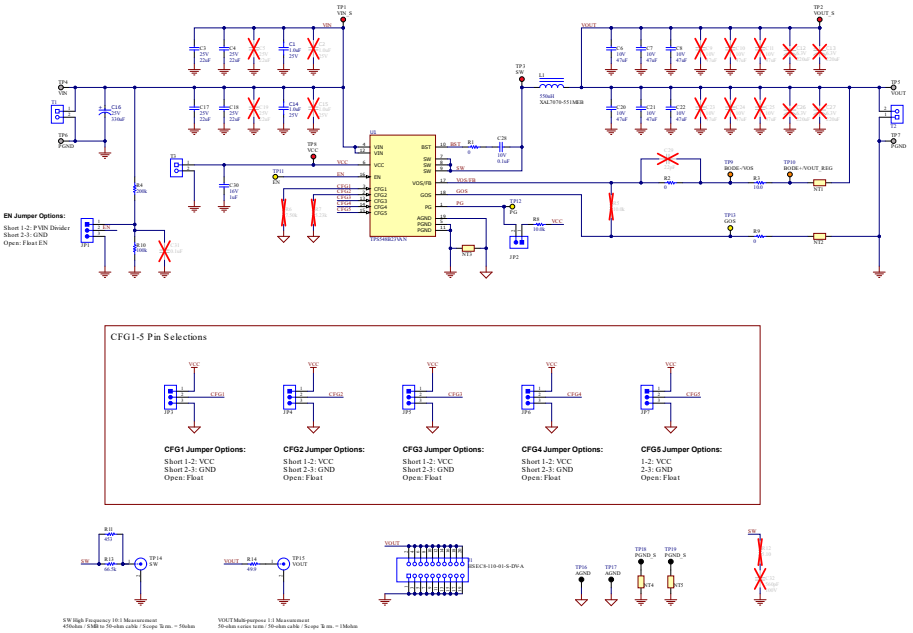



**Figure 4-1. Schematic**

## 4.2 Board Layout

This section provides a description of the TPS548B23EVM board layout and layer illustrations.

### *4.2.1 Layout*

The board layout for the TPS548B23EVM is shown in Figure 4-2 and Figure 4-9. The top-side layer of the EVM is laid out in a manner typical of a user application. The top, bottom, and internal layers are 2-oz. copper.

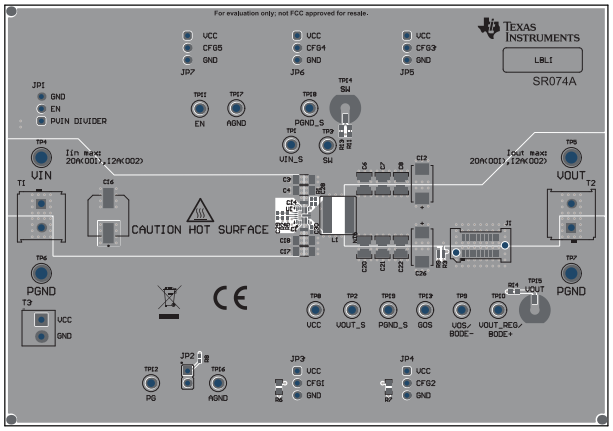



**Figure 4-2. Top-Side Composite View**

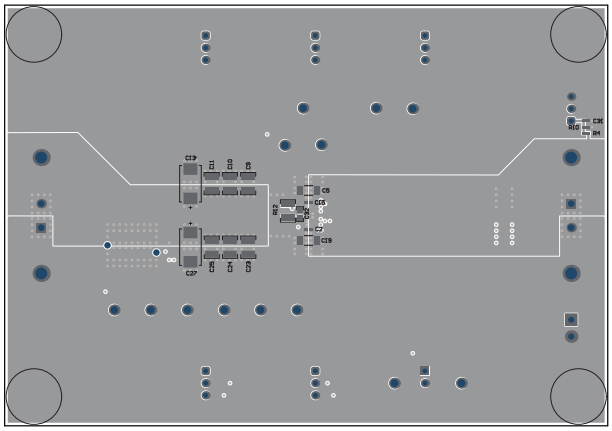


**Figure 4-3. Bottom-Side Composite View (Viewed From Bottom)**

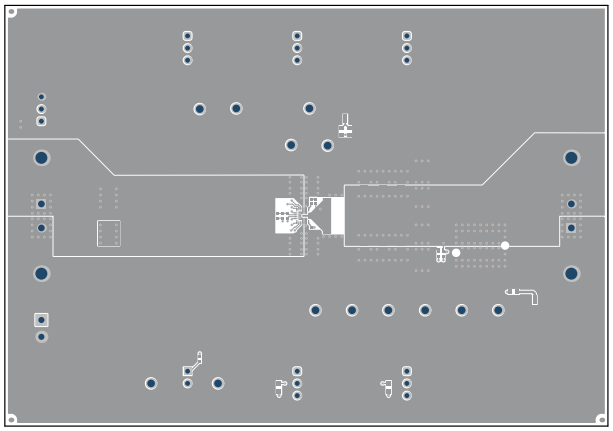


**Figure 4-4. Top Layer Layout**

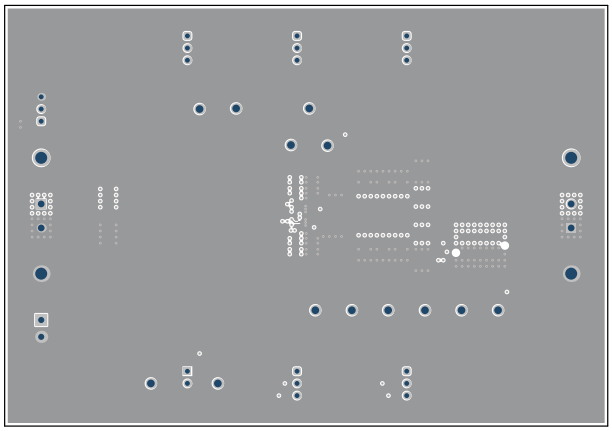


**Figure 4-5. Mid Layer 1 Layout**

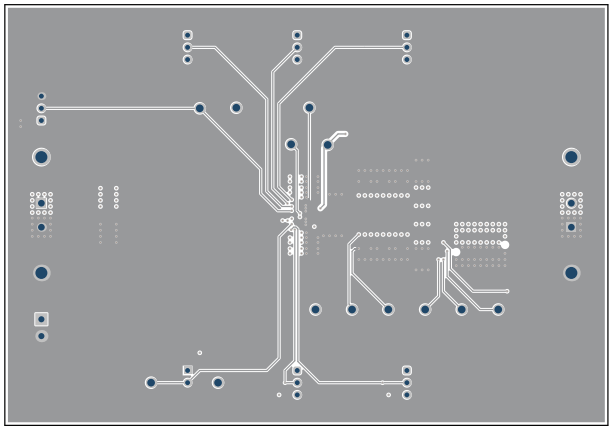


**Figure 4-6. Mid Layer 2 Layout**

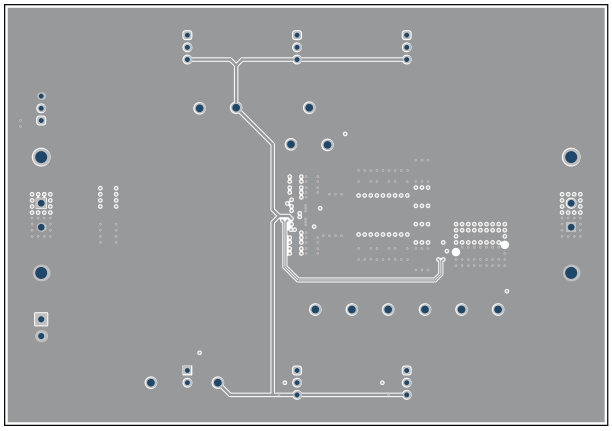


**Figure 4-7. Mid Layer 3 Layout**

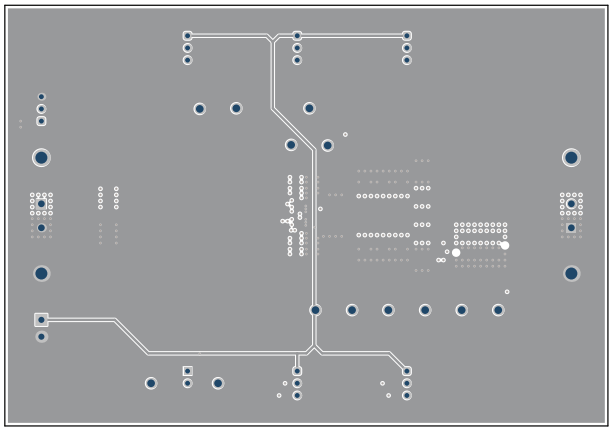


**Figure 4-8. Mid Layer 4 Layout**

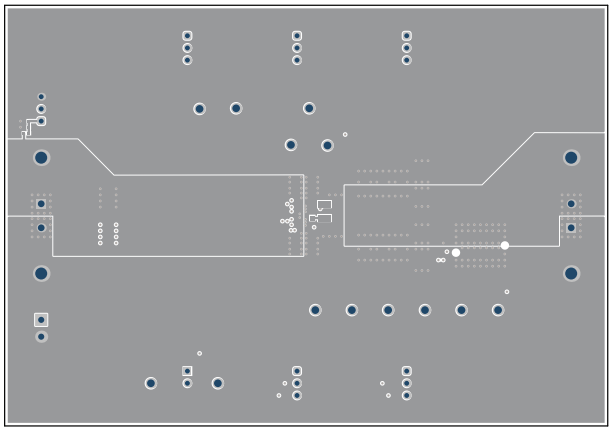


**Figure 4-9. Bottom Layer Layout**

## 4.3 Bill of Materials

The bill of materials for the TPS548B23EVM is detailed in Table 4-1.

**Table 4-1. Bill of Materials**

| Designator | Quantity | Value | Description | Package Reference | Part Number | Manufacturer |
|---|---|---|---|---|---|---|
| !PCB1 | 1 | | Printed Circuit Board | | SR074 | Any |
| C1, C14 | 2 | 1µF | Chip Multilayer Ceramic Capacitors for General Purpose, 0402, 1.0uF, X6S, 22%, 10%, 25V | 402 | GRM155C81E105KE11D | Murata |
| C3, C4, C17, C18 | 4 | 22uF | CAP, CERM, 22uF, 25V, +/- 20%, X6S, 1206_190 | 1206_190 | GRM31CC81E226ME11L | MuRata |
| C6, C7, C8, C20, C21, C22 | 6 | 47uF | CAP, CERM, 47uF, 10V, +/- 20%, X7R, 1210 | 1210 | GRM32ER71A476ME15L | MuRata |
| C16 | 1 | 330µF | Cap Aluminum Polymer 330uF 25V 20% Solder Cylindrical 19m Ohm 2325mA 2000 hr 125°C T/R | SMT_CAP_8MM3_8MM3 | A768KS337M1ELAE019 | KEMET |
| C28 | 1 | 0.1uF | CAP, CERM, 0.1uF, 10V, +/- 10%, X5R, 0402 | 402 | C1005X5R1A104K050BA | TDK |
| C30 | 1 | 1uF | CAP, CERM, 1uF, 16V, +/- 10%, X6S, 0402 | 402 | C1005X6S1C105K050BC | TDK |
| H1, H2, H3, H4 | 4 | | Bumpon, Hemisphere, 0.44 X 0.20, Clear | Transparent Bumpon | SJ-5303 (CLEAR) | 3M |
| J1 | 1 | | Card Edge Socket, 0.8mm, 10x2, SMT | Card Edge Socket, 0.8mm, 10x2, SMT | HSEC8-110-01-S-DV-A | Samtec |
| JP1, JP3, JP4, JP5, JP6, JP7 | 6 | | Header, 100mil, 3x1, Gold, TH | 3x1 Header | TSW-103-07-G-S | Samtec |
| JP2 | 1 | | Header, 100mil, 2x1, Gold, TH | Sullins 100mil, 1x2, 230 mil above insulator | PBC02SAAN | Sullins Connector Solutions |
| L1 | 1 | 550nH | Inductor, Shielded, Composite, 550 nH, 29A, 0.00142 ohm, SMD | 7.2x7x7.5mm | XAL7070-551MEB | Coilcraft |
| LBL1 | 1 | | Thermal Transfer Printable Labels, 0.650" W x 0.200" H - 10,000 per roll | PCB Label 0.650 x 0.200 inch | THT-14-423-10 | Brady |
| R1, R2, R9 | 3 | 0 | RES, 0, 5%, 0.063 W, AEC-Q200 Grade 0, 0402 | 402 | CRCW04020000Z0ED | Vishay-Dale |
| R3 | 1 | 10 | RES, 10.0, 1%, 0.063 W, AEC-Q200 Grade 0, 0402 | 402 | CRCW040210R0FKED | Vishay-Dale |
| R4 | 1 | 200k | RES, 200 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402 | 402 | CRCW0402200KFKED | Vishay-Dale |
| R8 | 1 | 10.0k | RES, 10.0 k, 1%, 0.2 W, AEC-Q200 Grade 0, 0402 | 402 | ERJPA2F1002X | Panasonic |
| R10 | 1 | 100k | RES, 100 k, 1%, 0.1 W, 0402 | 402 | ERJ-2RKF1003X | Panasonic |
| R11 | 1 | 453 | RES, 453, 1%, 0.1 W, 0603 | 603 | RC0603FR-07453RL | Yageo |
| R13 | 1 | 66.5k | RES, 66.5 k, 1%, 0.1 W, 0603 | 603 | RC0603FR-0766K5L | Yageo |
| R14 | 1 | 49.9 | RES, 49.9, 1%, 0.1 W, 0603 | 603 | RC0603FR-0749R9L | Yageo |
| SH-J1, SH-J2, SH-J3, SH-J4, SH-J5, SH-J6, SH-J7 | 7 | | Shunt, 100mil, Tin plated, Black | Shunt Connector Black Open Top, 2x1 | SNT-100-BK-T-H | Samtec |
| T1, T2 | 2 | | Therminal Block, 5mm, 2-pole, Tin, TH | TH, 2-Leads, Body 10x10mm, Pitch 5mm | 282856-2 | TE Connectivity |

**Table 4-1. Bill of Materials (continued)**

| Designator | Quantity | Value | Description | Package Reference | Part Number | Manufacturer |
|---|---|---|---|---|---|---|
| T3 | 1 | | Terminal Block, 3.5mm Pitch, 2x1, TH | 7.0x8.2x6.5mm | ED555/2DS | On-Shore Technology |
| TP1, TP2, TP3, TP8 | 4 | | Test Point, Multipurpose, Red, TH | Red Multipurpose Test point | 5010 | Keystone |
| TP4, TP5, TP6, TP7 | 4 | | Terminal, Turret, TH, Triple | Keystone1598-2 | 1598-2 | Keystone |
| TP9, TP10 | 2 | | Test Point, Multipurpose, Orange, TH | Orange Multipurpose Test point | 5013 | Keystone Electronics |
| TP11, TP12, TP13 | 3 | | Test Point, Multipurpose, Yellow, TH | Yellow Multipurpose Test point | 5014 | Keystone Electronics |
| TP14, TP15 | 2 | | Connector, Receptacle, 50 ohm, TH | SMB Connector | SMBR004D00 | JAE Electronics |
| TP16, TP17, TP18, TP19 | 4 | | Test Point, Multipurpose, Black, TH | Black Multipurpose Test point | 5011 | Keystone Electronics |
| U1 | 1 | | 4V to 16V Input, 20A, Remote Sense, D-CAP4 Synchronous Buck Converter | WQFN-HR19 | TPS548B23VAN | Texas Instruments |
| C2, C15 | 0 | 1µF | Chip Multilayer Ceramic Capacitors for General Purpose, 0402, 1.0uF, X6S, 22%, 10%, 25V | 402 | GRM155C81E105KE11D | Murata |
| C5, C19 | 0 | 22uF | CAP, CERM, 22uF, 25V, +/- 20%, X6S, 1206_190 | 1206_190 | GRM31CC81E226ME11L | MuRata |
| C9, C10, C11, C23, C24, C25 | 0 | 47uF | CAP, CERM, 47uF, 10V, +/- 20%, X7R, 1210 | 1210 | GRM32ER71A476ME15L | MuRata |
| C12, C13, C26, C27 | 0 | 220µF | Molded Tantalum Polymer Capacitor 220uF 20% 6.3V life 1000Hours SMD 2917 | 2917 | 6TCF220M5L | Panasonic |
| C29 | 0 | 22pF | CAP, CERM, 22pF, 50V, +/- 5%, C0G/NP0, AEC-Q200 Grade 1, 0402 | 402 | CGA2B2NP01H220J050BA | TDK |
| C31 | 0 | 0.1uF | CAP, CERM, 0.1uF, 50V, +/- 10%, X7R, AEC-Q200 Grade 1, 0402 | 402 | CGA2B3X7R1H104K050BB | TDK |
| C32 | 0 | 560pF | CAP, CERM, 560pF, 100V, +/- 10%, X7R, 0603 | 603 | GRM188R72A561KA01D | MuRata |
| FID1, FID2, FID3 | 0 | | Fiducial mark. There is nothing to buy or mount. | N/A | N/A | N/A |
| R5 | 0 | 10.0k | RES, 10.0 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402 | 402 | CRCW040210K0FKED | Vishay-Dale |
| R6 | 0 | 7.50k | RES, 7.50 k, 1%, 0.1 W, 0603 | 603 | ERJ-3EKF7501V | Panasonic |
| R7 | 0 | 5.23k | RES, 5.23 k, 0.1%, 0.1 W, 0603 | 603 | RT0603BRD075K23L | Yageo America |
| R12 | 0 | 5.1 | RES, 5.10, 1%, 0.5 W, 1210 | 1210 | RC1210FR-075R1L | Yageo |

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## 5.1 Trademarks

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