Technical Reference Manual

TPS652190C Technical Reference Manual

ABSTRACT

This Technical Reference Manual (TRM) can be used as a reference for the default register bits after the NVM download. The end user is responsible for validating the NVM settings for proper system use including any safety impact. This TRM does not provide information about the electrical characteristics, external components, package, or the functionality of the device. For this information and the full register map, refer to the device data sheet available on the TPS65219 product folder at ti.com.

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Trademarks

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1 Introduction

The TPS65219/TPS65220 PMIC is a cost and space optimized solution that has flexible mapping to support the power requirements from different processors and SoCs. This PMIC contains seven regulators; 3 Buck regulators and 4 Low Drop-out Regulators (LDOs). Additionally, it has I2C, GPIOs and configurable multi-function pins. TPS65219 is characterized for -40°C to +105°C ambient temperature and TPS65220 is characterized for -40°C to +125°C ambient temperature. For safety sensitive applications, TPS65220 is functional safety capable. Therefore the TPS65220 development process is a TI-quality managed process, also functional safety FIT rate calculation and Failure mode distribution (FMD) is available for TPS65220. Whenever entering the INITIALIZE state, the PMIC reads its memory and loads the registers with the content from the EEPROM. The EEPROM loading takes approximately 2.3ms. The power-up sequence can only be executed after the EEPROM-load and all rails are discharged below the SCG threshold. This document describes the default configuration programmed on TPS652190C.

Note

The NVM configuration described in this document is ideal for the application described below but can also be used to power other processors or SoCs with equivalent power requirements:

- Processor i.MX 8M Plus
- Memory: DDR4
- VSYS and PVIN_Bx input supply: 5V or 3.3V
- LDO input supply (PVIN_LDOx): 3.3V

2 PDN and Sequence Diagrams

This section details how the TPS65219 power resources and digital signals are connected to the processor and other peripheral components. Some of the external peripherals like uSD card, Ethernet PHY, HDMI among others are optional and might not be needed for the end product.

2.1 TPS652190C Sequence and Power Block Diagram

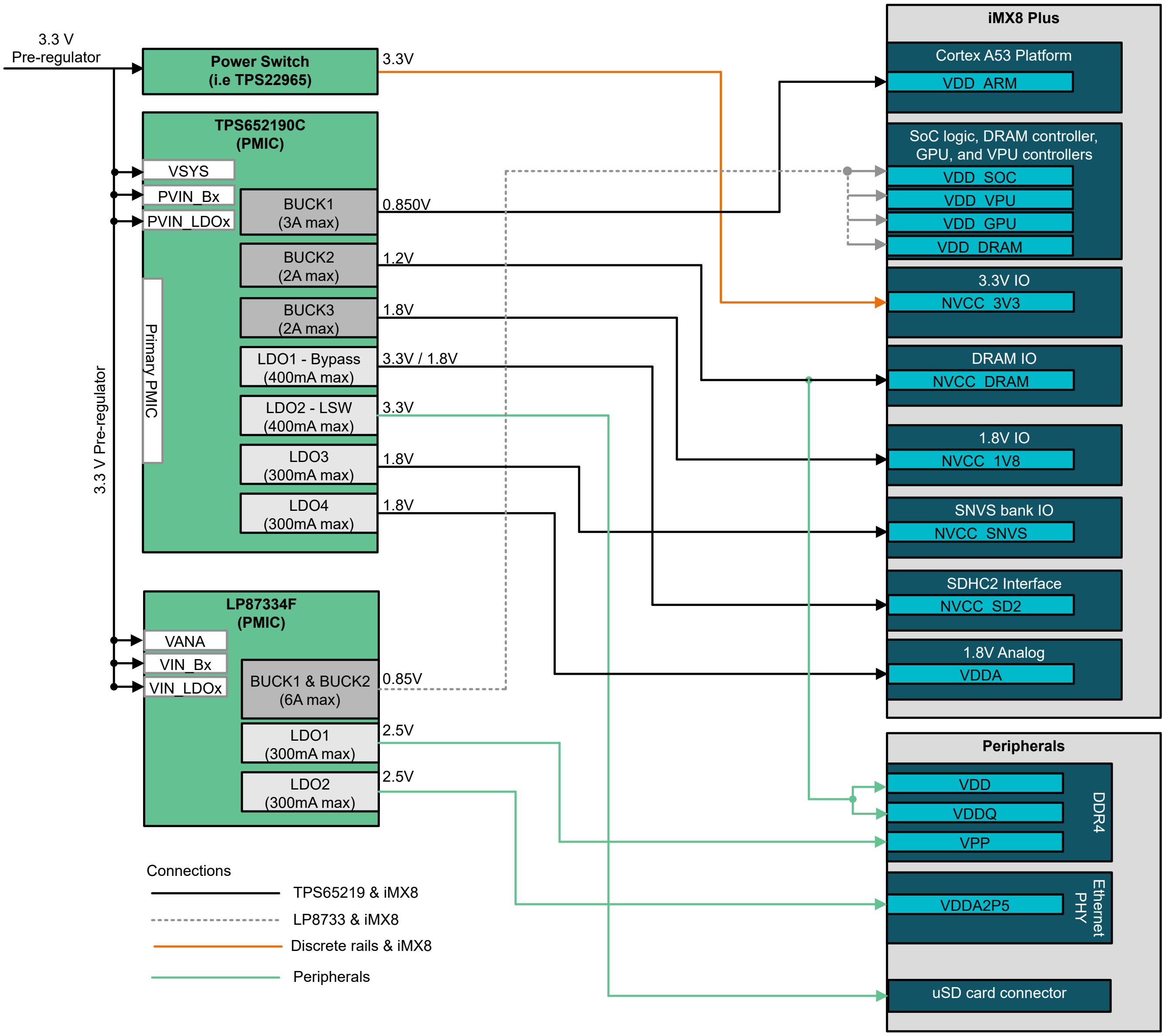


Figure 2-1. TPS652190C Example Diagram

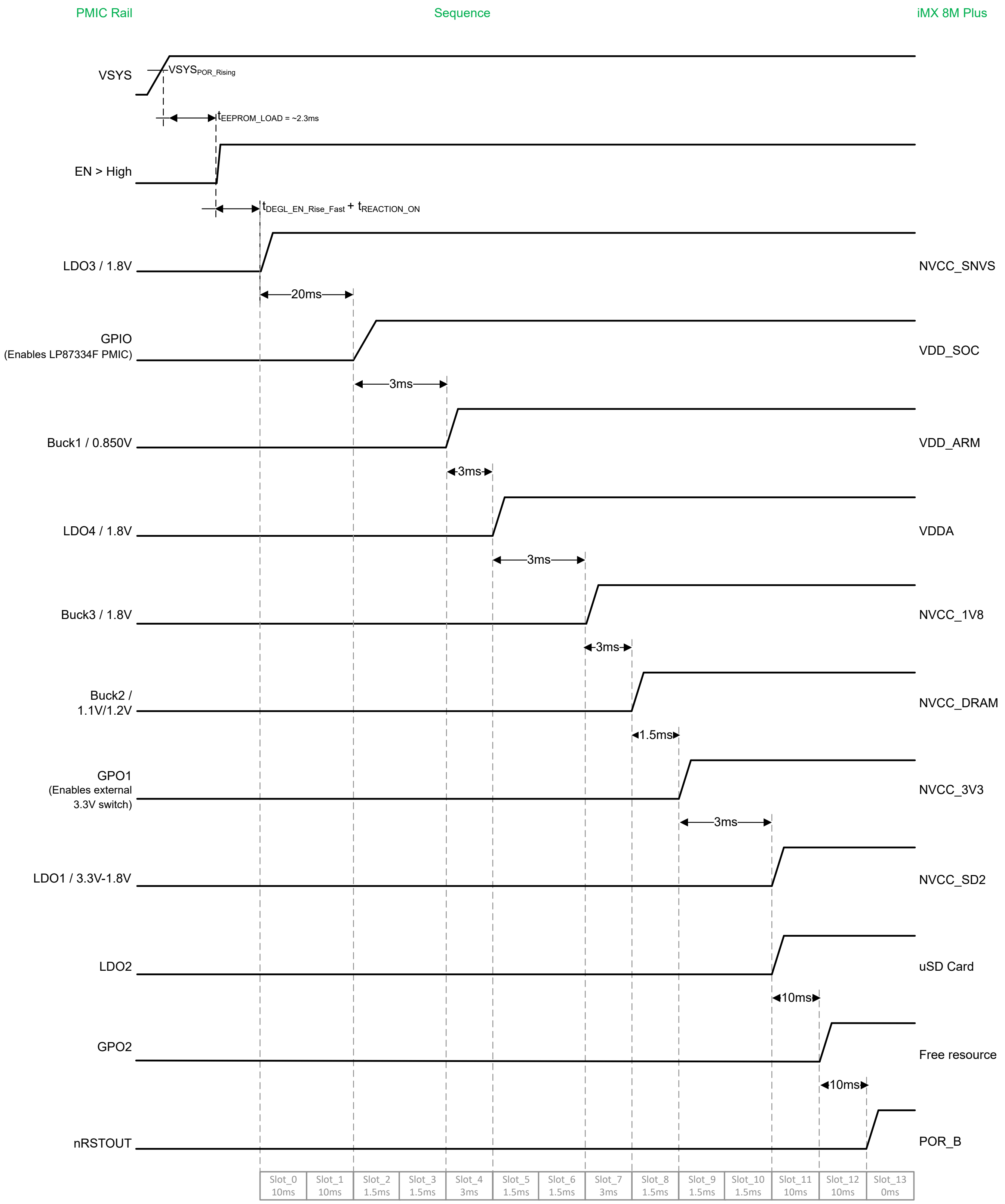
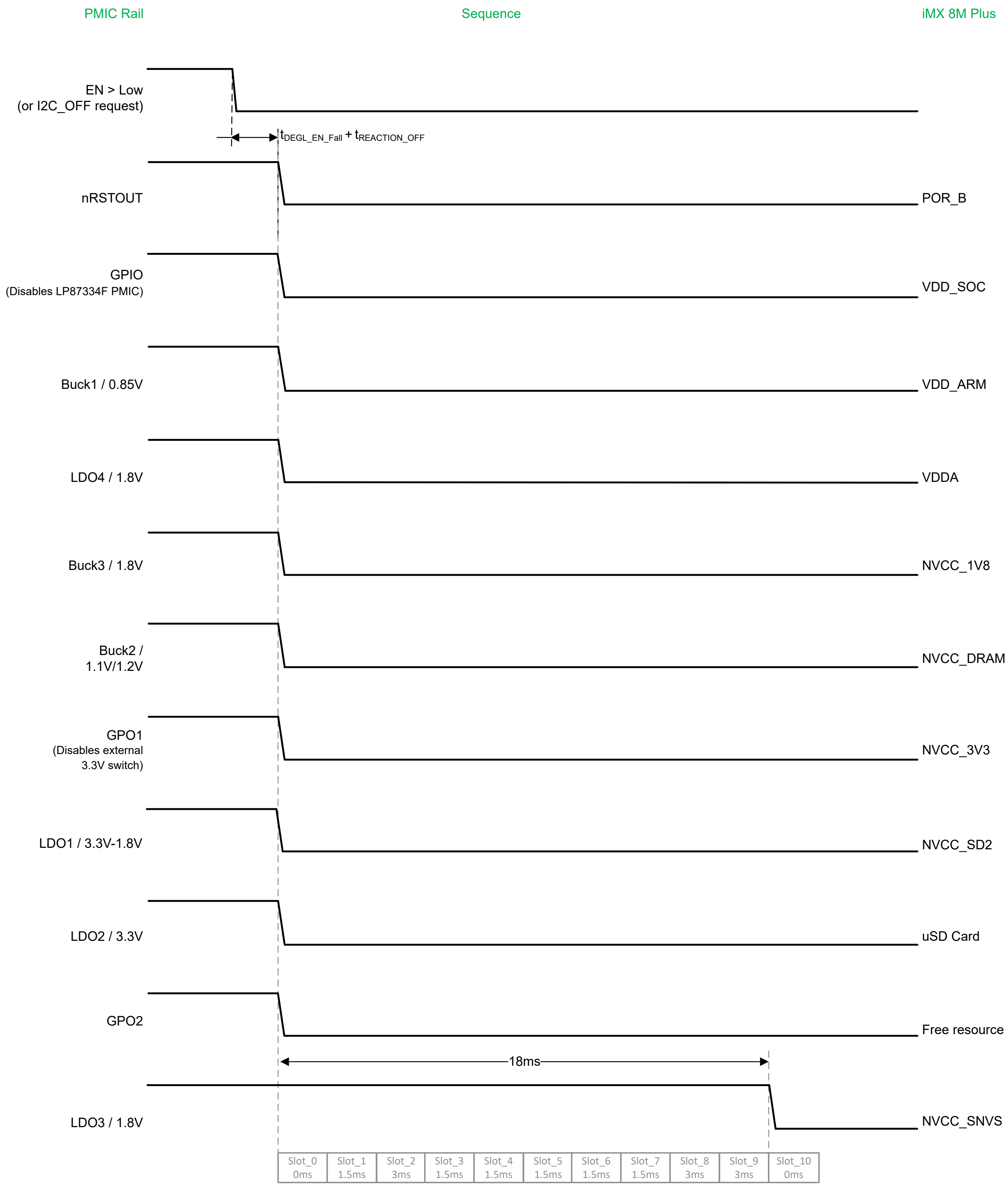


Figure 2-2. TPS652190C Power-Up Sequence



Slot_0	Slot_1	Slot_2	Slot_3	Slot_4	Slot_5	Slot_6	Slot_7	Slot_8	Slot_9	Slot_10
0ms	1.5ms	3ms	1.5ms	1.5ms	1.5ms	1.5ms	1.5ms	3ms	3ms	0ms

Figure 2-3. TPS652190C Power-Down Sequence

3 EEPROM Device Settings

The following sections describe the default configuration on the EEPROM-backed registers. During the power-down-sequence, non-EEPROM-backed bits get reset, with the exception of unmasked interrupt bits and DISCHARGE_EN bits.

3.1 Device ID

This section lists all the register settings to identify the supported temperature and the NVM ID with the corresponding revision that represent a list of default register settings.

Table 3-1. Device ID

Register Address	Field Name	Value	Description
0x00	TI_DEVICE_ID (Bits: 7-5)	0x00	Device specific ID code to identify supported ambient and junction temperature.
0x01	TI_NVM_ID (Bits: 7-0)	0x0C	Identification code for the NVM ID
0x41	NVM_REVISION (Bits: 7-5)	0x2	Identification code for the NVM revision
0x26	I2C_ADDRESS (Bits: 6-0)	0x30	I2C address

3.2 Enable Settings

This section describes the PMIC rails that are enabled in Active and Standby state. Any rail that is disabled by default has the option to be enabled through I2C once the device is in Active state and I2C communication is available.. The transition between Active and Standby state can be triggered by hardware (when MODE/STBY pin is configured as STBY) or by software (register field: STBY_I2C_CTRL).

Table 3-2. ACTIVE state

PMIC Rail	Register Address	Field Name	Value	Description
BUCK1	0x02	BUCK1_EN	0x1	Enabled
BUCK2	0x02	BUCK2_EN	0x1	Enabled
BUCK3	0x02	BUCK3_EN	0x1	Enabled
LDO1	0x02	LDO1_EN	0x1	Enabled
LDO2	0x02	LDO2_EN	0x1	Enabled
LDO3	0x02	LDO3_EN	0x1	Enabled
LDO4	0x02	LDO4_EN	0x1	Enabled
GPO1	0x1E	GPO1_EN	0x1	GPO1 enabled. The output state is Hi-Z.
GPO2	0x1E	GPO2_EN	0x1	GPO2 enabled. The output state is Hi-Z.
GPIO	0x1E	GPIO_EN	0x1	GPIO enabled. The output state is Hi-Z.

Table 3-3. STANBY (STBY) state

PMIC Rail	Register Address	Field Name	Value	Description
BUCK1	0x21	BUCK1_STBY_EN	0x1	Enabled in STBY Mode
BUCK2	0x21	BUCK2_STBY_EN	0x1	Enabled in STBY Mode
BUCK3	0x21	BUCK3_STBY_EN	0x1	Enabled in STBY Mode
LDO1	0x21	LDO1_STBY_EN	0x1	Enabled in STBY Mode
LDO2	0x21	LDO2_STBY_EN	0x1	Enabled in STBY Mode
LDO3	0x21	LDO3_STBY_EN	0x1	Enabled in STBY Mode
LDO4	0x21	LDO4_STBY_EN	0x1	Enabled in STBY Mode
GPO1	0x22	GPO1_STBY_EN	0x1	Enabled in STBY Mode

Table 3-3. STANBY (STBY) state (continued)

PMIC Rail	Register Address	Field Name	Value	Description
GPO2	0x22	GPO2_STBY_EN	0x1	Enabled in STBY Mode
GPIO	0x22	GPIO_STBY_EN	0x1	Enabled in STBY Mode

3.3 Regulator Voltage Settings

This section describes how each of the PMIC power resources were configured.

Table 3-4. Buck Regulator Settings

PMIC Rail	Register Address	Field Name	Value	Description
Bucks Switching Mode (Global for all Buck regulators)	0x03	BUCK_FF_ENABLE (Switching Mode)	0x0	Quasi-fixed frequency mode
	0x03	BUCK_SS_ENABLE (Spread-Specrum)	0x0	Spread spectrum disabled (only applicable if BUCK_FF_ENABLE=0x1)
BUCK1	0x1A	BUCK1_VSET (Output Voltage)	0xA	0.850V
	0x1A	BUCK1_UV_THR_SEL (UV threshold)	0x0	-5% UV detection
	0x1A	BUCK1_BW_SEL (Bandwidth)	0x1	high bandwidth
BUCK2	0x09	BUCK2_VSET (Output Voltage)	0x18	1.200V
	0x09	BUCK2_UV_THR_SEL (UV threshold)	0x0	-5% UV detection
	0x09	BUCK2_BW_SEL (Bandwidth)	0x1	high bandwidth
	0x03	BUCK2_PHASE_CONFIG	0x3	270 degrees (only applicable if BUCK_FF_ENABLE=0x1)
BUCK3	0x08	BUCK3_VSET (Output Voltage)	0x24	1.800V
	0x08	BUCK3_UV_THR_SEL (UV threshold)	0x0	-5% UV detection
	0x08	BUCK3_BW_SEL (Bandwidth)	0x1	high bandwidth
	0x03	BUCK3_PHASE_CONFIG	0x2	180 degrees (only applicable if BUCK_FF_ENABLE=0x1)

Note

- When Bucks are configured for quasi-fixed frequency (**BUCK_FF_ENABLE=0x0**), changing the switching mode between auto-PFM and forced-PWM can be triggered by I2C (MODE_I2C_CTRL) or with one of the multi-function pins (MODE/RESET or MODE/STBY) if one of them is configured as MODE. "Forced PWM" has priority over "Auto PFM".
- "BUCK2_PHASE_CONFIG", "BUCK3_PHASE_CONFIG" and "BUCK_SS_ENABLE" are only applicable when the Buck regulators are configured for fixed frequency (**BUCK_FF_ENABLE=0x1**).

Table 3-5. LDO Regulator Settings

PMIC Rail	Setting	Register Address	Field Name	Value	Description
LDO1	output voltage	0x07	LDO1_VSET	0x36	3.300V
	Rail configuration	0x07	LDO1_LSW_CONFIG	0x0	Not Applicable (LDO1 not configured as load-switch)
		0x07	LDO1_BYP_CONFIG	0x1	LDO1 configured as Bypass (only applicable if LDO1_LSW_CONFIG=0x0)
	UV threshold	0x1E	LDO1_UV_THR	0x0	-5% UV detection
LDO2	output voltage	0x06	LDO2_VSET	0x36	3.300V
	Rail configuration	0x06	LDO2_LSW_CONFIG	0x1	LDO1 configured as Load-switch
		0x06	LDO2_BYP_CONFIG	0x0	LDO2 configured as LDO (only applicable if LDO2_LSW_CONFIG=0x0)
	UV threshold	0x1E	LDO2_UV_THR	0x0	-5% UV detection
LDO3	output voltage	0x05	LDO3_VSET	0x18	1.800V
	Rail configuration	0x05	LDO3_LSW_CONFIG	0x0	LDO Mode
	ramp configuration	0x05	LDO3_SLOW_PU_RAMP	0x0	Fast ramp for power-up (~660us)
	UV threshold	0x1E	LDO3_UV_THR	0x0	-5% UV detection
LDO4	output voltage	0x04	LDO4_VSET	0x18	1.800V
	Rail configuration	0x04	LDO4_LSW_CONFIG	0x0	LDO Mode
	ramp configuration	0x04	LDO4_SLOW_PU_RAMP	0x0	Fast ramp for power-up (~660us)
	UV threshold	0x1E	LDO4_UV_THR	0x0	-5% UV detection

Note

- If a LDO is configured in bypass-mode or LSW-mode, UV-detection is not supported.
- If an LDO is configured in bypass-mode, the corresponding PVIN_LDOx supply must match the configured output voltage in the *LDOx_VOUT* register.
- If LDO is configured as load-switch (LSW_mode), the desired voltage does not need to be configured in the LDOx_VOUT register.
- In bypass- or LSW-mode, the LDO acts as a switch, where VOUT is VIN minus the drop over the FET-resistance.
- If LDO1 or LDO2 is configured as bypass, it allows voltage and function changes between LDO (VOUT=1.8V) and VOUT=VSET register setting. This voltage/function change can be triggered by hardware (using the VSEL_SD pin when configured as SD) or by software (VSEL_SD_I2C_CTRL).

3.4 Sequence Settings

This section breaks out the power sequence settings for the device including the power-up/power-down slot assignment and duration. There may be slots in which no rail nor GPO is assigned to ramp. In this case, we use a combination of slot durations to achieve desired delay times or allow to increase/reduce the timings.

3.4.1 Power-Up Sequence

Table 3-6. Power-Up Sequence - Slot Assignment

PMIC Rail	Register Address	Field Name	Value	Description
BUCK1	0x11	BUCK1_SEQUENCE_ON_SLOT	0x4	slot 4
BUCK2	0x10	BUCK2_SEQUENCE_ON_SLOT	0x8	slot 8
BUCK3	0x0F	BUCK3_SEQUENCE_ON_SLOT	0x7	slot 7
LDO1	0x0E	LDO1_SEQUENCE_ON_SLOT	0xB	slot 11
LDO2	0x0D	LDO2_SEQUENCE_ON_SLOT	0xB	slot 11
LDO3	0x0C	LDO3_SEQUENCE_ON_SLOT	0x0	slot 0
LDO4	0x0B	LDO4_SEQUENCE_ON_SLOT	0x5	slot 5

Table 3-6. Power-Up Sequence - Slot Assignment (continued)

PMIC Rail	Register Address	Field Name	Value	Description
GPO1	0x15	GPO1_SEQUENCE_ON_SLOT	0x9	slot 9
GPO2	0x14	GPO2_SEQUENCE_ON_SLOT	0xC	slot 12
GPIO	0x13	GPIO_SEQUENCE_ON_SLOT	0x2	slot 2
nRSTOUT	0x12	nRST_SEQUENCE_ON_SLOT	0xD	slot 13

Note

PMIC rails are turned ON during the power-up sequence if the corresponding EN bit on section "Enable Setting" is set to 0x01.

Table 3-7. Power-Up Sequence - Slot Duration

	Register Address	Field Name	Value	Description
SLOT0	0x16	POWER_UP_SLOT_0_DURATION	0x3	10ms
SLOT1	0x16	POWER_UP_SLOT_1_DURATION	0x3	10ms
SLOT2	0x16	POWER_UP_SLOT_2_DURATION	0x1	1.5ms
SLOT3	0x16	POWER_UP_SLOT_3_DURATION	0x1	1.5ms
SLOT4	0x17	POWER_UP_SLOT_4_DURATION	0x2	3ms
SLOT5	0x17	POWER_UP_SLOT_5_DURATION	0x1	1.5ms
SLOT6	0x17	POWER_UP_SLOT_6_DURATION	0x1	1.5ms
SLOT7	0x17	POWER_UP_SLOT_7_DURATION	0x2	3ms
SLOT8	0x18	POWER_UP_SLOT_8_DURATION	0x1	1.5ms
SLOT9	0x18	POWER_UP_SLOT_9_DURATION	0x1	1.5ms
SLOT10	0x18	POWER_UP_SLOT_10_DURATION	0x1	1.5ms
SLOT11	0x18	POWER_UP_SLOT_11_DURATION	0x3	10ms
SLOT12	0x19	POWER_UP_SLOT_12_DURATION	0x3	10ms
SLOT13	0x19	POWER_UP_SLOT_13_DURATION	0x0	0ms
SLOT14	0x19	POWER_UP_SLOT_14_DURATION	0x0	0ms
SLOT15	0x19	POWER_UP_SLOT_15_DURATION	0x0	0ms

3.4.2 Power-Down Sequence

Table 3-8. Power-Down Sequence - Slot Assignment

	Register Address	Field Name	Value	Description
BUCK1	0x11	BUCK1_SEQUENCE_OFF_SLOT	0x1	slot 1
BUCK2	0x10	BUCK2_SEQUENCE_OFF_SLOT	0x1	slot 1
BUCK3	0x0F	BUCK3_SEQUENCE_OFF_SLOT	0x1	slot 1
LDO1	0x0E	LDO1_SEQUENCE_OFF_SLOT	0x1	slot 1
LDO2	0x0D	LDO2_SEQUENCE_OFF_SLOT	0x1	slot 1
LDO3	0x0C	LDO3_SEQUENCE_OFF_SLOT	0xA	slot 10
LDO4	0x0B	LDO4_SEQUENCE_OFF_SLOT	0x1	slot 1
GPO1	0x15	GPO1_SEQUENCE_OFF_SLOT	0x1	slot 1
GPO2	0x14	GPO2_SEQUENCE_OFF_SLOT	0x1	slot 1
GPIO	0x13	GPIO_SEQUENCE_OFF_SLOT	0x0	slot 0
nRSTOUT	0x12	nRST_SEQUENCE_OFF_SLOT	0x1	slot 1

Table 3-9. Power-Down Sequence - Slot Duration

	Register Address	Field Name	Value	Description
SLOT0	0x16	POWER_DOWN_SLOT_0_DURATION	0x0	0ms
SLOT1	0x16	POWER_DOWN_SLOT_1_DURATION	0x1	1.5ms

Table 3-9. Power-Down Sequence - Slot Duration (continued)

	Register Address	Field Name	Value	Description
SLOT2	0x16	POWER_DOWN_SLOT_2_DURATION	0x2	3ms
SLOT3	0x16	POWER_DOWN_SLOT_3_DURATION	0x1	1.5ms
SLOT4	0x17	POWER_DOWN_SLOT_4_DURATION	0x1	1.5ms
SLOT5	0x17	POWER_DOWN_SLOT_5_DURATION	0x1	1.5ms
SLOT6	0x17	POWER_DOWN_SLOT_6_DURATION	0x1	1.5ms
SLOT7	0x17	POWER_DOWN_SLOT_7_DURATION	0x1	1.5ms
SLOT8	0x18	POWER_DOWN_SLOT_8_DURATION	0x2	3ms
SLOT9	0x18	POWER_DOWN_SLOT_9_DURATION	0x2	3ms
SLOT10	0x18	POWER_DOWN_SLOT_10_DURATION	0x0	0ms
SLOT11	0x18	POWER_DOWN_SLOT_11_DURATION	0x0	0ms
SLOT12	0x19	POWER_DOWN_SLOT_12_DURATION	0x0	0ms
SLOT13	0x19	POWER_DOWN_SLOT_13_DURATION	0x0	0ms
SLOT14	0x19	POWER_DOWN_SLOT_14_DURATION	0x0	0ms
SLOT15	0x19	POWER_DOWN_SLOT_15_DURATION	0x0	0ms

3.5 EN / PB / VSENSE Settings

The EN/PB/VSENSE pin is used to enable or disable the PMIC. This pin can be configured in one of three ways: EN, PB or VSENSE. The table below shows the default configuration on for this TRM which is linked to a specific part number. Please note, if the FSD (First supply detection) feature is enabled, the device goes from "No Power" to "Active" state, executing the power-up sequence as soon as the voltage on VSYS is above the POR threshold. In this scenario, the EN/PB/VSENSE pin is ignored ONLY during the first power-up.

Table 3-10. EN / PB / VSENSE Settings

	Register Address	Field Name	Value	Description
Pin Config	0x20	EN_PB_VSENSE_CONFIG	0x0	Device Enable Configuration
ON Deglitch	0x20	EN_PB_VSENSE_DEGL	0x0	short (typ: 120us for EN/VSENSE and 200ms for PB)
First Supply Detection	0x20	PU_ON_FSD	0x0	First Supply Detection (FSD) Disabled.

Note

The deglitch configured on register field "EN_PB_VSENSE_DEGL" is for the ON request. The deglitch for the OFF request is not configurable. The parameters that are not configurable can be found in the Specifications section of the device data sheet.

3.6 Multi-Function Pin Settings

The TPS65219 PMIC has three multi-function pins that can be configured to set the voltage on a specific power rail or to change the frequency mode or to trigger a warm or cold reset. This section describes how each of the multi-function pins were configured.

Table 3-11. Multi-Function Pin Settings

Pin Name	Setting	Register Address	Field Name	Value	Description
VSEL_SD / VSEL_DDR	Function selection	0x1F	VSEL_DDR_SD	0x1	VSEL pin configured as SD to set the voltage on the VSEL_RAIL
	Rail selection	0x1F	VSEL_RAIL	0x0	LDO1 (only applicable if VSEL_DDR_SD=0x1)
	pin polarity	0x1F	VSEL_SD_POLARITY	0x1	HIGH - 1.8V / LOW - LDOx_VOUT register setting (only applicable if VSEL_DDR_SD=0x1)

Table 3-11. Multi-Function Pin Settings (continued)

Pin Name	Setting	Register Address	Field Name	Value	Description
MODE / STBY	function selection	0x20	MODE_STBY_CONFIG	0x0	MODE
	pin polarity	0x1F	MODE_STBY_POLARITY	0x0	[if configured as MODE] LOW - auto-PFM / HIGH - forced PWM. [if configured as a STBY] LOW - STBY state / HIGH - ACTIVE state.
MODE / RESET	function selection	0x20	MODE_RESET_CONFIG	0x1	RESET
	reset selection	0x20	WARM_COLD_RESET_CONFIG	0x0	COLD RESET
	pin polarity	0x1F	MODE_RESET_POLARITY	0x0	[if configured as MODE] LOW - auto-PFM / HIGH - forced PWM. [if configured as RESET] LOW - reset / HIGH - normal operation.

Note

- If LDO1 (or LDO2) is configured as bypass and the VSEL pin is NOT configured as SD (**VSEL_DDR_SD=0x0**), the voltage change on the selected VSEL_RAIL can be changed by I2C (register field: VSEL_SD_I2C_CTRL).

Table 3-12. Default register setting for VSEL_SD_I2C_CTRL

Register Address	Field Name	Value	Description
0x1F	VSEL_SD_I2C_CTRL	0x1	0x0 = 1.8V 0x1 = LDOx_VOUT register setting

- If Bucks are configured for quasi-fixed frequency (**BUCK_FF_ENABLE=0x0**), and none of the multi-function pins are configured as MODE, switching between auto-PFM and forced-PWM can be changed by I2C (register field: MODE_I2C_CTRL).

Table 3-13. Default register setting for MODE_I2C_CTRL

Register Address	Field Name	Value	Description
0x1F	MODE_I2C_CTRL	0x0	0x0 = Auto PFM 0x1 = Forced PWM

3.7 Over-Current Deglitch

This section describes the default settings for the over current deglitch. When any of these registers are set (value = 1b), it enabled the long-deglitch option for the corresponding rail.

Table 3-14. Over Current Deglitch

Register Address	Field Name	Value	Description
0x23	EN_LONG_DEGL_FOR_OC_BUCK1	0x0	Deglitch duration for OverCurrent on BUCK1 is ~20us
0x23	EN_LONG_DEGL_FOR_OC_BUCK2	0x0	Deglitch duration for OverCurrent on BUCK2 is ~20us
0x23	EN_LONG_DEGL_FOR_OC_BUCK3	0x0	Deglitch duration for OverCurrent on BUCK3 is ~20us
0x23	EN_LONG_DEGL_FOR_OC_LDO1	0x0	Deglitch duration for OverCurrent on LDO1 is ~20us
0x23	EN_LONG_DEGL_FOR_OC_LDO2	0x0	Deglitch duration for OverCurrent on LDO2 is ~20us
0x23	EN_LONG_DEGL_FOR_OC_LDO3	0x0	Deglitch duration for OverCurrent on LDO3 is ~20us
0x23	EN_LONG_DEGL_FOR_OC_LDO4	0x0	Deglitch duration for OverCurrent on LDO4 is ~20us

3.8 Mask Settings

This section describes the settings that are masked by default and the effect they have on the device state as well as the nINT pin.

Table 3-15. Mask Settings

	Register Address	Field Name	Value	Description
Mask effects on device state and nINT pin	0x25	MASK_EFFECT	0x03	no state change, nINT reaction, bit set for Faults
UV Mask	0x24	BUCK1_UV_MASK	0x0	un-masked (Faults reported)
	0x24	BUCK2_UV_MASK	0x0	un-masked (Faults reported)
	0x24	BUCK3_UV_MASK	0x0	un-masked (Faults reported)
	0x24	LDO1_UV_MASK	0x0	un-masked (Faults reported)
	0x24	LDO2_UV_MASK	0x0	un-masked (Faults reported)
	0x24	LDO3_UV_MASK	0x0	un-masked (Faults reported)
	0x24	LDO4_UV_MASK	0x0	un-masked (Faults reported)
Power-up retries/ attempts	0x24	MASK_RETRY_COUNT	0x0	Device retries up to 2 times
Die Temperature	0x25	SENSOR_0_WARM_MASK	0x0	un-masked (Faults reported)
	0x25	SENSOR_1_WARM_MASK	0x0	un-masked (Faults reported)
	0x25	SENSOR_2_WARM_MASK	0x0	un-masked (Faults reported)
	0x25	SENSOR_3_WARM_MASK	0x0	un-masked (Faults reported)
Masking bit to control whether nINT pin is sensitive to PushButton (PB)	0x25	MASK_INT_FOR_PB	0x1	masked (nINT pin not sensitive to any PB events)
Masking bit to control whether nINT pin is sensitive to RV (Residual Voltage)	0x25	MASK_INT_FOR_RV	0x0	un-masked (nINT pin pulled low for any RV events during transition to ACTIVE state or during enabling of rails)

3.9 Discharge Check

Active discharge is enabled by default and not NVM based. Thus, if desired, it need to be disabled after each VSYS-power-cycle. During RESET or OFF-request, the discharge configuration is not reset, as long as VSYS is present. However, in INITIALIZE state and prior to the power-up-sequence, all rails are discharged, regardless of the setting. In case active discharge on a rail is disabled, it does not gate the disable of the subsequent rail, but the sequence is purely timing based. In case of residual voltage, the RV-bit is be set regardless.

Table 3-16. Discharge Check

Register Address	Field Name	Value	Description
0x1E	BYPASS_RAILS_DISCHARGED_CHECK	0x0	Discharged checks enforced

3.10 Multi PMIC Config

The TPS65219 allows to synchronize multiple devices, in case more rails are required to be supplied. The GPIO (pin#16) is an input/output digital pin, however, the input-functionality is only used in multi-PMIC configuration. The I/O-configuration of the GPIO-pin is done by the MULTI_DEVICE_ENABLE bit in MFP_1_CONFIG register. The table below shows the default multi-device register setting. For more information about the TPS65219 multi-PMIC operation, please refer to the device data sheet available on ti.com.

Table 3-17. Multi-PMIC Configuration

Register Address	Field Name	Value	Description
0x1F	MULTI_DEVICE_ENABLE	0x0	Single-device configuration, GPIO pin configured as GPO

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
December 2023	*	Initial Release

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